

3.11.5.5 – DDR2 Specific SDRAM Functions

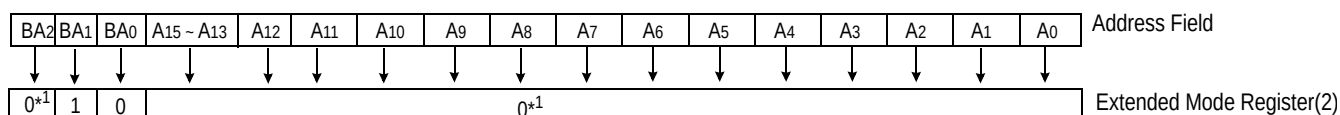
DDR2 SDRAM EMRS2 and EMRS3

For DDR2 SDRAMs, both bits BA0 and BA1 must be decoded for Mode/Extended Mode Register Set commands. Users must initialize all four Mode Registers. The registers may be initialized in any order.

Notes:

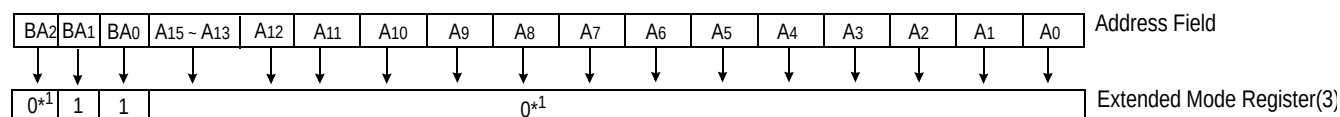
1. Background: This is to ensure future compatibility if/when any new feature is assigned to a bit or bits in EMR(2) or EMR(3).
2. EMR(2) and EMR(3): At this time, there are no features defined which use bit(s) in EMR(2) or EMR(3).

EMR(2) Programming: Reserved*¹



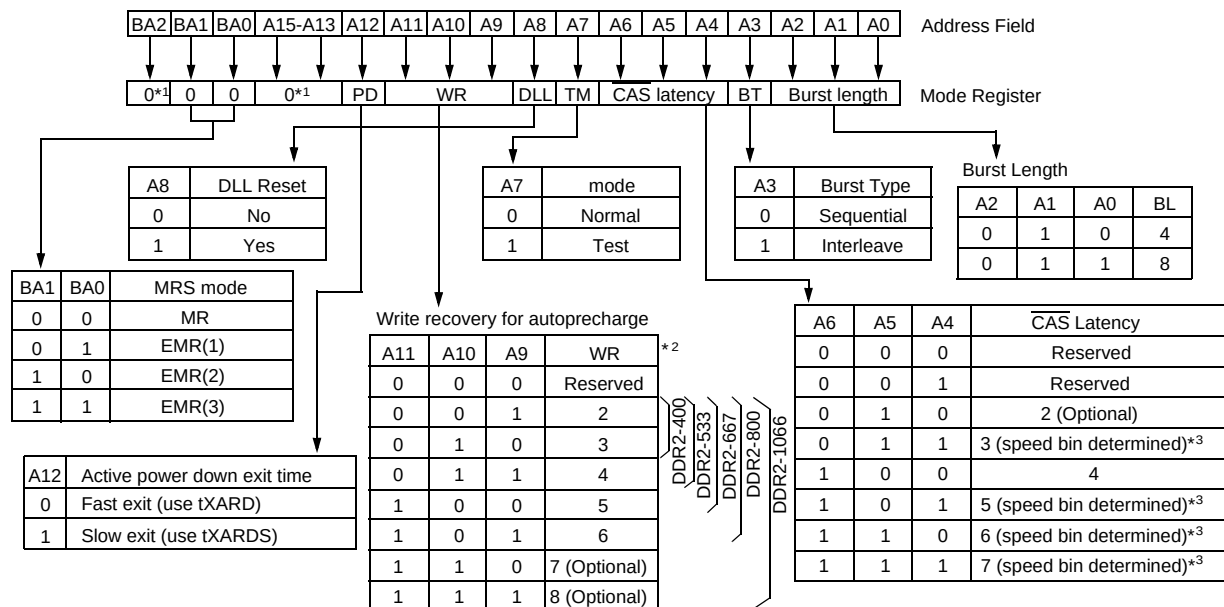
*1: EMRS(2) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

EMR(3) Programming: Reserved*¹



*1: EMRS(3) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

DDR2(x32) SDRAM MR Definition



* A12 must be driven by the system to properly program the mode registers.