

3.11.5.7 – GDDR3 Specific SGRAM Functions

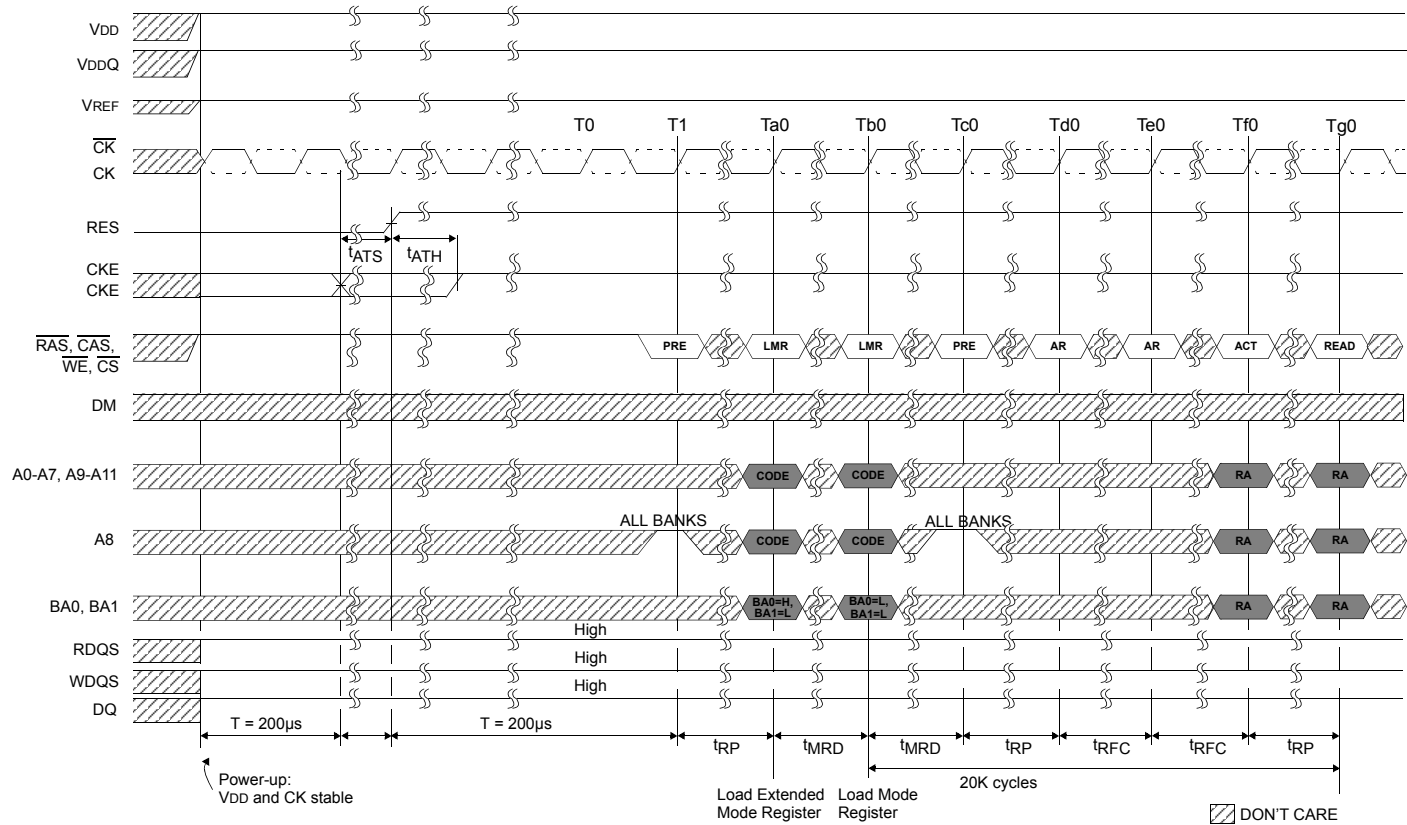
Initialization and Power Up

GDDR3 SGRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must be first applied to VDD and VDDQ simultaneously, and then to VREF. VREF can be applied any time after VDDQ. Once power has been applied and the clocks are stable the GDDR3 device requires 200 μ s before the RES pin transitions to high. Upon power-up and after the clock is stable, the on die termination value for the address and control pins will be set, based on the state of CKE when the RES pin transitions from LOW to HIGH. On the rising edge of RES, the CKE pin is latched to determine the on die termination value for the address and control lines. If CKE is sampled at a logic LOW then the on die termination will be set to 1/2 of ZQ and, if CKE is sampled logic HIGH then the on die termination will be set to the same value as ZQ. CKE must meet tATS and tATH on the rising of RES to set the on die termination for address and control lines. Once tATH is met, set CKE to HIGH. An additional 200 μ s is required for the address and command on die terminations to calibrate and update.

RES must be maintained at a logic LOW-level value and CS must be maintained HIGH, during the first stage of power-up to ensure that the DQ outputs will be in a High-Z state.

After the RES pin transitions from LOW to HIGH wait until a 200 μ s delay is satisfied. Issue DESELECT on the command bus during this time. Issue a PRECHARGE ALL command. Next a LOAD MODE REGISTER command must be issued for the extended mode register (BA1 LOW and BA0 HIGH) to activate the DLL and set operating parameters, followed by the LOAD MODE REGISTER command (BA0/BA1 both LOW) to reset the DLL and to program the rest of the operating parameters. 20k clock cycles are required between the DLL reset and any READ command to allow the DLL to lock. A PRECHARGE ALL command should then be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be issued. Following these requirements, the GDDR3 SGRAM is ready for normal operation.



ODT Control

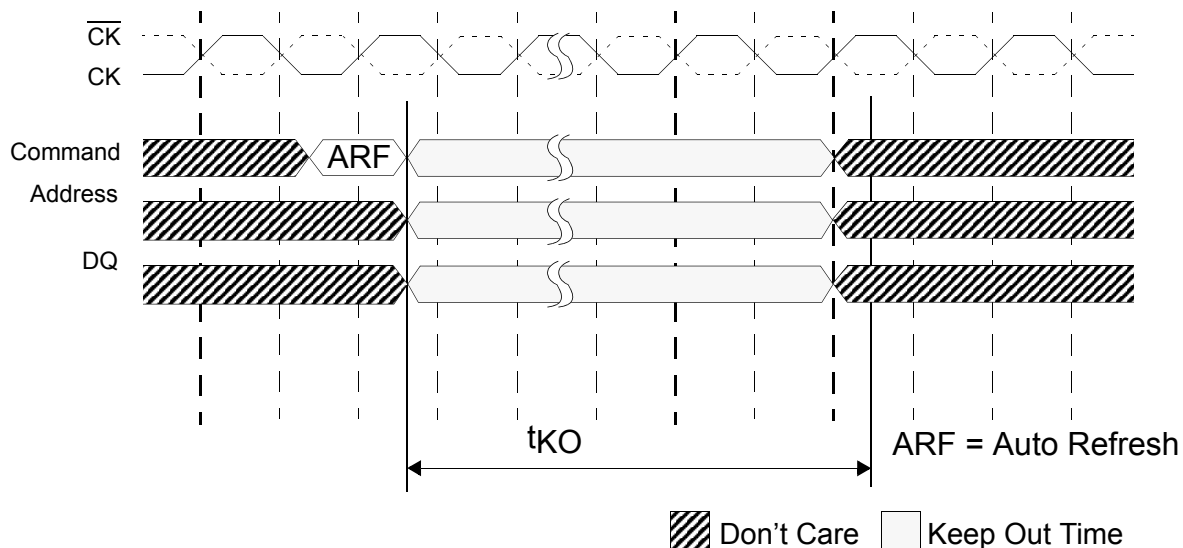
Bus snooping for READ commands excluding CS# is used to control the on die termination in the dual load configuration. The GDDR3 SGRAM will disable the DQ on die terminations when a READ command is detected regardless of the state of CS#. The on die terminations are disabled x clocks after the READ command where x equals $CL - 1$ and stay off for a duration of $BL/2 + 2tCK$. In a two-rank system, DRAM devices on both ranks snoop the bus for READ commands to devices on either rank and all DRAMs will disable the on die terminations, for the DQ pins if a READ command is detected. The on die terminations for input pins on the device such as command (except RES), address, WDQS and DM are always on for both a single-rank system and a dual-rank system unless it is turned off in the EMRS.

ODT Updating

The GDDR3 SGRAM uses a programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ pin and VSSQ. The value of the resistor must be six times the desired driver impedance. For example, a 240 Ω resistor is required for an output impedance of 40 Ω . To ensure that output impedance is one-sixth the value of RQ (within 10 percent), RQ should be in the range of 210 Ω to 270 Ω (35 Ω – 45 Ω output impedance).

The output impedance and on die termination is updated during every AUTO REFRESH commands to compensate for variations in supply voltage and temperature. The output impedance updates are transparent to the system. Impedance updates do not affect device operation, and all datasheet timings and current specifications are met during an update.

A maximum of eight AUTO REFRESH commands can be posted to any given GDDR3 SGRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 9×7.8 us (70.2 us). This maximum absolute interval guarantees that the output drivers and the on die terminations of GDDR3 SGRAMs are recalibrated often enough to keep the impedance characteristics of those within the specified boundaries. During the minimum keep out time of t_{KO} after AUTO REFRESH command, DES (i.e. /CS HIGH) should be issued on the command bus, and no activity on the address or data bus is recommended, because the signal integrity on the bus can not be guaranteed during this period.



Definition of Terminology

Hereafter are defined terminologies used in the GDDR3 SGRAM specification.

Although GDDR3 might be operated in ODT Disable Mode, it is not recommended and the specification describes the ODT Enable Mode only. Should a system be designed to operate the GDDR3 in ODT Disable Mode, the system should comprehend the effect of the discrepancies between this specification and its own design.

If it is stated that a bus is in one of the following state, it should be interpreted as described.

Following are three terminologies defined for ODT Enable Mode.

High{terminated}: A driver on the bus is driving the bus. One or more termination (ODT) on the bus is turned-on. The voltage level of the bus would be nominally VDDQ.

Hi-z{terminated}: No driver on the bus is driving the bus. One or more termination (ODT) on the bus is turned-on. The voltage level of the bus would be nominally VDDQ.

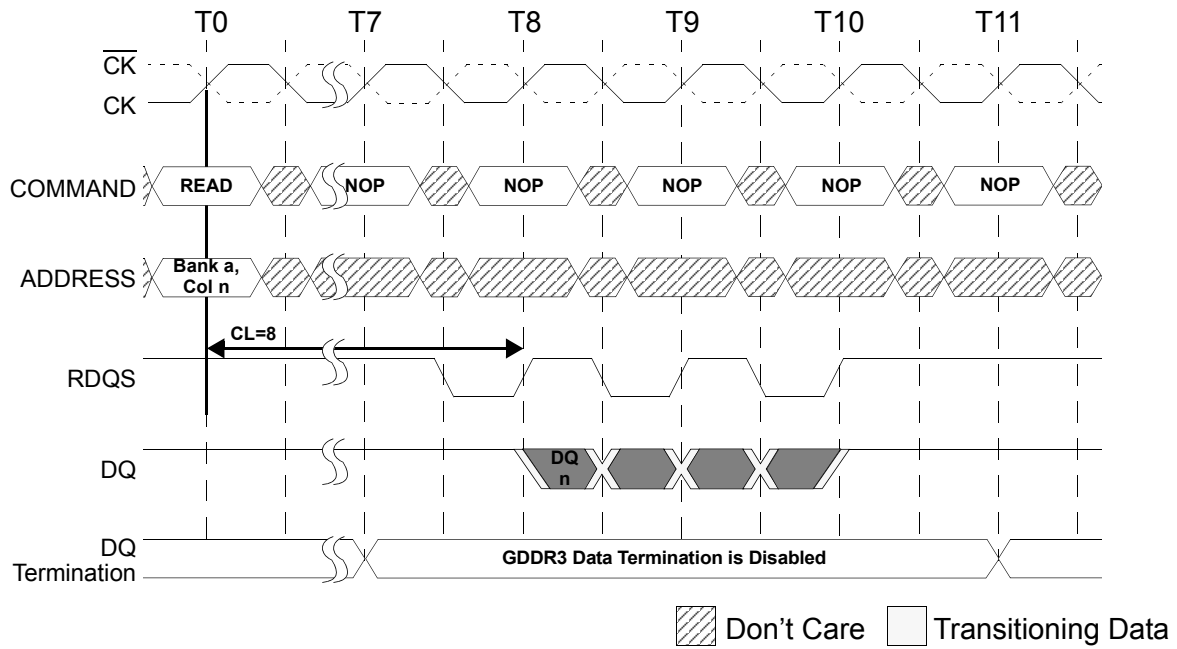
Low{terminated}: A driver on the bus is driving the bus. One or more termination (ODT) on the bus is turned-on. The voltage level of the bus would be nominally VOL(DC).

Corresponding terminologies for ODT Disable Mode are defined below. As mentioned before, ODT Disable Mode is not an intended mode of operation. However, there exist situations where ODT Enable Mode can not be guaranteed for a short period of time, like during power up, yet is indeed an intended mode of operation

High{unterminated}: A driver on the bus is driving the bus. No termination on the bus is active. The voltage level of the bus would be nominally VDDQ.

Hi-z{unterminated}: No driver on the bus is driving the bus. No termination on the bus is active. The voltage level of the bus would be undefined, because the bus would be floating.

Low{unterminated}: A driver on the bus is driving the bus. No termination on the bus is active. The voltage level of the bus would be nominally VSSQ.



READ Timing

The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after t_{RAS} min has been met.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative strobe edges. The GDDR3 SGRAM drives the output data edge aligned to RDQS. The initial HIGH transitioning LOW of RDQS is known as the read preamble; the half cycle coincident with the last data-out element is known as the read postamble. The GDDR3 devices starts to drive the preamble 1/2 clock cycle prior to the first falling edge of RDQS and continues to drive RDQS until 1/2 clock cycle after the last rising edge of the Postamble. RDQS also can only toggle when there is valid data on the bus.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go to VDD do to the on die termination.

Data from any READ burst may be concatenated with data from a subsequent READ command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued x cycles after the first READ command, where x equals $2x$ the number of data element nibbles depending on the burst length. READ data cannot be terminated or truncated.