

3.11.6 SDRAM Parametric Specifications

The following standards describe parametric specifications and characteristics that are applicable to one or more of the SDRAM devices described in section 3.11 of Std. 21-C.

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3.11.6.1 – DDR SDRAM/SGRAM I/O Voltage

The I/O for DDR SDRAM, VDDQ = 2.5V

Note: This does not preclude interim parts also supporting 3.3V I/O.

3.11.6.2 – 256M SDRAM/SGRAM REFRESH SPECIFICATION

All Synchronous DRAM (SDRAM) with densities of 256 Mb or higher must have the following statement on the pinout diagram:

Note: The standard refresh period is 64 ms.

(THIS STANDARD HAS BEEN MOVED FROM SEC. 3.11.5 TO THIS SECTION IN RELEASE 9)

3.11.6.3 – TIMING SPECIFICATION STANDARDS FOR 16M AND 64M SDRAM (LVTTTL I/O)

Symbol	Parameter	–8		–10		–12		Unit
		Min	Max	Min	Max	Min	Max	
Input Requirements								
tCK3	Clock period (CL=3)	8		10		12		ns
tCK2	Clock period (CL=2)	12		15		18		ns
tCH	CK high level width	3		4		4		ns
tCL	CK low level width	3		4		4		ns
tIS	Input set–up time	2		3		3		ns
tIH	Input hold time	1		1		1		ns
tRC	Row cycle time	72		90		108		ns
tRCD	Row to column delay	24		30		36		ns
tRAS	Row active time	48	20000	60	20000	72	20000	ns
tRP	Row precharge time	24		30		36		ns
tWR	Write recovery time	10		10		12		ns
tRRD	Act to act delay time	16		20		24		ns
tRFC	Row refresh cycle time	80		90		108		ns
tREFI	Average refresh interval time		15.6		15.6		15.6	us
Output Specifications								
tAC3	Data access time from CK (CL=3), tCK≥tCK3(min)		6		7.5		9	ns
tAC2	Data access time from CK (CL=2), tCK≥tCK2(min)		8		9		10	ns
tOH	Data output hold time	2		3		3		ns
tOHN	Data output hold time – no load	1		2		2		ns
tLZ	Data output low impedance	2		2		2		ns
tHZ	Data output high impedance		8		8		8	ns

Notes for reference:

- 1) The timing parameters listed above are the minimum performance requirements to claim adherence to a JEDEC standard for ac SDRAM timing.
- 2) All specifications are guaranteed by the supplier and does not imply that these are test specifications.
- 3) Output loading conditions to be specified in another JEDEC standard.

TABLE 3.11.6.3–1: Timing Parameters for 16M and 64M SDRAM (LVTTTL I/O)

3.11.6.3 (cont.) – SDRAM/SGRAM LVTTL AC TEST CONDITIONS

1. AC measurements assume input transition times, t_T , of 1ns where the value of t_T is measured between $V_{IH}(\min)$ and $V_{IL}(\max)$. Refer to Figure A.
2. Input transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$. Refer to Figure A.
3. The minimum voltage swing for inputs is between $(V_{IH}(\min) + 0.4V)$ and $(V_{IL}(\max) - 0.4V)$. Refer to Figure A.
4. The timing reference level for input signals is the midpoint between $V_{IH}(\min)$ and $V_{IL}(\max)$ {i.e., $[V_{IH}(\min) + V_{IL}(\max)]/2$ Volts}. Refer to Figure B.
5. The reference timing level for output signals is the midpoint between $V_{OH}(\min)$ and $V_{OL}(\max)$ {i.e., $[V_{OH}(\min) + V_{OL}(\max)]/2$ Volts}. Refer to Figure B.
6. The loading for output pins is shown in Figure C. Note that the specification t_{OHN} (data output hold time – no load) does not use the load in Figure C and is intended to specify when the output driver turns off or begins to pull the output to the complementary state.
7. Access times should be guaranteed from worst case conditions which can be generated from other chips in a system. Access times for a logic “1” should be measured with the DQ pin preconditioned to $V_{OL}(\min)$ and access times for a logic “0” should be measured with the DQ pin preconditioned to $V_{OH}(\max)$.

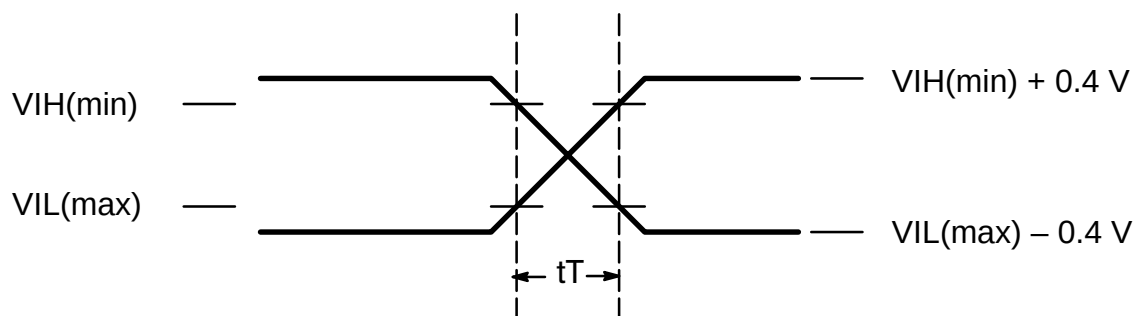


Figure 3.11.6.3-1: LVTTL AC Voltage Swings and Transition times for Input Signals

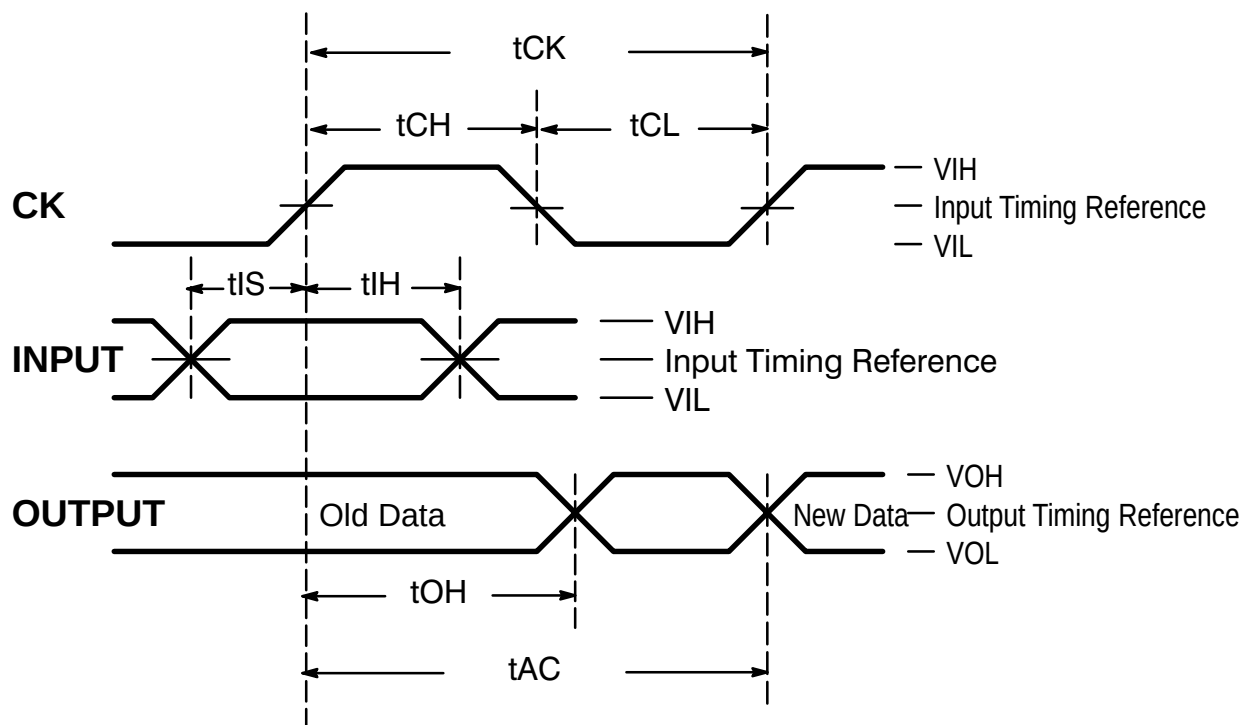
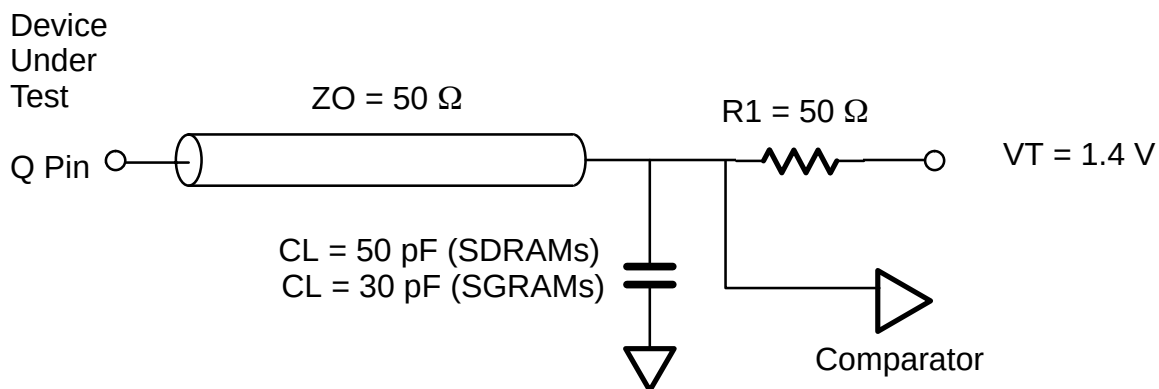


Figure 3.11.6.3-2: LVTTTL AC Test Relationships for Input and Output Signals



Note: CL includes probe and fixture capacitance.

Figure 3.11.6.3-3: LVTTTL AC Test Loading for Output Pins