

Annex J: Serial Presence Detects for DDR2 SDRAM (Revision 1.3)

1.0 Introduction

This appendix describes the serial presence detect values for the DDR2 version of the synchronous DRAM modules. These presence detect values are those referenced in the SPD standard document for 'Specific Features'. The following SPD fields will occur in the order presented in section 1.1. Further descriptions of Bytes 0 and 1 are found in the SPD standard. Further description of Byte 2 is found in Appendix A of the SPD standard. All unused entries will be coded as 00h. All unused bits in defined bytes will be coded as 0 except where noted. "Unused" includes reserved or TBD values.

1.1 Address map

The following is the SPD address map for DDR2 SDRAM. It describes where the individual lookup table entries will be held in the serial EEPROM.

Byte Number	Function Described	Notes
0	Number of Serial PD Bytes written during module production	1
1	Total number of Bytes in Serial PD device	2
2	Fundamental Memory Type (FPM, EDO, SDRAM, DDR, DDR2...)	
3	Number of Row Addresses on this assembly	
4	Number of Column Addresses on this assembly	
5	Number of DIMM Ranks	
6	Data Width of this assembly	
7	Reserved	
8	Voltage Interface Level of this assembly	
9	SDRAM Cycle time at Maximum Supported $\overline{\text{CAS}}$ Latency (CL), CL=X	3
10	SDRAM Access from Clock	
11	DIMM configuration type (Non-parity, Parity or ECC)	
12	Refresh Rate/Type	3, 4
13	Primary SDRAM Width	
14	Error Checking SDRAM Width	
15	Reserved	
16	SDRAM Device Attributes: Burst Lengths Supported	
17	SDRAM Device Attributes: Number of Banks on SDRAM Device	3
18	SDRAM Device Attributes: $\overline{\text{CAS}}$ Latency	3
19	DIMM Mechanical Characteristics	3
20	DIMM Type Information	3
21	SDRAM Module Attributes	
22	SDRAM Device Attributes: General	3
23	Minimum Clock Cycle at CLX-1	3
24	Maximum Data Access Time (tAC) from Clock at CLX-1	3
25	Minimum Clock Cycle at CLX-2	3
26	Maximum Data Access Time (tAC) from Clock at CLX-2	3
27	Minimum Row Precharge Time (tRP)	3
28	Minimum Row Active to Row Active delay (tRRD)	3
29	Minimum RAS to $\overline{\text{CAS}}$ delay (tRCD)	3

Byte Number	Function Described	Notes
30	Minimum Active to Precharge Time (tRAS)	3
31	Module Rank Density	
32	Address and Command Input Setup Time Before Clock (tIS)	3
33	Address and Command Input Hold Time After Clock (tIH)	3
34	Data Input Setup Time Before Strobe (tDS)	3
35	Data Input Hold Time After Strobe (tDH)	3
36	Write recovery time (tWR)	3
37	Internal write to read command delay (tWTR)	3
38	Internal read to precharge command delay (tRTP)	3
39	Memory Analysis Probe Characteristics	
40	Extension of Byte 41 tRC and Byte 42 tRFC	
41	SDRAM Device Minimum Active to Active/Refresh Time (tRC)	3
42	SDRAM Device Minimum Refresh to Active/Refresh Command Period (tRFC)	3
43	SDRAM Device Maximum device cycle time (tCKmax)	3
44	SDRAM Device maximum skew between DQS and DQ signals (tDQSQ)	3
45	SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)	3
46	PLL Relock Time	
47	Bits 7:4: Tcasemax Delta (DRAM case temperature difference between maximum case temperature and baseline maximum case temperature), the baseline maximum case temperature is 85 °C. Bits 3:0: DT4R4W Delta (Case temperature rise difference between IDD4R/page open burst read and IDD4W/page open burst write operations).	7, 8, 11
48	Thermal resistance of DRAM device package from top (case) to ambient (Psi T-A DRAM) at still air condition based on JESD51-2 standard.	6, 10
49	DT0/Tcase Mode Bits: Bits 7:2: Case temperature rise from ambient due to IDD0/activate-precharge operation minus 2.8 °C offset temperature. Bit 1: Double Refresh mode bit. Bit 0: High Temperature self-refresh rate support indication	7, 8, 11
50	DT2N/DT2Q: Case temperature rise from ambient due to IDD2N/precharge standby operation for UDIMM and due to IDD2Q/precharge quiet standby operation for RDIMM.	7, 8, 11
51	DT2P: Case temperature rise from ambient due to IDD2P/precharge power-down operation.	7, 8, 11
52	DT3N: Case temperature rise from ambient due to IDD3N/active standby operation.	7, 8, 11
53	DT3Pfast: Case temperature rise from ambient due to IDD3P Fast PDN Exit/active power-down with Fast PDN Exit operation.	7, 8, 11
54	DT3Pslow: Case temperature rise from ambient due to IDD3P Slow PDN Exit/active power-down with Slow PDN Exit operation.	7, 8, 11
55	DT4R/Mode Bit: Bits 7:1: Case temperature rise from ambient due to IDD4R/page open burst read operation. Bit 0: Mode bit to specify if DT4W is greater or less than DT4R.	7, 8, 11
56	DT5B: Case temperature rise from ambient due to IDD5B/burst refresh operation.	7, 8, 11
57	DT7: Case temperature rise from ambient due to IDD7/bank interleave read mode operation.	7, 8, 11
58	Thermal resistance of PLL device package from top (case) to ambient (Psi T-A PLL) at still air condition based on JESD51-2 standard.	6, 10
59	Thermal resistance of register device package from top (case) to ambient (Psi T-A Register) at still air condition based on JESD51-2 standard.	6, 10
60	DT PLL Active: Case temperature rise from ambient due to PLL in active mode at VCC = 1.9 V, the PLL loading is the DIMM loading.	9, 11

Byte Number	Function Described	Notes
61	DT Register Active/Mode Bit: Bits 7:1: Case temperature rise from ambient due to register in active mode at VCC = 1.9 V, the register loading is the RDIMM loading. Bit 0: mode bit to specify register data output toggle rate 50% or 100%.	9, 11
62	SPD Revision	
63	Checksum for Bytes 0-62	
64-71	Manufacturer's JEDEC ID Code	
72	Module Manufacturing Location	5
73-90	Module Part Number	5
91-92	Module Revision Code	5
93-94	Module Manufacturing Date	
95-98	Module Serial Number	
99-127	Manufacturer's Specific Data	5
128-255	Open for customer use	
1. This will typically be programmed as 128 Bytes. 2. This will typically be programmed as 256 Bytes. 3. From Datasheet. 4. High order bit is Self Refresh "flag". If set to "1", the assembly supports self refresh. 5. These are optional, in accordance with the JEDEC spec. 6. Refer to JESD51-3 "Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages" under JESD51-2 standard. 7. DT parameter is derived as following: $DTx = IDDx * VDD * \Psi T-A$, where $IDDx$ definition is based on JEDEC DDR2 SDRAM Component Specification and at VDD = 1.9 V, it is the datasheet (worst case) value, and $\Psi T-A$ is the programmed value of $\Psi T-A$ (value in SPD Byte 48). Programmed temperature rise data (DTx) is based on the programmed value of $\Psi T-A$ (value in SPD byte 48). 8. All DT parameters are defined for DDR2 DRAM densities up to 2 Gbit. 4 Gbit parameters will be defined later. 9. DT parameters for PLL and register are derived as following: $DTx = IDDx * VDD * \Psi T-A$, where $IDDx$ definition is at VDD = 1.9 V and it is the active PLL or register power corresponding to its respective DIMM configuration loading. The $IDDx$ is the worst case value. $\Psi T-A$ used to program DTx is the programmed value of $\Psi T-A$ (value in SPD byte 58 or byte 59). 10. Rule for rounding off $\Psi T-A$: $\Psi T-A$ shall be rounded such that it is nearest/closest to the true value of $\Psi T-A$. 11. Rule for rounding off DTx: DTx shall be rounded such that it is nearest/closest to the calculated value of DTx.		

2.0 Details of each byte

Byte 0: Number of Bytes Utilized by Module Manufacturer

This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Line #	Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
128	128	1	0	0	0	0	0	0	0	80
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 1: Total Number of Bytes in Serial PD Device

This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor.

Line #	Serial Memory	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	2 Bytes	0	0	0	0	0	0	0	1	01
2	4 Bytes	0	0	0	0	0	0	1	0	02
3	8 Bytes	0	0	0	0	0	0	1	1	03
4	16 Bytes	0	0	0	0	0	1	0	0	04
5	32 Bytes	0	0	0	0	0	1	0	1	05
6	64 Bytes	0	0	0	0	0	1	1	0	06
7	128 Bytes	0	0	0	0	0	1	1	1	07
8	256 Bytes	0	0	0	0	1	0	0	0	08
9	512 Bytes	0	0	0	0	1	0	0	1	09
10	1024 Bytes	0	0	0	0	1	0	1	0	0A
11	2048 Bytes	0	0	0	0	1	0	1	1	0B
12	4096 Bytes	0	0	0	0	1	1	0	0	0C
13	8192 Bytes	0	0	0	0	1	1	0	1	0D
14	16384 Bytes	0	0	0	0	1	1	1	0	0E
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
254	-	1	1	1	1	1	1	1	0	FE
255	-	1	1	1	1	1	1	1	1	FF

Byte 2: Memory Type

This byte describes the fundamental memory type (or technology) implemented on the module.

Line #	Fundamental Memory Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Reserved	0	0	0	0	0	0	0	0	00
1	Standard FPM DRAM	0	0	0	0	0	0	0	1	01
2	EDO	0	0	0	0	0	0	1	0	02
3	Pipelined Nibble	0	0	0	0	0	0	1	1	03
4	SDRAM	0	0	0	0	0	1	0	0	04
5	ROM	0	0	0	0	0	1	0	1	05
6	DDR SGRAM	0	0	0	0	0	1	1	0	06
7	DDR SDRAM	0	0	0	0	0	1	1	1	07
8	DDR2 SDRAM	0	0	0	0	1	0	0	0	08
-	-	-	-	-	-	-	-	-	-	-
253	TBD	1	1	1	1	1	1	0	1	FD
254	TBD	1	1	1	1	1	1	1	0	FE
255	TBD	1	1	1	1	1	1	1	1	FF

Byte 3: Number of Row Addresses

This field describes the Row addressing on the module. bits 0-4 are used to represent the number of row addresses, bits 5-7 are reserved and must be coded as '0'.

Examples of Byte 3 implementation include:

Number of Row Addresses	Module Organization	Device Used	Byte 3 Contents
13, RA0-RA12	32M x 64	32M x 16	0000 1101
14, RA0-RA13	64M x 64	64M x 8	0000 1110
16, RA0-RA15	512M x 64	512M x 8	0001 0000

Line #	Number of Row Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
7	7	0	0	0	0	0	1	1	1	07
8	8	0	0	0	0	1	0	0	0	08
9	9	0	0	0	0	1	0	0	1	09
10	10	0	0	0	0	1	0	1	0	0A
11	11	0	0	0	0	1	0	1	1	0B
12	12	0	0	0	0	1	1	0	0	0C
13	13	0	0	0	0	1	1	0	1	0D
14	14	0	0	0	0	1	1	1	0	0E
15	15	0	0	0	0	1	1	1	1	0F
16	16	0	0	0	1	0	0	0	0	10
-	-	-	-	-	-	-	-	-	-	-
31	31	0	0	0	1	1	1	1	1	1F
32	Undefined	0	0	1	0	0	0	0	0	20
-	-	-	-	-	-	-	-	-	-	-
255	Undefined	1	1	1	1	1	1	1	1	FF

Byte 4: Number of Column Addresses

This field describes the Column addressing on the module. bit 0-3 are used to represent the number of column addresses, bit 4-7 are reserved and should be coded as '0'

For example:

Number of Column Addresses	Module Organization	Device Used	Byte 4 Contents
10, CA0-CA9	32M x 64	32M x 16	0000 1010
10, CA0-CA9	64M x 64	64M x 8	0000 1010

Line #	Number of Column Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
7	7	0	0	0	0	0	1	1	1	07
8	8	0	0	0	0	1	0	0	0	08
9	9	0	0	0	0	1	0	0	1	09
10	10	0	0	0	0	1	0	1	0	0A
11	11	0	0	0	0	1	0	1	1	0B
12	12	0	0	0	0	1	1	0	0	0C
13	13	0	0	0	0	1	1	0	1	0D
14	14	0	0	0	0	1	1	1	0	0E
15	15	0	0	0	0	1	1	1	1	0F
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 5: Module Attributes - Number of Ranks, Package and Height

This field describes the number of ranks (Rank: any DRAMs connected to same physical $\overline{CS}$) and package on the SDRAM module, and module height. The number of logical banks for the SDRAM device is defined in Byte 17.

Bit 7 ~ Bit 5	Bit 4	Bit 3	Bit 2 ~ Bit 0
Module Height	DRAM Package	Card on Card	# of Ranks
Bit[7, 6, 5] 000 = less than 25.4 mm 001 = 25.4 mm 010 = greater than 25.4 mm and less than 30 mm 011 = 30.0 mm 100 = 30.5 mm 101 = greater than 30.5 mm	1 = stack 0 = planar	1 = yes 0 = no	Bit [2, 1, 0] : 000 = 1 rank 001 = 2 ranks 010 = 3 ranks 011 = 4 ranks 111 = 8 ranks

Byte 6: Module Data Width

Byte 6 is used to designate the module's data width. For example:

Line #	Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Not defined	0	0	0	0	0	0	0	0	0	00
-	-	-	-	-	-	-	-	-	-	-
32	32	0	0	1	0	0	0	0	0	20
33	33	0	0	1	0	0	0	0	1	21
-	-	-	-	-	-	-	-	-	-	-
36	36	0	0	1	0	0	1	0	0	24
-	-	-	-	-	-	-	-	-	-	-
64	64	0	1	0	0	0	0	0	0	40
-	-	-	-	-	-	-	-	-	-	-
72	72	0	1	0	0	1	0	0	0	48
-	-	-	-	-	-	-	-	-	-	-
80	80	0	1	0	1	0	0	0	0	50
-	-	-	-	-	-	-	-	-	-	-
128	128	1	0	0	0	0	0	0	0	80
-	-	-	-	-	-	-	-	-	-	-
144	144	1	0	0	1	0	0	0	0	90
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 7: Reserved

Byte 8: Voltage Interface Level of this assembly

This field describes the module's voltage interface.

Line #	Interface Levels	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	TTL/5 V tolerant	0	0	0	0	0	0	0	0	00
1	LVTTL (not 5 V tolerant)	0	0	0	0	0	0	0	1	01
2	HSTL 1.5 V	0	0	0	0	0	0	1	0	02
3	SSTL 3.3 V	0	0	0	0	0	0	1	1	03
4	SSTL 2.5 V	0	0	0	0	0	1	0	0	04
5	SSTL 1.8 V	0	0	0	0	0	1	0	1	05
6	TBD	0	0	0	0	0	1	1	0	06
-	-	-	-	-	-	-	-	-	-	-

Byte 9: SDRAM Cycle Time

This byte defines the minimum cycle time for the SDRAM module at the highest $\overline{\text{CAS}}$ Latency, $\overline{\text{CAS}}$ Latency=X, defined in byte 18. If other $\overline{\text{CAS}}$ latencies are supported, then the associated minimum cycle times are not related in this version of the SPD standard. Byte 9, Cycle time for CAS Latency=X, is split into two nibbles: the higher order nibble (bits 4-7) designates the cycle time to a granularity of 1 ns; the value presented by the lower order nibble (bits 0-3) has a granularity of 0.1 ns and is added to the value designated by the higher nibble. In addition, four lines of the lower order nibble are assigned to support +0.25, +0.33, +0.66 and +0.75. To indicate cycle time of 1.875 ns, 18h should be programmed. For example:

If bits 7:4 are	and bits 3:0 are	then the total time is:
0011	1101	
(3 ns)	+ (0.75 ns)	= 3.75 ns

Byte 9, SDRAM Cycle Time, Subfield A: Whole Nanoseconds (Bits 4-7)										
Line #	Cycle Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0A	Undefined	0	0	0	0	See Subfield Table B				0
1A	1 ns	0	0	0	1					1
2A	2 ns	0	0	1	0					2
3A	3 ns	0	0	1	1					3
4A	4 ns	0	1	0	0					4
5A	5 ns	0	1	0	1					5
6A	6 ns	0	1	1	0					6
7A	7 ns	0	1	1	1					7
8A	8 ns	1	0	0	0					8
9A	9 ns	1	0	0	1					9
10A	10 ns	1	0	1	0					A
11A	11 ns	1	0	1	1					B
12A	12 ns	1	1	0	0					C
13A	13 ns	1	1	0	1					D
14A	14 ns	1	1	1	0					E
15A	15 ns	1	1	1	1					F
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 9, SDRAM Cycle Time Subfield B: Tenths of Nanoseconds (Bits 0-3)										
Line #	Cycle Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0B	+0 ns	See Subfield Table B				0	0	0	0	0
1B	+0.1 ns					0	0	0	1	1
2B	+0.2 ns					0	0	1	0	2
3B	+0.3 ns					0	0	1	1	3
4B	+0.4 ns					0	1	0	0	4
5B	+0.5 ns					0	1	0	1	5
6B	+0.6 ns					0	1	1	0	6
7B	+0.7 ns					0	1	1	1	7
8B	+0.8 ns					1	0	0	0	8
9B	+0.9 ns					1	0	0	1	9
10B	+0.25 ns					1	0	1	0	A
11B	+0.33 ns					1	0	1	1	B
12B	+0.66 ns					1	1	0	0	C
13B	+0.75 ns					1	1	0	1	D
-	-	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 10: SDRAM Access from Clock (t_{AC})

This byte defines the maximum clock to data out for the SDRAM module. This is the Clock to data out specification at the highest given CAS Latency specified in byte 18 of this SPD specification. If other CAS latencies are supported, then the associated Maximum Clock Access times are not related in this version of the SPD standard. The byte is split into two nibbles: the higher order nibble (bits 4-7) designate the access time to a granularity of 0.1 ns; the value presented by the lower order nibble (bits 0-3) has the granularity of 0.01 ns and is added to the value designated by the higher nibble. For example:

if bits 7:4 are	and bits 3:0 are	then the total time is:
0011	0101	
(0.3 ns)	+ (0.05 ns)	= 0.35 ns

Byte 10: SDRAM Access from Clock, Subfield A: Tenths of Nanoseconds (Bits 4-7)										
Line #	Access from Clock	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0A	Undefined	0	0	0	0	See Subfield B				0
1A	0.1 ns	0	0	0	1					1
2A	0.2 ns	0	0	1	0					2
3A	0.3 ns	0	0	1	1					3
4A	0.4 ns	0	1	0	0					4
5A	0.5 ns	0	1	0	1					5
6A	0.6 ns	0	1	1	0					6
7A	0.7 ns	0	1	1	1					7
8A	0.8 ns	1	0	0	0					8
9A	0.9 ns	1	0	0	1					9
10A	RFU	1	0	1	0					A
11A	-	1	0	1	1					-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 10: SDRAM Access from Clock Subfield B: Hundredths of Nanoseconds (Bits 0-3)										
Line #	Access from Clock	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0B	+0 ns	See Subfield A				0	0	0	0	0
1B	+0.01 ns					0	0	0	1	1
2B	+0.02 ns					0	0	1	0	2
3B	+0.03 ns					0	0	1	1	3
4B	+0.04 ns					0	1	0	0	4
5B	+0.05 ns					0	1	0	1	5
6B	+0.06 ns					0	1	1	0	6
7B	+0.07 ns					0	1	1	1	7
8B	+0.08 ns					1	0	0	0	8
9B	+0.09 ns					1	0	0	1	9
10B	RFU					1	0	1	0	A
11B	-	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 11: DIMM Configuration Type

This byte describes the module's error detection and/or correction schemes on the data, address and command buses.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	TBD	TBD	TBD	Address/Command Parity	Data ECC	Data Parity
0	0	0	0	0	1 or 0	1 or 0	1 or 0

1 = Supported on this assembly, 0 = Not supported on this assembly.
Note: Data ECC includes Data Parity, therefore modules with Data ECC shall encode bit 1 as 1 and bit 0 as 0.

Byte 12: Refresh Rate

This byte describes the module's refresh rate in microseconds.

Line #	Refresh Period	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Normal (15.625 μ s)	1	0	0	0	0	0	0	0	80
1	Reduced (.25x)...3.9 μ s	1	0	0	0	0	0	0	1	81
2	Reduced (.5x)...7.8 μ s	1	0	0	0	0	0	1	0	82
3	Extended (2x)...31.3 μ s	1	0	0	0	0	0	1	1	83
4	Extended (4x)...62.5 μ s	1	0	0	0	0	1	0	0	84
5	Extended (8x)...125 μ s	1	0	0	0	0	1	0	1	85
6	TBD	1	0	0	0	0	1	1	0	86
7	TBD	1	0	0	0	0	1	1	1	87
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-

Byte 13: Primary SDRAM Width

Bits 0-7 of this byte indicate the width of the primary data SDRAM. The primary SDRAM is that which is used for data; examples of primary (data) SDRAM widths are x4, x8, x16, and x32. Note that if the module is made with SDRAMs which provide for data and error checking, e.g. x9, x18, and x36, then it is also designated in this field.

This table contains examples of SDRAM DIMM

Module Width	Primary SDRAM Width	Error Checking SDRAM Width	Byte 13 Contents
x72	x8	x8	0000 1000
x72	x16	x16	0001 0000

Line #	SDRAM Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
7	7	0	0	0	0	0	1	1	1	07
8	8	0	0	0	0	1	0	0	0	08
9	9	0	0	0	0	1	0	0	1	09
10	10	0	0	0	0	1	0	1	0	0A
11	11	0	0	0	0	1	0	1	1	0B
12	12	0	0	0	0	1	1	0	0	0C
13	13	0	0	0	0	1	1	0	1	0D
14	14	0	0	0	0	1	1	1	0	0E
15	15	0	0	0	0	1	1	1	1	0F
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 14: Error Checking SDRAM Width

If the module incorporates error checking and if the primary data SDRAM does not include these bits — i.e. there are separate error checking SDRAMs — then the error checking SDRAM's width is expressed in this byte. Bits 0-7 of this byte relate the error checking SDRAM's width.

The following table contains examples of error checking SDRAM widths

Module Width	Primary SDRAM Width	Error Checking SDRAM Width	Possible (512Mb based) Module Density	Byte 14 Contents
x72	x8	x8	512 MB	0000 1000
x72	x16	x16	256 MB	0001 0000

Line #	Error Checking SDRAM Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
7	7	0	0	0	0	0	1	1	1	07
8	8	0	0	0	0	1	0	0	0	08
9	9	0	0	0	0	1	0	0	1	09
10	10	0	0	0	0	1	0	1	0	0A
11	11	0	0	0	0	1	0	1	1	0B
12	12	0	0	0	0	1	1	0	0	0C
13	13	0	0	0	0	1	1	0	1	0D
14	14	0	0	0	0	1	1	1	0	0E
15	15	0	0	0	0	1	1	1	1	0F
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 15: Reserved

Byte 16: SDRAM Device Attributes – Burst Lengths Supported

This byte describes which various programmable burst lengths are supported by the devices on the module. If the bit is “1”, then that Burst Length is supported on the module; if the bit is “0”, then that Burst Length is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	TBD	TBD	Burst Length = 8	Burst Length = 4	TBD	TBD
0	0	0	0	1 or 0	1 or 0	0	0
1 = Supported on this assembly, 0 = Not supported on this assembly.							

Byte 17: SDRAM Device Attributes – Number of Banks on SDRAM Device

This byte details how many banks are on each SDRAM installed onto the module.

Line #	Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
4	4	0	0	0	0	0	1	0	0	04
-	-	-	-	-	-	-	-	-	-	-
8	8	0	0	0	0	1	0	0	0	08
-	-	-	-	-	-	-	-	-	-	-
255	255	1	1	1	1	1	1	1	1	FF

Byte 18: SDRAM Device Attributes – $\overline{\text{CAS}}$ Latency

This byte describes which of the programmable $\overline{\text{CAS}}$ latencies are acceptable for the module. If the bit is “1”, then that $\overline{\text{CAS}}$ latency is supported on the module; if the bit is “0”, then that $\overline{\text{CAS}}$ latency is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{\text{CAS}}$ Latency = 7	$\overline{\text{CAS}}$ Latency = 6	$\overline{\text{CAS}}$ Latency = 5	$\overline{\text{CAS}}$ Latency = 4	$\overline{\text{CAS}}$ Latency = 3	$\overline{\text{CAS}}$ Latency = 2	TBD	TBD
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	0	0
1 = Supported on this assembly; 0 = Not supported on this assembly.							

Byte 19: DIMM Mechanical Characteristics

This byte identifies the DDR2 SDRAM memory module mechanical information. Each memory module type as specified in Byte 20 defines a unique encoding of thickness ranges in Byte 19. Module thickness is the maximum value including all finished assembly parts: devices, heat spreaders, or other mechanical components.

Type	Reserved					Module Thickness		
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined / Not Specified	Reserved					0	0	0
Thickness (See Indexed Tables below)						x	x	x

Decoding of the module thickness field, based on module type:

Module Thickness			RDIMM	UDIMM	SO-DIMM	Micro-DIMM	Mini-RDIMM	Mini-UDIMM	Unit
Bit 2	Bit 1	Bit 0	Byte 20 = 01 hex	Byte 20 = 02 hex	Byte 20 = 04 hex	Byte 20 = 08 hex	Byte 20 = 10 hex	Byte 20 = 20 hex	
0	0	0	Undefined / Not specified						mm
0	0	1	$x \leq 4.10$	$x \leq 4.10$	$x \leq 3.80$	$x \leq 3.80$	$x \leq 3.85$	$x \leq 3.85$	mm
0	1	0	$4.10 < x \leq 6.75$	$4.10 < x \leq 6.75$	$3.80 < x \leq \text{TBD}$	$3.80 < x \leq \text{TBD}$	$3.85 < x \leq 6.45$	$3.85 < x \leq 6.45$	mm
0	1	1	$6.75 < x \leq 7.55$	$6.75 < x \leq 7.55$	$\text{TBD} < x \leq \text{TBD}$	$\text{TBD} < x \leq \text{TBD}$	$6.45 < x \leq 7.25$	$6.45 < x \leq 7.25$	mm
1	0	0	$7.55 < x$	$7.55 < x$	$\text{TBD} < x$	$\text{TBD} < x$	$7.25 < x$	$7.25 < x$	mm
1	0	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	mm
1	1	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	mm
1	1	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	mm

Module Thickness			72b-SO-RDIMM	72b-SO-CDIMM	Unit
Bit 2	Bit 1	Bit 0	Byte 20 = 07 hex	Byte 20 = 06 hex	
0	0	0	Undefined / Not specified		mm
0	0	1	$x \leq 3.80$	$x \leq 3.80$	mm
0	1	0	$3.80 < x \leq 7.10$	$3.80 < x \leq 7.10$	mm
0	1	1	$7.10 < x$	$7.10 < x$	mm
1	0	0	Reserved	Reserved	mm
1	0	1	Reserved	Reserved	mm
1	1	0	Reserved	Reserved	mm
1	1	1	Reserved	Reserved	mm

Byte 20: DIMM type information

This byte identifies the DDR2 SDRAM memory module type. Each module type specified in Byte 20 defines a unique index for module thicknesses specified in Byte 19, which may be used in conjunction with thermal specifications in Bytes 21 and 47 - 61 to adjust system operating conditions based on installed modules.

Type	Reserved		Module Type						Hex
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Undefined / Not specified	Reserved		0	0	0	0	0	0	00
RDIMM (width = 133.35 mm nom)			0	0	0	0	0	1	01
UDIMM (width = 133.35 mm nom)			0	0	0	0	1	0	02
SO-DIMM (width = 67.60 mm nom)			0	0	0	1	0	0	04
72b-SO-CDIMM (width = 67.60 mm nom)			0	0	0	1	1	0	06
72b-SO-RDIMM (width = 67.60 mm nom)			0	0	0	1	1	1	07
Micro-DIMM (width = 54.00 mm nom)			0	0	1	0	0	0	08
Mini-RDIMM (width = 82.00 mm nom)			0	1	0	0	0	0	10
Mini-UDIMM (width = 82.00 mm nom)			1	0	0	0	0	0	20
Reserved		All other encodings of bits 0:5							

Definitions:

RDIMM: Registered Dual In-Line Memory Module
 UDIMM: Unbuffered Dual In-Line Memory Module
 SO-DIMM: Small Outline Dual In-Line Memory Module
 72b-SO-CDIMM: Clocked SO-DIMM with 72-bit data bus
 72b-SO-RDIMM: Registered SO-DIMM with 72-bit data bus
 Micro-DIMM: Micro Dual In-Line Memory Module
 Mini-RDIMM: Mini Registered Dual In-Line Memory Module
 Mini-UDIMM: Mini Unbuffered Dual In-Line Memory Module