

4.1.2 Serial Presence Detect (SPD), General Standard

Release Version 7R10

Introduction

New memory technologies are continually being introduced to the industry. As these new technologies are considered, the need for expansion modules becomes evident; consequently, new memory technologies are being incorporated onto existing module form factors. Unfortunately, upon a module's first implementation, the module designer is often unable to predict all of the (as yet unreleased) memory technologies which would eventually be used on the module form factor; hence the parallel Presence Detect method did not allow for these newer technologies. Given that memory modules do not regularly change form factor when a new memory technology is implemented, a Serial Presence Detect (SPD) method should be available and predefined so that it can be considered for new memory modules when needed.

1 Scope

This standard defines the means to implement a Presence Detect (PD) scheme serially. This Serial Presence Detect (SPD) standard is intended for use on any memory module, independent of memory technology or module form factor. At the point of standardization of any given memory module, SPD being defined within this standard, may be easily implemented if so chosen. The body of this standard will depict generally how SPD is implemented; this will be independent of the module's memory technology.

When a specific memory technology is being depicted (e.g., Fast Page Mode DRAM), an annex to this standard will be added describing the characteristics, features, and attributes of that memory technology needed for Presence Detection. The entire address map of the SPD scheme must be presented in each annex.

When a new module form factor implementing SPD is standardized, the (proposed) standard for that module must also include the following information pertinent to the SPD:

- SPD Interface protocol (see 2, herein),
- Acceptable module configurations,
- Legitimate architectures: depth, width, #banks, addressing,
- Acceptable error checking schemes (ECC, Parity...),
- SPD wiring diagram and pinout to module.

Note that all writable memory modules that include a Serial Presence Detect (SPD) feature must also support "Page Write" operations of at least 4 sequential addresses.

2 Interface Protocol

Upon the development/standardization of a new module form factor incorporating SPD, the SPD interface protocol will be defined. As long as that module form factor is used, this protocol must remain constant. Examples of SPD interface protocol include I²C, Microwire, etc. The physical implementation (pinouts etc.) must also be defined in the standard for the module form factor if it implements SPD.

The interface standard for the SPD used on all JEDEC memory modules is defined for the following device types:

- EE1002 family of EEPROM devices
- TSE2002 family of EEPROM devices with integrated thermal sensor
- TS3000 family of standalone thermal sensors

Though not technically an SPD device, the TS3000 family of sensors are defined to be compatible with modules using SPD devices. In addition, the TSE2002 family of devices is intended to be a superset of the functionality of EE1002 and TS3000 family devices.

3 Data Order and PD Size

This document will present the order in which the PD bytes should follow. It also defines how many bytes must be used to define a given PD; in most cases it will be one byte per PD. The SPD address map is fixed upon selection of any given fundamental technology, this includes all required and optional data; when a fundamental memory technology's PD bits are defined, then the entire address map for those SPDs must also be defined.

4 SPD Data Types

SPD data is stored in a non-volatile serial memory device. The different types of data include, but are not limited to:

- Look Up Table entries
- Binary data
- Optional data (Binary, ASCII, etc.)
- Checksums or Cyclic Redundancy Checks

4.1 Look Up Table (LUT) Entries

Much of the SPD data is organized as a series of table entries. Each table entry contains one or more bytes of information. Each table entry represents one particular characteristic pertinent to the memory module; e.g., fast page mode DRAM will have specific tables for tRAC, tCAC, number of banks, number of row addresses, number of column addresses, error detection/correction, refresh rates, data width, and interface standard. Each table entry corresponds to a position on a lookup table specified within an annex of this standard. The number of bytes (one or more) needed to express a particular aspect of the module is fixed and defined in this standard or in one of its annexes.

4.2 Optional Data

The current JEDEC Standard allows for manufacturers to insert some of their own specific data into the SPD EEROM. This data includes manufacturer ID, manufacturers' module serial numbers, and other ASCII, Binary Coded Decimal, or binary data.

4.3 Checksums and Cyclic Redundancy Checks

In various cases, checksums are required. This procedure applies to all situations where a Checksum is required. Checksum calculation method is as follows:

1. Convert binary information in byte locations 0 to 62 to decimal.
2. Sum all decimal values for locations 0 to 62.
3. Divide "sum" by 256.
4. Convert remainder to binary (will be less than 256).
5. Store result (single byte) in location 63 as 'Checksum'.

Note that the same result can be obtained by summing the binary values in locations 0 to 62, and eliminating all but the low order byte. The low order byte would be the 'checksum'.

4.3 Checksums and Cyclic Redundancy Checks (Cont'd)

Example

SPD Byte Address	Serial PD		Convert to Decimal	
0	0010 0100	=>	36	
1	1111 1110	=>	254	
2	0000 0000	=>	0	
3	0000 0000	=>	0	
-	-	-	-	
-	-	-	-	
-	-	-	-	
59	0000 0000	=>	0	
60	0000 0000	=>	0	
61	0000 0000	=>	0	
62	0000 0000	=>	0	
			290	(Sum of all decimal values)
			290/256	(Divide by 256) = 1, with a remainder of 34
			34	(Keep remainder)
			0010 0010	(Convert remainder to binary)
63	0010 0010			Store checksum in address location #63

4.3 Checksums and Cyclic Redundancy Checks (Cont'd)

Newer SPDs use a more robust Cyclic Redundancy Check (CRC) algorithm for validating the contents of the SPD EEPROM. The polynomial calculated with this algorithm is $x^{16} + x^{12} + x^5 + 1$. The following algorithm is an example of how to code this polynomial.

```
int Crc16 (char *ptr, int count)
{
    int crc, i;

    crc = 0;
    while (--count >= 0) {
        crc = crc ^ (int)*ptr++ << 8;
        for (i = 0; i < 8; ++i)
            if (crc & 0x8000)
                crc = crc << 1 ^ 0x1021;
            else
                crc = crc << 1;
    }
    return (crc & 0xFFFF);
}

char spdBytes[] = { SPD_byte_0, SPD_byte_1, ..., SPD_byte_N-1 };
int data16;

data16 = Crc16 (spdBytes, sizeof(spdBytes));
SPD_byte_126 = (char) (data16 & 0xFF);
SPD_byte_127 = (char) (data16 >> 8);
```

5 SPD Content, Legacy and Modern Definitions

The legacy SPD definition was traditionally used for memory and module types. As space on the SPD EEPROM ran out, redefinitions of the SPD layout arose for use in subsequent memory and module types. Table 1 summarizes the type of SPD encoding used for various memory types.

Table 1 — Legacy and Modern Definitions

Fundamental Memory Type	SPD Encoding
Fast Page Mode (FPM)	Legacy
Extended Data Out (EDO)	Legacy
SDRAM	Legacy
DDR1 SDRAM	Legacy
DDR2 SDRAM except for FB-DIMM	Legacy
DDR2 FB-DIMM	DDR2 FB-DIMM
DDR3 SDRAM	DDR3 SDRAM

Among all the SPD definitions, Byte 2 (Fundamental Memory Type) is the common Key Byte that is used to differentiate the SPD encoding type.

6 SPD Content, Legacy SPD Definition

The Serial Presence Detect standard calls for various features and items to be defined. Specifically, the definitions listed in Table 2 must be addressed in any SPD implementation.

Table 2 — Legacy SPD Definition

Description	Data Type	Address Map Byte #
SPD size	LUT Entry	0
Total SPD memory size	LUT Entry	1
Fundamental memory type	LUT Entry, Annex A	2
Definition of features specific to the fundamental memory	See pertinent annex	3-XX
(Optional) Superset memory type	See Annex B	XX-60
(Optional) definition of features specific to the superset memory	See pertinent annex	33-61
SPD Revision designator	LUT	62
Checksum for bytes 0-62	Checksum	63
Manufacturer's Jedec ID code per JEP-106	LUT	64-71
Manufacturing location	Supplier Unique	72
Manufacturer's Part Number	Supplier Unique	73-90
Revision Code	Supplier Unique	91-92
Manufacturing date	BCD	93-94
Assembly Serial Number	Supplier Unique	95-98
Manufacturer Specific Data	Supplier Unique	99-125
Reserved	N/A	126-127
Open free-form area	Application Specific	128-255