

4.1.2.4 – Appendix D, Rev. 1.0 : SPD's for DDR SDRAM

1.0 Introduction

This Appendix D, Rev. 1.0 describes the second release of Serial Presence Detect used on Double Data Rate Synchronous DRAM Modules where the SPD revision byte encoding is 10h compared to revision 0.0 SPDs. All bytes except Byte 22, 31, 41 ~ 45, 47, and 62 are encoded identically with the equivalent bytes in the first original release of Appendix D0.0, SPD Revision 0.0 for DDR SDRAMs. Byte 31 added a code to accomodate 4 GB and Byte 62 is changed to follow new SPD revision method. Byte 41 ~ 45 and 47 are added.

All unused entries will be coded as 00h. All unused bits in defined bytes will be coded as 0 except where noted.

These PD's are those referenced in the SPD standard document for "Specific Features". The following SPD fields will occur in the order presented 1.1. Further descriptions of Bytes 0 and 1 are found in the SPD standard. Further description of Byte2 is found in appendix A of the SPD standard

1.1 Address map

The following is the SPD address map for DDR SDRAM. It describes where the individual LUT-entries will be held in the serial EEPROM.

Byte Number	Function Described	Notes
0	Number of Serial PD Bytes written during module production	1
1	Total number of Bytes in Serial PD device	2
2	Fundamental Memory Type (FPM, EDO, SDRAM ...)	
3	Number of Row Addresses on this assembly	
4	Number of Column Addresses on this assembly	
5	Number of DIMM Banks	
6-7	Data Width of this assembly	
8	Voltage Interface Level of this assembly	
9	SDRAM Cycle time at Maximum Supported $\overline{\text{CAS}}$ Latency (CL), CL=X	3
10	SDRAM Access from Clock	
11	DIMM configuration type (Non-parity, Parity or ECC)	
12	Refresh Rate/Type	3, 4
13	Primary SDRAM Width	
14	Error Checking SDRAM Width	
15	SDRAM Device Attributes: Minimum Clock Delay, Back-to-Back Random Column Access	
16	SDRAM Device Attributes: Burst Lengths Supported	
17	SDRAM Device Attributes: Number of Banks on SDRAM Device	3
18	SDRAM Device Attributes: $\overline{\text{CAS}}$ Latency	3
19	SDRAM Device Attributes: $\overline{\text{CS}}$ Latency	3
20	SDRAM Device Attributes: Write Latency	3
21	SDRAM Module Attributes	
22	SDRAM Device Attributes: General	3, 5
23	Minimum Clock Cycle at CL = X - 0.5	3
24	Maximum Data Access Time (t_{AC}) from Clock at CL = X - 0.5	3
25	Minimum Clock Cycle at CL = X - 1	3
26	Maximum Data Access Time (t_{AC}) from Clock at CL = X - 1	3
27	Minimum Row Precharge Time (t_{RP})	3
28	Minimum Row Active to Row Active delay (t_{RRD})	3
29	Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay (t_{RCD})	3
30	Minimum Active to Precharge Time (t_{RAS})	3

Byte Number	Function Described	Notes
31	Module Bank Density	5
32	Address and Command Input Setup Time Before Clock	
33	Address and Command Input Hold Time After Clock	
34	Data Input Setup Time Before Clock	
35	Data Input Hold Time After Clock	
36-40	Superset Information (may be used in the future)	
41	SDRAM Device Minimum Active to Active/Auto Refresh Time (tRC)	5
42	SDRAM Device Minimum Auto Refresh to Active/Auto Refresh (tRFC)	5
43	SDRAM Device Maximum device cycle time (tCKmax)	5
44	SDRAM Device Maximum skew between DQS and DQ signals (tDQSQ)	5
45	DDR SDRAM Device Maximum Read Data Hold Skew Factor (tQHS)	5
46	Reserved for future use	
47	SDRAM Device Attributes - DDR SDRAM DIMM Height	5
48 ~ 61	Reserved for future use	
62	SPD Revision	5
63	Checksum for Bytes 0-62	
64-71	Manufacturer's JEDEC ID Code	
72	Module Manufacturing Location	
73-90	Module Part Number	
91-92	Module Revision Code	
93-94	Module Manufacturing Date	
95-98	Module Serial Number	
99-127	Manufacturer's Specific Data	
128-255	Open for customer use	
1. This will typically be programmed as 128 Bytes. 2. This will typically be programmed as 256 Bytes. 3. From Datasheet. 4. High order bit is Self Refresh "flag". If set to "1", the assembly supports self refresh. 5. Changed or added since the first original release of DDR SPD revision 0.0		

2.0 Details of each byte

Byte 0: Number of Bytes Utilized by Module Manufacturer

This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Line #	Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
128	128	1	0	0	0	0	0	0	0	80
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 1: Total Number of Bytes in Serial PD Device

This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor.

Line #	Serial Memory	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	2 Bytes	0	0	0	0	0	0	0	1	01
2	4 Bytes	0	0	0	0	0	0	1	0	02
3	8 Bytes	0	0	0	0	0	0	1	1	03
4	16 Bytes	0	0	0	0	0	1	0	0	04
5	32 Bytes	0	0	0	0	0	1	0	1	05
6	64 Bytes	0	0	0	0	0	1	1	0	06
7	128 Bytes	0	0	0	0	0	1	1	1	07
8	256 Bytes	0	0	0	0	1	0	0	0	08
9	512 Bytes	0	0	0	0	1	0	0	1	09
10	1024 Bytes	0	0	0	0	1	0	1	0	0A
11	2048 Bytes	0	0	0	0	1	0	1	1	0B
12	4096 Bytes	0	0	0	0	1	1	0	0	0C
13	8192 Bytes	0	0	0	0	1	1	0	1	0D
14	16384 Bytes	0	0	0	0	1	1	1	0	0E
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
254	-	1	1	1	1	1	1	1	0	FE
255	-	1	1	1	1	1	1	1	1	FF

Byte 2: Memory Type

This byte describes the fundamental memory type (or technology) implemented on the module.

Line #	Fundamental Memory Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Reserved	0	0	0	0	0	0	0	0	00
1	Standard FPM DRAM	0	0	0	0	0	0	0	1	01
2	EDO	0	0	0	0	0	0	1	0	02
3	Pipelined Nibble	0	0	0	0	0	0	1	1	03
4	SDRAM	0	0	0	0	0	1	0	0	04
5	ROM	0	0	0	0	0	1	0	1	05
6	SGRAM DDR	0	0	0	0	0	1	1	0	06
7	SDRAM DDR	0	0	0	0	0	1	1	1	07
8	DDR2 SDRAM	0	0	0	0	1	0	0	0	08
-	-	-	-	-	-	-	-	-	-	-
254	TBD	1	1	1	1	1	1	1	0	FE
255	TBD	1	1	1	1	1	1	1	1	FF

Byte 3: Number of Row Addresses

This field describes the Row addressing on the module. If there is one physical bank on the module **or** if there are two physical banks of the same size and organization, then bits 0-3 are used to represent the number of row addresses for each physical bank. If the module has two physical banks of asymmetric size, then bits 0-3 represent the number of row addresses for physical bank 1 and bits 4-7 represent the number of row addresses for physical bank 2 (bank 2 device is 2x bank 1 device width). Note that these do not include the Bank Address pin since physical bank selection of DIMM modules is asserted on dedicated BA (Bank Address) pins.

Examples of Byte 3 implementation include:

Number of Phys Banks	Number of Row Addresses for Physical Bank 1	Number of Row Addresses for Physical Bank 2	Module Organization	Device Used	Byte 3 Contents
1	12, RA0-RA11	N/A	16M x 64	16M x 8	0000 1100
2	12, RA0-RA11	12, RA0-RA11	2 x 16M x 64	16M x 8	0000 1100
2	12, RA0-RA11	12, RA0-RA11	16M x 64 & 8M x 64	16M x 8 & 8M x 16	1100 1100

Byte 3, Subfield A: Number of Row Addresses on physical Bank 1, OR Number of Row Addresses on physical Bank 1 and 2 if both physical banks have the same depth (Bits 0-3)										
Line #	Number of Row Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0A	Undefined	See Subfield B				0	0	0	0	<u>0</u>
1A	1/16					0	0	0	1	<u>1</u>
2A	2/17					0	0	1	0	<u>2</u>
:	:					:	:	:	:	:
7A	7					0	1	1	1	<u>7</u>
8A	8					1	0	0	0	<u>8</u>
9A	9					1	0	0	1	<u>9</u>
10A	10					1	0	1	0	<u>A</u>
11A	11					1	0	1	1	<u>B</u>
12A	12					1	1	0	0	<u>C</u>
13A	13					1	1	0	1	<u>D</u>
14A	14					1	1	1	0	<u>E</u>
15A	15					1	1	1	1	<u>F</u>

Byte 3, Subfield B: Number of Row Addresses on physical Bank 2 if physical banks have different depths (Bits 4-7)										
Line #	Number of Row Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0B	No 2nd Asymmetric Physical Bank	0	0	0	0	See Subfield A				0 <u>_</u>
1B	1/16	0	0	0	1					1 <u>_</u>
2B	2/17	0	0	1	0					2 <u>_</u>
:	:	:	:	:	:					:
7B	7	0	1	1	1					7 <u>_</u>
8B	8	1	0	0	0					8 <u>_</u>
9B	9	1	0	0	1					9 <u>_</u>
10B	10	1	0	1	0					A <u>_</u>
11B	11	1	0	1	1					B <u>_</u>
12B	12	1	1	0	0					C <u>_</u>
13B	13	1	1	0	1					D <u>_</u>
14B	14	1	1	1	0					E <u>_</u>
15B	15	1	1	1	1					F <u>_</u>

Byte 4: Number of Column Addresses

This field describes the Column addressing on the module. If there is one physical bank on the module **or** if there are two physical banks of the same size, then bits 0-3 are used to represent the number of column addresses for each physical bank. If the module has two physical banks of asymmetric size, then bits 0-3 represent the number of column addresses for physical bank 1 and bits 4-7 represent the number of column addresses for physical bank 2 (bank 2 device is 2x bank 1 device width). For example:

Number of Phys Banks	Number of Column Addresses for Physical Bank 1	Number of Column Addresses for Physical Bank 2	Module Organization	Device Used	Byte 4 Contents
1	10, CA0-CA9	N/A	16M x 64	16M x 8	0000 1010
2	10, CA0-CA9	10, CA0-CA9	2 x 16M x 64	16M x 8	0000 1010
2	10, CA0-CA9	9, CA0-CA8	16M x 64 & 8M x 64	16M x 8 & 8M x 16	1010 1001

Byte 4, Subfield A: Number of Column Addresses on physical Bank 1, OR Number of Column Addresses on physical Bank 1 and 2 if both physical banks have the same depth (Bits 0-3)										
Line Number	Number of Column Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0A	Undefined	See Subfield B				0	0	0	0	_0
1A	1/16					0	0	0	1	_1
2A	2/17					0	0	1	0	_2
:	:					:	:	:	:	:
7A	7					0	1	1	1	_7
8A	8					1	0	0	0	_8
9A	9					1	0	0	1	_9
10A	10					1	0	1	0	_A
11A	11					1	0	1	1	_B
12A	12					1	1	0	0	_C
13A	13					1	1	0	1	_D
14A	14					1	1	1	0	_E
15A	15					1	1	1	1	_F

Byte 4, Subfield B: Number of Column Addresses on physical Bank 2 if physical banks have different depths (Bits 4-7)										
Line Number	Number of Column Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0B	No 2nd Asymmetric Physical Bank	0	0	0	0	See Subfield A				0_
1B	1/16	0	0	0	1					1_
2B	2/17	0	0	1	0					2_
:	:	:	:	:	:					:
7B	7	0	1	1	1					7_
8B	8	1	0	0	0					8_
9B	9	1	0	0	1					9_
10B	10	1	0	1	0					A_
11B	11	1	0	1	1					B_
12B	12	1	1	0	0					C_
13B	13	1	1	0	1					D_
14B	14	1	1	1	0					E_
15B	15	1	1	1	1					F_

Byte 5: Number of DIMM Banks

This field describes the number of physical banks on the SDRAM module. The number of logical banks for the SDRAM device is defined in Byte 17.

Line #	Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
7	7	0	0	0	0	0	1	1	1	07
8	8	0	0	0	0	1	0	0	0	08
9	9	0	0	0	0	1	0	0	1	09
10	10	0	0	0	0	1	0	1	0	0A
11	11	0	0	0	0	1	0	1	1	0B
12	12	0	0	0	0	1	1	0	0	0C
13	13	0	0	0	0	1	1	0	1	0D
14	14	0	0	0	0	1	1	1	0	0E
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Bytes 6 and 7: Module Data Width

Bytes 6 and 7 are used to designate the module's data width. The data width is presented as a 16-bit word: bit 0 of byte 6 becomes the LSB of the 16 bit width identifier and bit 7 of byte 7 becomes the MSB. Consequently, if the module has a width of less than 255 bits, byte 7 will be 00h. If the data width is 256 bits or more, byte 7 is used in conjunction with byte 6 to designate the total module width. For example:

If the module's Data Width is:	then Byte 7 is:	and Byte 6 is:
64	0000 0000	0100 0000
72	0000 0000	0100 1000
576	0000 0010	0100 0000

Byte 6: Module Data Width

Line #	Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	0	0	0	0	0	0	0	0	0	00
-	-	-	-	-	-	-	-	-	-	-
32	32	0	0	1	0	0	0	0	0	20
33	33	0	0	1	0	0	0	0	1	21
-	-	-	-	-	-	-	-	-	-	-
36	36	0	0	1	0	0	1	0	0	24
-	-	-	-	-	-	-	-	-	-	-
64	64	0	1	0	0	0	0	0	0	40
-	-	-	-	-	-	-	-	-	-	-
72	72	0	1	0	0	1	0	0	0	48
-	-	-	-	-	-	-	-	-	-	-
80	80	0	1	0	1	0	0	0	0	50
-	-	-	-	-	-	-	-	-	-	-
128	128	1	0	0	0	0	0	0	0	80
-	-	-	-	-	-	-	-	-	-	-
144	144	1	0	0	1	0	0	0	0	90
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 7: Module Data Width Continuation

This byte will be left at 00h if the module data width is less than 256 bits wide. If the width is 256 or greater, then this byte will be used in conjunction with byte 6.

Line #	Data Width (cont'd)	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Hex
0	0 (+)	0	0	0	0	0	0	0	0	00
1	256 (+)	0	0	0	0	0	0	0	1	01
2	512 (+)	0	0	0	0	0	0	1	X	02-03
3	1024 (+)	0	0	0	0	0	1	X	X	04-07
4	2048 (+)	0	0	0	0	1	X	X	X	08-15

X = 0 or 1.

Byte 8: Voltage Interface Level of this assembly

This field describes the module's voltage interface.

Line #	Interface Levels	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	TTL/5V tolerant	0	0	0	0	0	0	0	0	00
1	LVTTL (not 5V tolerant)	0	0	0	0	0	0	0	1	01
2	HSTL 1.5V	0	0	0	0	0	0	1	0	02
3	SSTL 3.3V	0	0	0	0	0	0	1	1	03
4	SSTL 2.5V	0	0	0	0	0	1	0	0	04
5	SSTL 1.8V	0	0	0	0	0	1	0	1	05
6	TBD	0	0	0	0	0	1	1	0	06
-	-	-	-	-	-	-	-	-	-	-

Byte 9: DDR SDRAM Cycle Time

This byte defines the minimum cycle time for the SDRAM module at the highest $\overline{\text{CAS}}$ Latency, $\overline{\text{CAS}}$ Latency = X, defined in byte 18. If other $\overline{\text{CAS}}$ latencies are supported, then the associated minimum cycle times are not related in this version of the SPD standard. Byte 9, Cycle time for CAS Latency=X, is split into two nibbles: the higher order nibble (bits 4-7) designates the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0-3) has a granularity of .1ns and is added to the value designated by the higher nibble. For example:

If bits 7:4 are	and bits 3:0 are	then the total time is:
0111	0101	
(7ns)	+ (.5ns)	= 7.5ns

Byte 9, SDRAM Cycle Time, Subfield A: Whole Nanoseconds (Bits 4-7)										
Line #	Cycle Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0A	Undefined	0	0	0	0	See Subfield Table B				0_
1A	1ns	0	0	0	1					1_
2A	2ns	0	0	1	0					2_
3A	3ns	0	0	1	1					3_
4A	4ns	0	1	0	0					4_
5A	5ns	0	1	0	1					5_
6A	6ns	0	1	1	0					6_
7A	7ns	0	1	1	1					7_
8A	8ns	1	0	0	0					8_
9A	9ns	1	0	0	1					9_
10A	10ns	1	0	1	0					A_
11A	11ns	1	0	1	1					B_
12A	12ns	1	1	0	0					C_
13A	13ns	1	1	0	1					D_
14A	14ns	1	1	1	0					E_
15A	15ns	1	1	1	1					F_
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 9, SDRAM Cycle Time Subfield B: Tenths of Nanoseconds (Bits 0-3)										
Line #	Cycle Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0B	+0ns	See Subfield Table B				0	0	0	0	_0
1B	+.1ns					0	0	0	1	_1
2B	+.2ns					0	0	1	0	_2
3B	+.3ns					0	0	1	1	_3
4B	+.4ns					0	1	0	0	_4
5B	+.5ns					0	1	0	1	_5
6B	+.6ns					0	1	1	0	_6
7B	+.7ns					0	1	1	1	_7
8B	+.8ns					1	0	0	0	_8
9B	+.9ns					1	0	0	1	_9
10B	RFU					1	0	1	0	_A
-	-	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 10: SDRAM Access from Clock (t_{AC})

This byte defines the maximum clock to data out for the SDRAM module. This is the Clock to data out specification at the highest given CAS Latency specified in byte 18 of this SPD specification. If other CAS latencies are supported, then the associated Maximum Clock Access times are not related in this version of the SPD standard. The byte is broken into two nibbles: the higher order nibble (bits 4-7) designate the access time to a granularity of 0.1ns; the value presented by the lower order nibble (bits 0-3) has the granularity of .01ns and is added to the value designated by the higher nibble. For example:

if bits 7:4 are	and bits 3:0 are	then the total time is:
0111	0101	
(0.7ns)	+ (0.05ns)	= 0.75ns

Byte 10: SDRAM Access from Clock, Subfield A: Tenths of Nanoseconds (Bits 4-7)

Line #	Access from Clock	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0A	Undefined	0	0	0	0	See Subfield B				0
1A	.1ns	0	0	0	1					1
2A	.2ns	0	0	1	0					2
3A	.3ns	0	0	1	1					3
4A	.4ns	0	1	0	0					4
5A	.5ns	0	1	0	1					5
6A	.6ns	0	1	1	0					6
7A	.7ns	0	1	1	1					7
8A	.8ns	1	0	0	0					8
9A	.9ns	1	0	0	1					9
10A	RFU	1	0	1	0					A
11A	-	1	0	1	1					-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 10: SDRAM Access from Clock Subfield B: Hundredths of Nanoseconds (Bits 0-3)

Line #	Access from Clock	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0B	+0ns	See Subfield A				0	0	0	0	0
1B	+0.01ns					0	0	0	1	1
2B	+0.02ns					0	0	1	0	2
3B	+0.03ns					0	0	1	1	3
4B	+0.04ns					0	1	0	0	4
5B	+0.05ns					0	1	0	1	5
6B	+0.06ns					0	1	1	0	6
7B	+0.07ns					0	1	1	1	7
8B	+0.08ns					1	0	0	0	8
9B	+0.09ns					1	0	0	1	9
10B	RFU					1	0	1	0	A
11B	-	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 11: DIMM Configuration Type

This byte describes the module's error detection and/or correction scheme.

Line #	Error Detection/Correction	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	None	0	0	0	0	0	0	0	0	00
1	Parity	0	0	0	0	0	0	0	1	01
2	ECC	0	0	0	0	0	0	1	0	02
3	TBD	0	0	0	0	0	0	1	1	03
4	TBD	0	0	0	0	0	1	0	0	04
5	TBD	0	0	0	0	0	1	0	1	05
6	TBD	0	0	0	0	0	1	1	0	06
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-

Byte 12: Refresh Rate/Type

This byte describes the module's refresh rate and type.

Line #	Refresh Period	Bit 7 (Self Refresh Flag)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Normal (15.625 us)	0	0	0	0	0	0	0	0	00
1	Reduced (.25x)...3.9us	0	0	0	0	0	0	0	1	01
2	Reduced (.5x)...7.8us	0	0	0	0	0	0	1	0	02
3	Extended (2x)...31.3us	0	0	0	0	0	0	1	1	03
4	Extended (4x)...62.5us	0	0	0	0	0	1	0	0	04
5	Extended (8x)...125us	0	0	0	0	0	1	0	1	05
6	TBD	0	0	0	0	0	1	1	0	06
7	TBD	0	0	0	0	0	1	1	1	07
-	-	-	-	-	-	-	-	-	-	-
Self Refresh Entries										
128	Normal (15.625 us)	1	0	0	0	0	0	0	0	80
129	Reduced (.25x)...3.9us	1	0	0	0	0	0	0	1	81
130	Reduced (.5x)...7.8us	1	0	0	0	0	0	1	0	82
131	Extended (2x)...31.3us	1	0	0	0	0	0	1	1	83
132	Extended (4x)...62.5us	1	0	0	0	0	1	0	0	84
133	Extended (8x)...125us	1	0	0	0	0	1	0	1	85
134	TBD	1	0	0	0	0	1	1	0	86
135	TBD	1	0	0	0	0	1	1	1	87
-	-	-	-	-	-	-	-	-	-	-