

4.1.2.5 - Appendix E: Specific PD's for Synchronous DRAM (SDRAM).

- 1.0 Introduction: This appendix describes the Presence Detects for Synchronous DRAM Modules with SPD revision level 2 (02h). These PD's are those referenced in the SPD standard document for "Specific Features". The following PD fields will occur, in the order presented, in table 1.1. Further descriptions of bytes 0 and 1 are found in the SPD standard. Further description of byte 2 is found in appendix A of the SPD standard. **All unused entries will be coded as 00h or FFh. All unused bits in defined bytes will be coded as 0 except where noted.**
- 1.1 Address map: The following is the SPD address map for SDRAM, which describes where the individual LUT-Entries/bytes will be held in the serial EEPROM:

Byte Number	Function described	Notes
0	Defines # bytes written into serial memory at module mfg	1
1	Total # bytes of SPD memory device	2
2	Fundamental memory type (FPM, EDO, SDRAM...) from appendix A	
3	# Row Addresses on this assembly	3
4	# Column Addresses on this assembly	
5	# Module Banks on this Assembly	
6	Data Width of this assembly...	
7	...Data Width continuation	
8	Voltage interface standard of this assembly	
9	SDRAM Cycle time at Max. Supported CAS Latency (CL), CL=X	4
10	SDRAM Access from Clock at CL=X	4
11	DIMM Configuration type (Non-parity, Parity, ECC)	
12	Refresh Rate/Type	4,5
13	SDRAM width, Primary DRAM	
14	Error Checking SDRAM data width	
15	Minimum Clock Delay, Back to Back Random Column Addresses	
16	Burst Lengths Supported	
17	# Banks on Each SDRAM device	4
18	CAS# Latencies Supported	4
19	CS# Latency	4
20	Write Latency	4
21	SDRAM Module Attributes	
22	SDRAM Device Attributes: General	
23	Minimum Clock Cycle Time at CL X-1	4
24	Maximum Data Access Time from Clock @ CL X-1	4
25	Minimum Clock Cycle Time at CL X-2	4
26	Maximum Data Access Time from Clock @ CL X-2	4
27	Minimum Row Precharge Time	4
28	Minimum Row Active to Row Active delay	4
29	Minimum RAS to CAS delay	4
30	Minimum RAS Pulse Width	4
31	Module Bank Density	
32	Address and Command Setup time before Clock	6
33	Address and Command Hold time after Clock	6
34	Data Input Setup Time before Clock	6
35	Data Input Hold Time after Clock	6
36-40	Reserved for VCSDRAM	
41	Minimum Bank Cycle Time (tRC)	6
42-61	Superset Information (may be used in future)	
62	SPD Revision	
63	Checksum for bytes 0-62	
64-71	Manufacturers JEDEC ID code per JEP-106E	
72	Manufacturing location	
73-90	Manufacturer's Part Number	
91-92	Revision Code	
93	Module Manufacturing Year	
94	Module Manufacturing Week	
95-98	Assembly Serial Number	9
99-125	Manufacturer Specific Data	7
126-127	Vendor Specific	7
128-255	Open for Customer use.	8

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notes:

- 1) This will be programmed as 128 bytes for the 168 pin DIMM Module.
- 3) High order bit defines if assembly has "redundant" addressing (if set to "1", highest order RAS# address must be re-sent as highest order CAS# address.)
- 4) From data sheet.
- 5) High order bit (MSB) is Self Refresh 'flag'. If Bit seven is "1", assembly supports self refresh.
- 6) The JEDEC spec. specifies that these bytes are optional for 66MHz applications. If they are not included then the SPD revision level (byte 62) is set at revision 1 (01h).
- 7) The JEDEC spec specifies that these bytes are optional.
- 8) Module suppliers will need to assure that these bytes are open for reads/writes by Customer.
- 9) Bytes 95-98 must be coded such that bytes 64-72 and 93-98 will result in a unique serial number. .

2.0 For Reference, Bytes 1-3. Descriptions of bytes 1 and 2 can be found in the main body of the SPD standard, and byte 3 is detailed in appendix A to this standard. For reference and convenience, applicable portions of their descriptions are presented again:

2.1 BYTE 0, From General SPD Standard, Number of Bytes used by Module Manufacturer: This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

2.2 Byte 1, From General SPD Standard, Total SPD Memory Size: This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Invalid	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16384 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

- 2.3 Byte 2, From Appendix A, Memory Type: This byte describes the fundamental memory type (or technology) implemented on the module. See Appendix A for the complete list of memory types:

Fundamental Mem. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SDR SDRAM	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.
.DDR SDRAM	0	0	0	0	0	1	1	1

- 3.0 Data Type(s): Even though many of the PD's seem to be binary numbers representing the feature they are describing, they are considered Look Up Table (LUT) entries.

- 4.0 The following PD bytes are those specific to modules implementing Synchronous DRAM technology. Note that these full descriptions start at byte 3 below and are not covered in the main body of the SPD standard since they are specific to a given fundamental memory type/technology

- 4.1 Byte 3, Number of ROW Addresses: This field describes the Row addressing on the module. If there is one physical bank on the module OR if there are two physical banks of the same size and organization, then Bits 0-3 are used to represent the number of row addresses for each physical bank. If the module has two physical banks of asymmetric size, then Bits 0-3 represent the number of row addresses for physical bank 1 and Bits 4-7 represent the number of row addresses for physical bank 2. Note that these do not include the Bank Address pin since physical bank selection on DIMM modules is asserted on dedicated BA (Bank Address) pins. Also note that if the module employs redundant addressing, then it is denoted in Byte 21, Bit 6. Examples of Byte 3 implementation include:

#Banks	# Row Addr Bank 1	# Row Addr Bank2	Module Organization	Discrete Used	Byte 3 Contents
1	11,RA0-RA10	N/A	2Mx64	2Mx8	0000 1011
2	11,RA0-RA10	11,RA0-RA10	2x2Mx64	2Mx8	0000 1011
2	11,RA0-RA10	11,RA0-RA10	2Mx64 & 1Mx64	2Mx8 & 1Mx16	1011 1011

# Row Addr					Table Subfield A: No. of Row addresses on Bank 1 -OR- No. of Row addresses on Bank 1 and 2 if both banks have the same depth, Bits 0-3			
					Bit 3	Bit 2	Bit 1	Bit 0
Undefined	See Subfield B				0	0	0	0
1/16					0	0	0	1
2/17					0	0	1	0
:					:	:	:	:
7					0	1	1	1
8					1	0	0	0
9					1	0	0	1
10					1	0	1	0
11					1	0	1	1
12					1	1	0	0
13					1	1	0	1
14					1	1	1	0
15					1	1	1	1
# Row Addr	Table Subfield B: Number of Row addresses on Bank 2 (if different from bank 1), Bits 4-7				See Subfield A			
	Bit 7	Bit 6	Bit 5	Bit 4				
No 2 nd Asymet- rical bank	0	0	0	0				
1/16	0	0	0	1				
2/17	0	0	1	0				
:	:	:	:	:				
7	0	1	1	1				
8	1	0	0	0				
9	1	0	0	1				
10	1	0	1	0				
11	1	0	1	1				
12	1	1	0	0				
13	1	1	0	1				
14	1	1	1	0				
15	1	1	1	1				

- 4.2 Byte 4, Number of Column Addresses: This field describes the Column addressing on the module. If there is one physical bank on the module OR if there are two physical banks of the same size, then Bits 0-3 are used to represent the number of column addresses for each physical bank. If the module has two physical banks of asymmetric size, then Bits 0-3 represent the number of column addresses for physical bank 1 and Bits 4-7 represent the number of column addresses for physical bank 2. For example:

#Banks	# Col Addr Bank 1	# Col AddrModule Bank2	Discrete Organization	Used	Byte 3 Contents
1	9,CA0-CA8	N/A	2Mx64	2Mx8	0000 1001
2	9,CA0-CA8	9,CA0-CA8	2x2Mx64	2Mx8	0000 1001
2	9,CA0-CA8	8,CA0-CA7	2Mx64 & 1Mx64	2Mx8 & 1Mx16	1000 1001

# Column Addr					Table Subfield A: No. of Column addresses on Bank 1 -OR- No. of Column addresses on Bank 1 and 2 if both banks same depth, Bits 0-3			
					Bit 3	Bit 2	Bit 1	Bit 0
Undefined	See Subfield B				0	0	0	0
1/16					0	0	0	1
2/17					0	0	1	0
:					:	:	:	:
7					0	1	1	1
8					1	0	0	0
9					1	0	0	1
10					1	0	1	0
11					1	0	1	1
12					1	1	0	0
13					1	1	0	1
14					1	1	1	0
15					1	1	1	1
# Column Addr	Table Subfield B: Number of Column addresses on Bank 2 (if different from bank 1), Bits 4-7				See Subfield A			
	Bit 7	Bit 6	Bit 5	Bit 4				
No 2 nd Asymmetrical bank	0	0	0	0				
1/16	0	0	0	1				
2/17	0	0	1	0				
:	:	:	:	:				
7	0	1	1	1				
8	1	0	0	0				
9	1	0	0	1				
10	1	0	1	0				
11	1	0	1	1				
12	1	1	0	0				
13	1	1	0	1				
14	1	1	1	0				
15	1	1	1	1				

- 4.3 Byte 5, Number of Banks on module: This field describes the number of physical banks on the SDRAM Module. This is not to be confused with the number of logical banks on a given SDRAM device which are defined in Byte 17:

Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

- 4.4 Bytes 6 & 7, Module Data Width: Bytes 6 and 7 are used to designate the module's data width. The data width is presented as a 16 bit word; Bit 0 of byte 6 becomes the LSB of the 16 bit width identifier and Bit 7 of byte 7 becomes the MSB. Consequently, if the module has a width of less than 255 Bits wide, byte 7 will be 00h. If the data width is 256 Bits or higher, byte 7 is used in conjunction with byte 6 to designate the total module width. For example, if the module's

data width is: then byte 7 is and byte 6 is:

-----	-----	-----
64	0000 0000	0100 0000
72	0000 0000	0100 1000
80	0000 0000	0101 0000
576	0000 0010	0100 0000

4.4.1 Byte 6:

Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
.	.	.	.	.	.	.	.	.
32	0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.	.
36	0	0	1	0	0	1	0	0
.	.	.	.	.	.	.	.	.
64	0	1	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
72	0	1	0	0	1	0	0	0
.	.	.	.	.	.	.	.	.
80	0	1	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
144	1	0	0	1	0	0	0	0
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

- 4.4.2 Byte 7, Module Data Width Continued: This byte will be left at 00h if the original module data width is less than 256 Bits wide. If the width is more than 255, then this byte will be used in conjunction with byte 6.

Module Data Width Cont.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0(+)	0	0	0	0	0	0	0	0
256(+)	0	0	0	0	0	0	0	1
512(+)	0	0	0	0	0	0	1	X
1024(+)	0	0	0	0	0	1	X	X
2048(+)	0	0	0	0	1	X	X	X
.	.	.	.	.	.	.	.	.

- 4.5 Byte 8, Module Interface Levels: This field describes the module's voltage interface:

Voltage Interface	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5.0 Volt/TTL	0	0	0	0	0	0	0	0
LVTTL	0	0	0	0	0	0	0	1
HSTL 1.5 V	0	0	0	0	0	0	1	0
SSTL 3.3 V	0	0	0	0	0	0	1	1
SSTL 2.5 V	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
.	1	1	1	1	1	1	1	1

- 4.6 Byte 9, SDRAM Cycle time (tCYC): This byte defines the minimum cycle time for the SDRAM Module at the highest CAS Latency, CAS Latency=X, defined in byte 18. If other CAS latencies are supported, then the associated minimum cycle times are not related in this version of the SPD standard. At this time of publication, proposals are being made to widen the standard to relate cycle times at lower CAS Latencies. Byte 9, Cycle time for CAS Latency = X, is split into two nibbles: the higher order nibble (Bits 4 through 7) designate the cycle time to a granularity of 1 ns; the value presented by the lower order nibble (Bits 0 through 3) has a granularity of 1/10 ns and is added to the value designated by the higher nibble. For example, if

Bits 7:4 are 1010 and Bits 3:0 are 0101 then the cycle time is (10 ns) + (0.5 ns) = 10.5 ns

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SDRAM Cycle Time Subfield A: Units of nanoseconds (Bits 4 through 7)								
Undefined	0	0	0	0	SEE Subfield Table B			
1 ns	0	0	0	1				
2 ns	0	0	1	0				
3 ns	0	0	1	1				
4 ns	0	1	0	0				
5 ns	0	1	0	1				
6 ns	0	1	1	0				
7 ns	0	1	1	1				
8 ns	1	0	0	0				
9 ns	1	0	0	1				
10 ns	1	0	1	0				
11 ns	1	0	1	1				
12 ns	1	1	0	0				
13 ns	1	1	0	1				
14 ns	1	1	1	0				
15 ns	1	1	1	1				
SDRAM Cycle Time Subfield B: Tenths of ns (Bits 0 through 3)								
+0 ns	SEE Subfield table A				0	0	0	0
+0.1 ns					0	0	0	1
+0.2 ns					0	0	1	0
+0.3 ns					0	0	1	1
+0.4 ns					0	1	0	0
+0.5 ns					0	1	0	1
+0.6 ns					0	1	1	0
+0.7 ns					0	1	1	1
+0.8 ns					1	0	0	0
+0.9 ns					1	0	0	1
RFU					1	0	1	0
.					.	.	.	.
Undefined	1	1	1	1	1	1	1	1

- 4.7 Byte 10, SDRAM Access time from Clock (tAC): This byte defines the maximum clock to data out for the module. This is the Clock to data out specification at the highest given CAS Latency specified/depicted in byte 18 of this SPD specification/standard. If other CAS latencies are supported, then the associated Maximum Clock Access times are not related in this version of the SPD standard. At this time of publication, proposals are being made to widen the standard to relate tAC's at lower CAS Latencies.

The byte is split into two nibbles: the higher order nibble (Bits 4 through 7) designate the cycle time to a granularity of 1 ns; the value presented by the lower order nibble (Bits 0 through 3) has a granularity of 1/10 ns and is added to the value designated by the higher nibble. For example, if

Bits 7:4 are 1001 and Bits 3:0 are 0000 then the cycle time is
 $(9 \text{ ns}) + (0.0 \text{ ns}) = 9.0 \text{ ns}$

Nanoseconds	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SDRAM Access time from Clock:								
Subfield A: Units of nanoseconds (Bits 4 through 7)								
Undefined	0	0	0	0	SEE Subfield Table B			
1 ns	0	0	0	1				
2 ns	0	0	1	0				
3 ns	0	0	1	1				
4 ns	0	1	0	0				
5 ns	0	1	0	1				
6 ns	0	1	1	0				
7 ns	0	1	1	1				
8 ns	1	0	0	0				
9 ns	1	0	0	1				
10 ns	1	0	1	0				
11 ns	1	0	1	1				
12 ns	1	1	0	0				
13 ns	1	1	0	1				
14 ns	1	1	1	0				
15 ns	1	1	1	1				
SDRAM Access time from CLK								
Subfield B: Tenths of ns (Bits 0 through 3)								
+0 ns	SEE Subfield table A				0	0	0	0
+0.1 ns					0	0	0	1
+0.2 ns					0	0	1	0
+0.3 ns					0	0	1	1
+0.4 ns					0	1	0	0
+0.5 ns					0	1	0	1
+0.6 ns					0	1	1	0
+0.7 ns					0	1	1	1
+0.8 ns					1	0	0	0
+0.9 ns					1	0	0	1
RFU					1	0	1	0
.	.	.	.	.	.	.	.	
Undefined	1	1	1	1	1	1	1	1