

4.1.2.6 – Appendix F: Specific PD's for Address Multiplexed ROMs (MXROM).

1.0 Introduction: This appendix describes the Presence Detects for Multiplexed ROM modules. These PD's are those referenced in the SPD standard as "Specific Features". The following PD fields will occur, in the order presented, at the point in the standard where the Specific Features are referenced; that is after the identification of the Fundamental Memory Type and before identification of whether there is any Superset Features presented. For convenience sake however, the complete address map is presented herein.

1.1 Address map: The following is the SPD address map for Multiplexed ROM. It describes where the individual LUT-Entries/ bytes will be held in the serial EEPROM:

Byte Number	Function described	Notes
0	Defines # bytes written into serial memory at module mfg	1
1	Total # bytes of SPD memory device	2
2	Fundamental memory type (FPM, EDO, SDRAM...) from appendix A	
3	# Row Addresses on this assembly	
4	# Column Addresses on this assembly	
5	# ROM Banks on this Assembly	
6	Data Width of this assembly...	
7	...Data Width continuation	
8	Voltage interface standard of this assembly	
9	Address Access Time of this assembly\$	3
10	\$Address Access Time continuation	3
11	DIMM Configuration type (Non-parity, Parity, ECC)	
12	Reserved	
13	Page Mode Access Time of this assembly	3
14	Output Enable Access Time of this assembly	3
15	Chip Enable Access Time of this assembly\$	3
16	\$Chip Enable Access Time continuation	3
17	Burst Length of this assembly	
18–31	Reserved for future offerings	
32	Superset Memory Type (may be used in future)	
33–62	Superset Memory Specific Features (may be used in future)	
63	Checksum for bytes 0–62	
64–71	Manufacturers JEDEC ID code per JEP-106	4
72	Manufacturing location	4
73–90	Manufacturer's Part Number	4
91–92	Revision Code	4
93–94	Manufacturing date	4
95–98	Assembly Serial Number	4
99–125	Manufacturer Specific Data	4
126–127	Reserved	
128–255	Open User Free-Form area\$not defined	

notes:

- 1) This will be 128 bytes for Multiplexed ROM assemblies.
- 2) This will be 256 bytes, represented as 08h. See below.
- 3) From data sheet.
- 4) Per the JEDEC spec, these are optional.

2 Bytes #0–2, For Reference: Descriptions of bytes 0–1 can be found in the main body of the SPD standard, and byte 2 is detailed in appendix A to this standard. For reference and convenience, applicable portions of their descriptions are presented again:

2.1 BYTE #0, From General SPD Standard, Number of Bytes used by Module Manufacturer: This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

2.2 Byte #1, From General SPD Standard, Total SPD Memory Size: This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor:

Serial Memory Density	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16284 Bytes	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	1	1	1	1	1	1	1	0
.	1	1	1	1	1	1	1	1

- 2.3 Byte #2, From Appendix A, Memory Type:** This byte describes the fundamental memory type (or technology) implemented on the module:

Fundamental Mem. Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	0	0	0	0	0	0	0	0
Standard FPM DRAM	0	0	0	0	0	0	0	1
EDO	0	0	0	0	0	0	1	0
.	.	.	.	.	.	.	.	.
Multiplexed ROM	0	0	0	0	0	1	0	1

- 3 Data Type(s):** Even though many of the PD's seem to be binary numbers representing the feature they are describing, they are considered Look Up Table (LUT) entries.
- 4** The following PD bytes are those specific to modules implementing ROM devices with a multiplexed address interface. Note that full descriptions start at byte 3 and are not covered in the main body of the SPD standard since they are specific to a given fundamental memory type/technology.

- 4.1 Byte #3, Number of ROW Addresses:** This first field describes the number of Row Addresses in the ROM array:

No. of Row Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1