

Appendix X: Serial Presence Detect (SPD) for Fully Buffered DIMM (Revision 1.1)

1.0 Introduction

This appendix describes the serial presence detect (SPD) values for Fully Buffered DIMMs. These presence detects are those referenced in the SPD standard document for ‘Specific Features’. The following SPD fields will occur in the order presented in section 1.1. *Note that the descriptions of Bytes 0 and 1 are different from those found in previous SPD standards.* Further description of Byte 2 is found in Appendix A of the SPD standard. All unused entries will be coded as 0x00. All unused bits in defined bytes will be coded as 0 except where noted.

1.1 Address map

The following is the SPD address map for FB-DIMM, i.e., when the value in Key Byte 2 is 0x09. It describes where the individual look-up table entries will be held in the serial EEPROM.

Byte Number	Function Described	Notes
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	1,2
1	SPD Revision	
2	Key Byte / DRAM Device Type	
3	Voltage Levels of this Assembly	
4	SDRAM Addressing	
5	Module Physical Attributes	
6	Module Type / Thickness	
7	Module Organization	
8	Fine Timebase Dividend and Divisor	
9	Medium Timebase Dividend	
10	Medium Timebase Divisor	
11	SDRAM Minimum Cycle Time (tCKmin)	3
12	SDRAM Maximum Cycle Time (tCKmax)	3
13	SDRAM CAS Latencies Supported	
14	SDRAM Minimum CAS Latency Time (tCAS)	
15	SDRAM Write Recovery Times Supported	
16	SDRAM Write Recovery Time (tWR)	3
17	SDRAM Write Latencies Supported	
18	SDRAM Additive Latencies Supported	
19	SDRAM Minimum RAS to CAS Delay (tRCD)	3
20	SDRAM Minimum Row Active to Row Active Delay (tRRD)	3
21	SDRAM Minimum Row Precharge Time (tRP)	3
22	SDRAM Upper Nibbles for tRAS and tRC	3
23	SDRAM Minimum Active to Precharge Time (tRAS)	3
24	SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Time (tRC)	3
25-26	SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)	3
27	SDRAM Internal Write to Read Command Delay (tWTR)	3
28	SDRAM Internal Read to Precharge Command Delay (tRTP)	3
29	SDRAM Burst Lengths Supported	
30	SDRAM Terminations Supported	

Byte Number	Function Described	Notes
31	SDRAM Drivers Supported	
32	SDRAM Average Refresh Interval (tREFI) / Double Refresh mode bit / High Temperature self-refresh rate support indication	3
33	Bits 7:4: Tcasemax Delta (SDRAM case temperature difference between maximum case temperature and baseline maximum case temperature), the baseline maximum case temperature is 85 °C. Bits 3:0: DT4R4W Delta (Case temperature rise difference between IDD4R/page open burst read and IDD4W/page open burst write operations).	6, 7, 10, 11
34	Thermal resistance of SDRAM device package from top (case) to ambient (Psi T-A SDRAM) at still air condition based on JESD51-2 standard.	5, 9, 11
35	DT0: Case temperature rise from ambient due to IDD0/activate-precharge operation minus 2.8 °C offset temperature.	6, 7, 10, 11
36	DT2N/DT2Q: Case temperature rise from ambient due to IDD2N/precharge standby operation for UDIMM and due to IDD2Q/precharge quiet standby operation for RDIMM.	6, 7, 10, 11
37	DT2P: Case temperature rise from ambient due to IDD2P/precharge power-down operation.	6, 7, 10, 11
38	DT3N: Case temperature rise from ambient due to IDD3N/active standby operation.	6, 7, 10, 11
39	DT4R/Mode Bit: Bits 7:1: Case temperature rise from ambient due to IDD4R/page open burst read operation. Bit 0: Mode bit to specify if DT4W is greater or less than DT4R.	6, 7, 10, 11
40	DT5B: Case temperature rise from ambient due to IDD5B/burst refresh operation.	6, 7, 10, 11
41	DT7: Case temperature rise from ambient due to IDD7/bank interleave read mode operation.	6, 7, 10, 11
42-59	Reserved	
60-78	Reserved	
79	FB-DIMM ODT Values	
80	Reserved	
81-82	FB-DIMM Channel Protocols Supported	
83	Back-to-Back Access Turnaround Time	
84	AMB Read Access Time for DDR2-800 (AMB.LINKPARNXT[1:0] = 11)	
85	AMB Read Access Time for DDR2-667 (AMB.LINKPARNXT[1:0] = 10)	
86	AMB Read Access Time for DDR2-533 (AMB.LINKPARNXT[1:0] = 01)	
87	Thermal Resistance of AMB Package from top (case) to ambient (Psi T-A AMB)	
88	AMB DT Idle_0	8, 10, 11
89	AMB DT Idle_1	8, 10, 11
90	AMB DT Idle_2	8, 10, 11
91	AMB DT Active_1	8, 10, 11
92	AMB DT Active_2	8, 10, 11
93	AMB DT L0s	8, 10, 11
94-97	Reserved	
98	AMB Case Temperature Maximum (Tcase_max)	
99-100	Reserved	
101-106	AMB Personality Bytes: Pre-initialization	
107-114	AMB Personality Bytes: Post-initialization	
115-116	AMB Manufacturer's JEDEC ID Code	
117-118	Module ID: Module Manufacturer's JEDEC ID Code	

Byte Number	Function Described	Notes
119	Module ID: Module Manufacturing Location	
120-121	Module ID: Module Manufacturing Date	
122-125	Module ID: Module Serial Number	
126-127	Cyclical Redundancy Code	
128-145	Module Part Number	4
146-147	Module Revision Code	4
148-149	SDRAM Manufacturer's JEDEC ID Code	4
150-175	Manufacturer's Specific Data	4
176-255	Open for customer use	

1. Number of SPD bytes written will typically be programmed as 128 or 176 bytes.
2. Size of SPD device will typically be programmed as 256 bytes.
3. From SDRAM datasheet.
4. These are optional, in accordance with the JEDEC spec.
5. Refer to JESD51-3 "Low Effective Thermal Conductivity Test Board for Leadless Surface Mount Packages" under JESD51-2 standard.
6. DT parameter is derived as following: $DTx = IDDx * VDD * \Psi_{T-A}$, where $IDDx$ definition is based on JEDEC DDR2 Component Specification and at $VDD = 1.9\text{ V}$, it is the datasheet (worst case) value, and Ψ_{T-A} is the programmed value of Ψ_{T-A} (value in SPD Byte 33). Programmed temperature rise data (DTx) is based on the programmed value of Ψ_{T-A} (value in SPD byte 33).
7. All DT parameters are defined for DDR2 SDRAM densities up to 2 Gbit. 4 Gbit parameters will be defined later.
8. DT parameters for the AMB are derived as following: $DTx = (IDDx * VDD * \Psi_{T-A}) + (ICCx * VCC * \Psi_{T-A}) + (IDDSPDx * VDDSPD * \Psi_{T-A})$ where $IDDx$ is at $VDD = 1.9\text{ V}$, $ICCx$ is at $VCC = 1.535\text{ V}$, and $IDDSPDx$ is at $VDDSPD = 3.6\text{ V}$; these are the active AMB powers corresponding to the AMB's respective DIMM configuration loading. The $IDDx$, $ICCx$, and $ISPDx$ are worst case values. Ψ_{T-A} used to program DTx is the programmed value of AMB Ψ_{T-A} (value in SPD byte 87).
9. Rule for rounding off thermal resistance values: Ψ_{X-X} shall be rounded such that it is nearest/closest to the true value of Ψ_{X-X} .
10. Rule for rounding off DTx : DTx shall be rounded such that it is nearest/closest to the calculated value of DTx .
11. Thermal bytes are for the DIMM as shipped, with any associated heat spreader, heat sink, mechanical clips, and label.

2.0 Details of each byte

2.1 General Section: Bytes 0 to 59

This section contains fields which with little modification can be used for SPD definitions for non-FB-DIMM modules.

Byte 0: Number of Bytes Utilized / Number of Bytes in SPD Device / CRC Coverage

The least significant nibble of this byte describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data. Bits 6-4 describe the total size of the serial memory used to hold the Serial Presence Detect data. Bit 7 indicates whether the unique module identifier (found in bytes 117 to 125) is covered by the CRC encoded on bytes 126 and 127.

Bit 7	Bit 6 ~ 4	Bit 3 ~ Bit 0
CRC Coverage	SPD Bytes Total	SPD Bytes Used
0 = CRC covers bytes 0 ~ 125 1 = CRC covers bytes 0 ~ 116	Bit [6, 5, 4] : 000 = Undefined 001 = 256 All Others TBD	Bit [3, 2, 1, 0] : 0000 = Undefined 0001 = 128 0010 = 176 0011 = 256 All Others TBD

Byte 1: SPD Revision

This byte describes the compatibility level of the encoding of the bytes contained in the SPD EEPROM, and the current collection of valid defined bytes. This byte must be coded as 0x11 for SPDs with revision level 1.1. Software should examine the upper nibble(Encoding Level) to determine if it can correctly interpret the contents of the module SPD. The lower nibble (Additions Level) can optionally be used to determine which additional bytes or attribute bits have been defined; however, since any undefined additional byte must be encoded as 0x00 or undefined attribute bit must be defined as 0, software can safely detect additional bytes and use safe defaults if a zero encoding is read for these bytes.

SPD Revision	Encoding Level				Additions Level				Hex
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Revision 0.0	0	0	0	0	0	0	0	0	00
Undefined	0	0	0	0	0	0	0	1	01
...	.	.	.	.	.	.	.	.	.
Revision 1.0	0	0	0	1	0	0	0	0	10
Revision 1.1	0	0	0	1	0	0	0	1	11
...	.	.	.	.	.	.	.	.	...
Undefined	1	1	1	1	1	1	1	1	FF

Byte 2: Key Byte

This byte is the key byte used by BIOS to determine how to interpret all other bytes in the SPD EEPROM. BIOS must check this byte first to ensure that the EEPROM data is interpreted correctly. Any SDRAM or Module type that requires significant changes to the SPD format (beyond defining previously undefined bytes or bits) also requires a new entry in the key byte table below.

Line #	SDRAM / Module Type Corresponding to Key Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Reserved	0	0	0	0	0	0	0	0	00
1	Standard FPM DRAM	0	0	0	0	0	0	0	1	01
2	EDO	0	0	0	0	0	0	1	0	02
3	Pipelined Nibble	0	0	0	0	0	0	1	1	03
4	SDRAM	0	0	0	0	0	1	0	0	04
5	ROM	0	0	0	0	0	1	0	1	05
6	DDR1 SGRAM	0	0	0	0	0	1	1	0	06
7	DDR1 SDRAM	0	0	0	0	0	1	1	1	07
8	DDR2 SDRAM	0	0	0	0	1	0	0	0	08
9	DDR2 SDRAM FB-DIMM	0	0	0	0	1	0	0	1	09
10	DDR2 SDRAM FB-DIMM PROBE	0	0	0	0	1	0	1	0	0A
-	-	-	-	-	-	-	-	-	-	-
253	TBD	1	1	1	1	1	1	0	1	FD
254	TBD	1	1	1	1	1	1	1	0	FE
255	TBD	1	1	1	1	1	1	1	1	FF

Byte 3: Voltage Levels of this Assembly

This byte describes the expected voltage level for two power supplies that are connected to the module. For example, Fully Buffered DIMM Power Supply 1 is defined as the supply for the channel interface, and Power Supply 2 is defined as the supply for the DRAM interface.

Bit 7 ~ 4	Bit 3 ~ Bit 0
Power Supply 2	Power Supply 1
Bit [7, 6, 5, 4] : 0000 = Undefined 0001 = 1.8 V 0010 = 1.5 V 0011 = 1.2 V All Others TBD	Bit [3, 2, 1, 0] : 0000 = Undefined 0001 = 1.8 V 0010 = 1.5 V 0011 = 1.2 V All Others TBD

Byte 4: SDRAM Addressing

This byte describes the row addressing, the column addressing, and the number of banks in the SDRAM device. Bits 1-0 encode the number of banks, bits 4-2 encode the number of column address bits, and bits 7-5 encode the number of row address bits.

Bit 7 ~ 5	Bit 4 ~ 2	Bit 1 ~ Bit 0
Row Address Bits	Column Address Bits	Number of Banks
Bit [7, 6, 5] : 000 = 12 001 = 13 010 = 14 011 = 15 All Others TBD	Bit [4, 3, 2] : 0000 = 9 0001 = 10 0010 = 11 All Others TBD	Bit [1, 0] : 00 = 4 01 = 8 10 = 16 11 = 32

Byte 5: Module Physical Attributes

This byte describes the height and thickness of the SDRAM module. Bits 2-0 encode the module thickness, which is defined as the maximum value including all finished assembly parts: devices, heat spreaders, or other mechanical components. Encodings for bits 2-0 will depend on the value of Byte 6, the Module Type.

Bit 7 ~ Bit 6	Bit 5 ~ Bit 3	Bit 2 ~ Bit 0
Reserved	Module Height (mm)	Module Thickness (mm)
	Bit [5, 4, 3] : 000 = Undefined 001 = $15 < x \leq 20$ 010 = $20 < x \leq 25$ 011 = $25 < x \leq 30$ 100 = $30 < x \leq 35$ 101 = $35 < x \leq 40$ 110 = $40 < x \leq 50$ All others undefined	Bit [2, 1, 0] : See indexed tables below
Note: Refer to JEDEC standard MO-256 for standard module outline characteristics including height and thickness.		

Decoding of the Module Thickness field, based on Module Type (units in mm) is shown below. Table entries other than FB-DIMM are shown for reference only.

Module Thickness			FB-DIMM
Bit 2	Bit 1	Bit 0	Byte 6 [3:0] = 0111
0	0	0	Undefined / Not specified
0	0	1	$x \leq 6.0$
0	1	0	$6.0 < x \leq 7.0$
0	1	1	$7.0 < x \leq 8.0$
1	0	0	$8.0 < x \leq 9.0$
1	0	1	$9.0 < x$
1	1	0	Reserved
1	1	1	Reserved

Byte 6: Module Type

This byte identifies the SDRAM memory module type and also indicates the width of the module. BIOS uses the module type information in this byte to determine the encoding of the module thickness field in byte 5.

Table entries other than FB-DIMM are shown for reference only.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
Reserved	Module Type
	Bit [3, 2, 1, 0] : 0000 = Undefined 0001 = RDIMM (width = 133.35 mm nom) 0010 = UDIMM (width = 133.35 mm nom) 0011 = SO-DIMM (width = 67.6 mm nom) 0100 = Micro-DIMM (width = 54.0 mm nom) 0101 = Mini-RDIMM (width = 82.0 mm nom) 0110 = Mini-UDIMM (width = 82.0 mm nom) 0111 = FB-DIMM (width = 133.35 mm nom) All others TBD
Definitions: RDIMM: Registered Dual In-Line Memory Module UDIMM: Unbuffered Dual In-Line Memory Module SO-DIMM: Small Outline Dual In-Line Memory Module Micro-DIMM: Micro Dual In-Line Memory Module Mini-RDIMM: Mini Registered Dual In-Line Memory Module Mini-UDIMM: Mini Unbuffered Dual In-Line Memory Module FB-DIMM: Fully Buffered Dual In-Line Memory Module	

Byte 7: Module Organization

This byte describes the organization of the SDRAM module. Bits 2-0 encode the device width of the SDRAM devices. Bits 5-3 encode the number of physical ranks on the SDRAM. For example, for a single-rank module with x8 SDRAMs, this byte is encoded 00 001 001, or 0x09.

Bit 7 ~ Bit 6	Bit 5 ~ Bit 3	Bit 2 ~ Bit 0
Reserved	Number of Ranks	SDRAM Device Width
	Bit [5, 4, 3] : 000 = Undefined 001 = 1 Rank 010 = 2 Ranks All others undefined	Bit [2, 1, 0] : 000 = 4 bits 001 = 8 bits 010 = 16 bits 011 = 32 bits All others undefined

Byte 8: Fine Timebase (FTB) Dividend / Divisor

This byte defines a value in picoseconds that represents the fundamental timebase for fine grain timing calculations. This value is used as a multiplier for formulating subsequent timing parameters. The fine timebase (FTB) is defined as the fine timebase dividend, bits 7~4, divided by the fine timebase divisor, bits 3~0. A value of 0x00 should only be programmed if the FTB is not utilized by any SPD fields.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
Fine Timebase (FTB) Dividend	Fine Timebase (FTB) Divisor
Values defined from 0 to 15	Values defined from 0 to 15

Examples:

Dividend	Divisor	Timebase (ps)	Use
5	1	5	When time granularity of 5 ps is required
5	2	2.5	When time granularity of 2.5 ps is required

Byte 9: Medium Timebase (MTB) Dividend

Byte 10: Medium Timebase (MTB) Divisor

These bytes define a value in nanoseconds that represents the fundamental timebase for medium grain timing calculations. This value is typically the greatest common divisor for the range of clock frequencies (clock periods) supported by a particular SDRAM. This value is used as a multiplier for formulating subsequent timing parameters. The medium timebase (MTB) is defined as the medium timebase dividend (byte 9) divided by the medium timebase divisor (byte 10).

Byte 9 Bit 7 ~ Bit 0	Byte 10 Bit 7 ~ Bit 0
Medium Timebase (MTB) Dividend	Medium Timebase (MTB) Divisor
Values defined from 1 to 255	Values defined from 1 to 255

Examples:

Dividend	Divisor	Timebase (ns)	Use
1	4	0.25	For clock frequencies of 200, 267, 333, and 400 MHz
1	8	0.125	For clock frequencies of 400, 533, 667, and 800 MHz

To simplify BIOS implementation, DIMMs associated with a given key byte value may differ in MTB value only by a factor of two. For DDR2 FB-DIMM (key byte values 0x09 and 0x10), the defined MTB values are:

Dividend	Divisor	Timebase (ns)	Use
1	4	0.25	FB-DIMM MTB Value
1	8	0.125	FB-DIMM MTB Value

Byte 11: Minimum SDRAM Cycle Time (t_{CKmin})

This byte defines the minimum cycle time for the SDRAM module, in medium timebase (MTB) units. This number applies to all applicable components on the module. This byte applies to SDRAM and support components as well as the overall capability of the DIMM.

Bit 7 ~ Bit 0
Minimum SDRAM Cycle Time (t_{CKmin}) MTB Units
Values defined from 1 to 255

Examples:

t_{CKmin} (MTB units)	Timebase (ns)	t_{CKmin} Result (ns)	Use
20	0.25	5	DDR2 with 200 MHz clock
15	0.25	3.75	DDR2 with 266 MHz clock
12	0.25	3	DDR2 with 333 MHz clock
10	0.25	2.5	DDR2 with 400 MHz clock
20	0.125	2.5	DDR3 with 400 MHz clock
15	0.125	1.875	DDR3 with 533 MHz clock
12	0.125	1.5	DDR3 with 667 MHz clock
10	0.125	1.25	DDR3 with 800 MHz clock

Byte 12: Maximum SDRAM Cycle Time (t_{CKmax})

This byte defines the maximum cycle time for the SDRAM module, in medium timebase (MTB) units. This number applies to all applicable components on the module. This byte applies to SDRAM and support components as well as the overall capability of the DIMM.

Bit 7 ~ Bit 0
Maximum SDRAM Cycle Time (t_{CKmax}) MTB Units
Values defined from 1 to 255

Examples:

t_{CKmax} (MTB units)	Timebase (ns)	t_{CKmax} Result (ns)	Use
32	0.25	8	DDR2, 125 MHz maximum clock period
64	0.125	8	DDR3, 125 MHz maximum clock period

Byte 13: CAS Latencies Supported

This field describes the CAS Latency (CL) values supported by the SDRAMs on the memory module, in units of memory clocks. The lower four bits describe the lowest value of CL, and the upper four bits describe the range, defined as total number of values supported. For example, SDRAMs that support CAS latencies 3, 4, and 5 would program a CL Range of 3 and a minimum CL of 3: 0011 0011 = 0x33.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
CL Range (clocks)	Minimum CL (clocks)
Bit [7, 6, 5, 4] : 0000 = Undefined 0001 = 1 0010 = 2 0011 = 3 0100 = 4 All other values TBD	Bit [3, 2, 1, 0] : 0011 = 3 0100 = 4 0101 = 5 0110 = 6 All other values TBD

Byte 14: Minimum CAS Latency Time (t_{AAmin})

his byte defines the minimum CAS Latency in medium timebase (MTB) units. Software can use this information, along with range of CAS Latencies supported (found in byte 13) to determine the optimal cycle time for a particular module. Parameter t_{AAmin} for a specific DDR2 SDRAM is the smallest number resulting from the multiplication of t_{CKmin} @ CL=n times the CAS latency n for each supported CAS latency for that SDRAM speed bin.

Bit 7 ~ Bit 0
Minimum SDRAM CAS Latency Time (t_{AAmin}) MTB Units
Values defined from 1 to 255

Examples:

t_{AAmin} (MTB units)	Timebase (ns)	t_{AAmin} Result (ns)	Use
60	0.25	15	DDR2-400B
80	0.25	20	DDR2-400C
45	0.25	11.25	DDR2-533B
60	0.25	15	DDR2-533C
48	0.25	12	DDR2-667C
60	0.25	15	DDR2-667D
40	0.25	10	DDR2-800C
50	0.25	12.5	DDR2-800D
60	0.25	15	DDR2-800E

Calculation Examples for t_{AAmin}

SDRAM suppliers may support more CAS latency values than the JEDEC required minimum, so the calculations shown here should be performed for all supported CL values.

Example 1: DDR2-533B

- t_{CKmin} @ CL=3 is 3.75 ns
- t_{CKmin} @ CL=4 is 3.75 ns
- $t_{AAmin} = \min(3 * 3.75, 4 * 3.75) = 11.25$ ns

Example 2: DDR2-800D

- t_{CKmin} @ CL=4 is 3.75 ns
- t_{CKmin} @ CL=5 is 2.5 ns
- $t_{AAmin} = \min(4 * 3.75, 5 * 2.5) = 12.5$ ns

CAS Latency Calculation and Examples

CAS latency is not a purely analog value as DDR2 SDRAMs use the DLL to synchronize data and strobe outputs with the clock. All possible frequencies may not be tested, therefore an application should use the next smaller JEDEC standard tCKmin value (5.0, 3.75, 3.0, or 2.5 ns) when calculating CAS Latency. This section shows how the BIOS calculates CAS latency based on Bytes 11 ~ 14.

Step 1: The BIOS first determines the common operating frequency of all modules in the system, ensuring that the corresponding value of tCK (tCKactual) falls between tCKmin (Byte 11) and tCKmax (Byte 12). If tCKactual is not a JEDEC standard value, the next smaller standard tCKmin value is used for calculating CAS Latency.

Step 2: The BIOS then calculates the “desired” CAS Latency (CLdesired):

$$CL_{desired} = \text{ceiling} (tA_{min} / tCK_{actual})$$

where tAmin is defined in Byte 14. The ceiling function requires that the quotient be rounded up always.

Step 3: The BIOS then determines the “actual” CAS Latency (CLactual):

$$CL_{actual} = \text{max} (CL_{desired}, \text{min CL supported})$$

where min CL supported is found in the least significant nibble of Byte 13.

Example 1: DDR2-533C 4-4-4 module operating at 533

tAmin = 15 ns
Min CL = 3, range = 3 (CL = 3, 4, 5 supported)
tCK actual = 3.75 ns (266 MHz Clock)
CLdesired = ceiling (15 / 3.75) = 4
CLactual = max (4, 3) = 4

Example 2: DDR2-667C 4-4-4 standard latency module operating at 533

tAmin = 12 ns
Min CL = 4, range = 3 (CL = 4, 5, 6 supported)
tCK actual = 3.75 ns (266 MHz Clock)
CLdesired = ceiling (12 / 3.75) = 4
CLactual = max (4, 4) = 4

Example 3: DDR2-667 4-4-4 fast latency module operating at 533 (downshifting to 3-3-3)

tAmin = 11.25 ns (chosen to allow CL=3 at 533, exceeds value required to meet minimum JEDEC standard)
Min CL = 3, range = 3 (CL = 3, 4, 5 supported)
tCK actual = 3.75 ns (266 MHz Clock)
CLdesired = ceiling (11.25 / 3.75) = 3
CLactual = max (3, 3) = 3

Example 4: DDR2-800D 5-5-5 module operating at 313 (debug & hardware bringup scenario)

tAmin = 12.5 ns
Min CL = 4, range = 3 (CL = 4, 5, 6 supported)
tCK actual = 3.2 ns (156 MHz Clock) reduced to next lower JEDEC standard tCKmin = 3.0 ns
CLdesired = ceiling (12.5 / 3.0) = 5
CLactual = max (5, 4) = 5

Byte 15: Write Recovery Times Supported

This field describes the Write Recovery (WR) values supported by the SDRAMs on the memory module, in units of memory clocks. The lower four bits describe the lowest value of WR, and the upper four bits describe the range, defined as total number of values supported. For example, SDRAMs that support WR values of 2 and 3 would program a WR Range of 2 and a minimum WR of 2: 0010 0010 = 0x22.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
WR Range (clocks)	Minimum WR (clocks)
Bit [7, 6, 5, 4] : 0000 = Undefined 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 All other values TBD	Bit [3, 2, 1, 0] : 0010 = 2 All other values TBD

Byte 16: Write Recovery Time (t_{WR})

This byte defines the SDRAM write recovery time in medium timebase (MTB) units.

Bit 7 ~ Bit 0
Minimum Write Recovery Time (t_{WR}) MTB Units
Values defined from 1 to 255

Example:

t_{WR} (MTB units)	Timebase (ns)	t_{WR} Result (ns)	Use
60	0.25	15	All DDR2 speed grades

Byte 17: Write Latencies Supported

This field describes the Write Latency (WL) values supported by the SDRAMs on the memory module, in units of memory clocks. The lower four bits describe the lowest value of WL, and the upper four bits describe the range, defined as total number of values supported. For example, SDRAMs that support WL values of 2, 3, and 4 would program a WL Range of 3 and a minimum WL of 2: 0011 0010 = 0x32.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
WL Range (clocks)	Minimum WL (clocks)
Bit [7, 6, 5, 4] : 0000 = Undefined 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 0110 = 6 0111 = 7 1000 = 8 1001 = 9 All other values TBD	Bit [3, 2, 1, 0] : 0010 = 2 All other values TBD

Byte 18: Additive Latencies Supported

This field describes the Additive Latency (AL) values supported by the SDRAMs on the memory module, in units of memory clocks. The lower four bits describe the lowest value of AL, and the upper four bits describe the range, defined as total number of values supported. For example, SDRAMs that support AL values of 0, 1, 2, and 3 would program a AL Range of 4 and a minimum AL of 0: 0100 0000 = 0x40.

Bit 7 ~ Bit 4	Bit 3 ~ Bit 0
AL Range (clocks)	Minimum AL (clocks)
Bit [7, 6, 5, 4] : 0000 = Undefined 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 0110 = 6 All other values TBD	Bit [3, 2, 1, 0] : 0000 = 0 All other values TBD

Byte 19: Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay (t_{RCD})

This byte defines the SDRAM RAS# to CAS# Delay in medium timebase (MTB) units.

Bit 7 ~ Bit 0
Minimum RAS# to CAS# Delay (t_{RCD}) MTB Units
Values defined from 1 to 255

Examples:

t_{RCD} (MTB units)	Timebase (ns)	t_{RCD} Result (ns)	Use
60	0.25	15	3 clocks at DDR2-400B
80	0.25	20	4 clocks at DDR2-400C
45	0.25	11.25	3 clocks at DDR2-533B
60	0.25	15	4 clocks at DDR2-533C
48	0.25	12	4 clocks at DDR2-667C
60	0.25	15	5 clocks at DDR2-667D
40	0.25	10	4 clocks at DDR2-800C
50	0.25	12.5	5 clocks at DDR2-800D
60	0.25	15	6 clocks at DDR2-800E

Byte 20: Minimum Row Active to Row Active Delay (t_{RRD})

This byte defines the minimum SDRAM Row Active to Row Active Delay in medium timebase units.

Bit 7 ~ Bit 0
Minimum Row Active to Row Active Delay (t_{RRD}) MTB Units
Values defined from 1 to 255

Examples:

t_{RRD} (MTB units)	Timebase (ns)	t_{RRD} Result (ns)	Use
30	0.25	7.5	For SDRAMs with 1KB page size
40	0.25	10	For SDRAMs with 2KB page size