

Annex L: Serial Presence Detect (SPD) for DDR4 SDRAM Modules

DDR4 SPD Document Release 1

UDIMM Revision 1.0

RDIMM Revision 1.0

LRDIMM Revision 1.0

1.0 Introduction

This annex describes the serial presence detect (SPD) values for all DDR4 modules. Differences between module types are encapsulated in subsections of this annex. These presence detect values are those referenced in the SPD standard document for 'Specific Features'. The following SPD fields will be documented in the order presented in section 1.1 with the exception of bytes 128~255 which are documented in separate annexes, one for each family of module types. Further description of Byte 2 is found in Annex A of the SPD standard.

All unused entries will be coded as 0x00. All unused bits in defined bytes will be coded as 0 except where noted.

DDR4 generation systems are required to check the voltages supported by the DRAMs by reading the SPD and parsing byte 6, the Module Nominal Voltage, before applying power to the DRAMs. All JEDEC standard modules allow applying SPD power without applying a supply voltage to the DRAMs in order to support this requirement.

Timing parameters in the SPD represent the operation of the module including all DRAMs and support devices at the lowest supported supply voltage (see SPD byte 11), and are valid from $t_{CKAVGmin}$ to $t_{CKAVGmax}$ (see SPD bytes 18 and 19).

To allow for maximum flexibility as devices evolve, SPD fields described in this document may support device configuration and timing options that are not included in the JEDEC DDR4 SDRAM data sheet (JESD79-4). Please refer to DRAM supplier data sheets or JESD79-4 to determine the compatibility of components.

1.1 Address map

The following is the SPD address map for all DDR4 modules. It describes where the individual lookup table entries will be held in the serial EEPROM. Consistent with the definition of DDR4 generation SPD devices, which have four individual write protection blocks of 128 bytes in length each, the SPD contents are aligned with these blocks as follows:

Block	Range		Description
0	0~127	0x000~0x07F	Base Configuration and DRAM Parameters
1	128~255	0x080~0x0FF	Module Specific Parameters -- See subsections L1, L2, and L3 for details
2	256~319	0x100~0x13F	Reserved -- must be coded as 0x00
	320~383	0x140~0x17F	Manufacturing Information
3	384~511	0x180~0x1FF	End User Programmable

Block 0: Base Configuration and DRAM Parameters

The following table details the location of each byte in this block.

Byte Number		Function Described	Notes
0	0x000	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	1, 2
1	0x001	SPD Revision	
2	0x002	Key Byte / DRAM Device Type	
3	0x003	Key Byte / Module Type	
4	0x004	SDRAM Density and Banks	3
5	0x005	SDRAM Addressing	3
6	0x006	SDRAM Package Type	3
7	0x007	SDRAM Optional Features	3
8	0x008	SDRAM Thermal and Refresh Options	3
9	0x009	Other SDRAM Optional Features	3
10	0x00A	Reserved -- must be coded as 0x00	
11	0x00B	Module Nominal Voltage, VDD	3
12	0x00C	Module Organization	
13	0x00D	Module Memory Bus Width	
14	0x00E	Module Thermal Sensor	
15~16	0x00F~0x010	Reserved -- must be coded as 0x00	
17	0x011	Timebases	
18	0x012	SDRAM Minimum Cycle Time ($t_{CKAVGmin}$)	3
19	0x013	SDRAM Maximum Cycle Time ($t_{CKAVGmax}$)	3
20	0x014	CAS Latencies Supported, First Byte	3
21	0x015	CAS Latencies Supported, Second Byte	3
22	0x016	CAS Latencies Supported, Third Byte	3
23	0x017	CAS Latencies Supported, Fourth Byte	3
24	0x018	Minimum CAS Latency Time (t_{AAmin})	3
25	0x019	Minimum RAS to CAS Delay Time (t_{RCDmin})	3

Note 1 Number of SPD bytes written will typically be programmed as 384 bytes.

Note 2 Size of SPD device will typically be programmed as 512 bytes.

Note 3 From DDR4 SDRAM datasheet.

Note 4 These are optional, in accordance with the JEDEC specification.



Byte Number		Function Described	Notes
26	0x01A	Minimum Row Precharge Delay Time (t_{RPmin})	3
27	0x01B	Upper Nibbles for t_{RASmin} and t_{RCmin}	3
28	0x01C	Minimum Active to Precharge Delay Time (t_{RASmin}), Least Significant Byte	3
29	0x01D	Minimum Active to Active/Refresh Delay Time (t_{RCmin}), Least Significant Byte	3
30	0x01E	Minimum Refresh Recovery Delay Time ($t_{RFC1min}$), LSB	3
31	0x01F	Minimum Refresh Recovery Delay Time ($t_{RFC1min}$), MSB	3
32	0x020	Minimum Refresh Recovery Delay Time ($t_{RFC2min}$), LSB	3
33	0x021	Minimum Refresh Recovery Delay Time ($t_{RFC2min}$), MSB	3
34	0x022	Minimum Refresh Recovery Delay Time ($t_{RFC4min}$), LSB	3
35	0x023	Minimum Refresh Recovery Delay Time ($t_{RFC4min}$), MSB	3
36	0x024	Minimum Four Activate Window Time (t_{FAWmin}), Most Significant Nibble	3
37	0x025	Minimum Four Activate Window Time (t_{FAWmin}), Least Significant Byte	3
38	0x026	Minimum Activate to Activate Delay Time (t_{RRD_Smin}), different bank group	3
39	0x027	Minimum Activate to Activate Delay Time (t_{RRD_Lmin}), same bank group	3
40	0x28	Minimum CAS to CAS Delay Time (t_{CCD_Lmin}), same bank group	3
41~59	0x029~0x03B	Reserved -- must be coded as 0x00	
60~77	0x03C~0x04D	Connector to SRAM Bit Mapping	
78~116	0x04E~0x074	Reserved -- must be coded as 0x00	
117	0x75	Fine Offset for Minimum CAS to CAS Delay Time (t_{CCD_Lmin}), same bank group	
118	0x76	Fine Offset for Minimum Activate to Activate Delay Time (t_{RRD_Lmin}), same bank group	3
119	0x77	Fine Offset for Minimum Activate to Activate Delay Time (t_{RRD_Smin}), different bank group	3
120	0x078	Fine Offset for Minimum Activate to Activate/Refresh Delay Time (t_{RCmin})	3
121	0x079	Fine Offset for Minimum Row Precharge Delay Time (t_{RPmin})	3
122	0x07A	Fine Offset for Minimum RAS to CAS Delay Time (t_{RCDmin})	3
123	0x07B	Fine Offset for Minimum CAS Latency Time (t_{Amin})	3
124	0x07C	Fine Offset for SDRAM Maximum Cycle Time ($t_{CKAVGmax}$)	3
125	0x07D	Fine Offset for SDRAM Minimum Cycle Time ($t_{CKAVGmin}$)	3
126	0x07E	CRC for Base Configuration Section, Least Significant Byte	
127	0x07F	CRC for Base Configuration Section, Most Significant Byte	
Note 1 Number of SPD bytes written will typically be programmed as 384 bytes. Note 2 Size of SPD device will typically be programmed as 512 bytes. Note 3 From DDR4 SDRAM datasheet. Note 4 These are optional, in accordance with the JEDEC specification.			

Block 1: Module Specific Parameters

Bytes 128~255 (0x080~0x0FF) Parameters in this block are specific to the module type as selected by the contents of SPD Key Byte 3. Refer to the appropriate annex for detailed byte descriptions.

Block 2, lower half: Reserved

Bytes 256~319 (0x100~0x13F) Reserved -- must be coded as 0x00.

Block 2, upper half: Manufacturing Information

Bytes 320~383 (0x140~0x17F) The following table details the location of each byte in this block.

Byte Number		Function Described	Notes
320	0x140	Module Manufacturer's ID Code, Least Significant Byte	
321	0x141	Module Manufacturer's ID Code, Most Significant Byte	
322	0x142	Module Manufacturing Location	
323~324	0x143~0x144	Module Manufacturing Date	
325~328	0x145~0x148	Module Serial Number	
329~348	0x149~0x15C	Module Part Number	
349	0x15D	Module Revision Code	
350	0x15E	DRAM Manufacturer's ID Code, Least Significant Byte	
351	0x15F	DRAM Manufacturer's ID Code, Most Significant Byte	
352	0x160	DRAM Stepping	
353~381	0x161~0x17D	Module Manufacturer's Specific Data	
382~383	0x17E~0x17F	Reserved; must be coded as 0x00	

Block 3: End User Programmable

Bytes 384~511 (0x180~0x1FF) Bytes in this block are reserved for use by end users.

2.0 Details of each byte

2.1 General Configuration Section: Bytes 0~127 (0x000~0x07F)

This section contains defines parameters that are common to all DDR4 module types.

Byte 0 (0x000): Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage

The least significant nibble of this byte describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data. Bits 6~4 describe the total size of the serial memory used to hold the Serial Presence Detect data.

Bit 7	Bits 6~4	Bits 3~0
Reserved	SPD Bytes Total	SPD Bytes Used
Reserved	Bit [6, 5, 4] : 000 = Undefined 001 = 256 010 = 512 All others reserved	Bit [3, 2, 1, 0] : 0000 = Undefined 0001 = 128 0010 = 256 0011 = 384 0100 = 512 All others reserved
Note 1 Typical programming of bits 3~0 will be 0011 (384 bytes).		

Byte 1 (0x001): SPD Revision

This byte describes the compatibility level of the encoding of the bytes contained in the SPD EEPROM, and the current collection of valid defined bytes. Software should examine the upper nibble (Encoding Level) to determine if it can correctly interpret the contents of the module SPD. The lower nibble (Additions Level) can optionally be used to determine which additional bytes or attribute bits have been defined; however, since any undefined additional byte must be encoded as 0x00 or undefined attribute bit must be defined as 0, software can safely detect additional bytes and use safe defaults if a zero encoding is read for these bytes.

Production Status	SPD Revision	Encoding Level				Additions Level				Hex
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Pre-production	Revision 0.0	0	0	0	0	0	0	0	0	00
	Revision 0.1	0	0	0	0	0	0	0	1	01
	...	.	.	.	.	.	.	.	.	.
	Revision 0.9	0	0	0	0	1	0	0	1	09
Production	Revision 1.0	0	0	0	1	0	0	0	0	10
	Revision 1.1	0	0	0	1	0	0	0	1	11
	...	.	.	.	.	.	.	.	.	...
Undefined	Undefined	1	1	1	1	1	1	1	1	FF

The Additions Level is never reduced even after an increment of the Encoding Level. For example, if the current SPD revision level were 1.2 and a change in Encoding Level were approved, the next revision level would be 2.2. If additions to revision 2.2 were approved, the next revision would be 2.3. Changes in the Encoding Level are extremely rare, however, since they can create incompatibilities with older systems.

The exceptions to the above rule are the SPD revision levels used during development prior to the Revision 1.0 release. Revisions 0.0 through 0.9 are used to indicate sequential pre-production SPD revision levels, however the first production release will be Revision 1.0.

This document defines the SPD contents for multiple families of DDR4 memory modules, with a separate subsection of this Annex for each family that defines the bytes in SPD locations 128~255 (0x080~0x0FF). These module families and their respective subsections are:

- Annex L.1: Unbuffered Memory Modules
- Annex L.2: Registered Memory Modules
- Annex L.3: Load Reduced Memory Modules

The SPD revision level for each module family type is independent. This allows changes to be made to the Registered DIMM annex, for example, without necessarily changing the revision of Unbuffered DIMMs. In this context, the SPD revision value corresponds to all SPD bytes *for that DIMM type*. It also means that over time, the revisions for each module type may vary. Note that changes to a DIMM specific annex do not affect the revisions of other module types, but changes in the General Section of the SPD affect all DIMM types. The following example suggests a possible historical progression:

Table 1 — Hypothetical Historic Progression of SPD Revisions by DIMM Type

Event	UDIMM	RDIMM	LRDIMM
Initial SPD release	1.0	1.0	1.0
Addition in RDIMM Annex	1.0	1.1	1.0
Addition in LRDIMM Annex	1.0	1.1	1.1
Addition in LRDIMM Annex	1.0	1.1	1.2
Addition in General Section	1.1	1.2	1.3
Addition in UDIMM Annex	1.2	1.2	1.3
Encoding change in LRDIMM Annex	1.2	1.2	2.3
Addition in LRDIMM Annex	1.2	1.2	2.4
Encoding change in General Section	2.2	2.2	3.4
Addition in RDIMM Annex	2.2	2.3	3.4

Byte 2 (0x002): Key Byte / DRAM Device Type

This byte is the key byte used by the system BIOS to determine how to interpret all other bytes in the SPD EEPROM. The BIOS must check this byte first to ensure that the EEPROM data is interpreted correctly. Any DRAM or Module type that requires significant changes to the SPD format (beyond defining previously undefined bytes or bits) also requires a new entry in the key byte table below.

Line #	SDRAM / Module Type Corresponding to Key Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Reserved	0	0	0	0	0	0	0	0	00
1	Fast Page Mode	0	0	0	0	0	0	0	1	01
2	EDO	0	0	0	0	0	0	1	0	02
3	Pipelined Nibble	0	0	0	0	0	0	1	1	03
4	SDRAM	0	0	0	0	0	1	0	0	04
5	ROM	0	0	0	0	0	1	0	1	05
6	DDR SGRAM	0	0	0	0	0	1	1	0	06
7	DDR SDRAM	0	0	0	0	0	1	1	1	07
8	DDR2 SDRAM	0	0	0	0	1	0	0	0	08
9	DDR2 SDRAM FB-DIMM	0	0	0	0	1	0	0	1	09
10	DDR2 SDRAM FB-DIMM PROBE	0	0	0	0	1	0	1	0	0A
11	DDR3 SDRAM	0	0	0	0	1	0	1	1	0B
12	DDR4 SDRAM	0	0	0	0	1	1	0	0	0C
-	-	-	-	-	-	-	-	-	-	-
253	Reserved	1	1	1	1	1	1	0	1	FD
254	Reserved	1	1	1	1	1	1	1	0	FE
255	Reserved	1	1	1	1	1	1	1	1	FF

Byte 3 (0x003): Key Byte / Module Type

This byte is a Key Byte used to index the module specific section of the SPD from bytes 128~255. Byte 3 identifies the SDRAM memory module type which implies the width (D dimension) of the module. Other module physical characteristics, such as height (A dimension) or thickness (E dimension) are documented in the module specific section of the SPD. Refer to the relevant JEDEC JC-11 module outline (MO) documents for dimension definitions.

Bits 7~4	Bits 3~0
Reserved	Module Type
	Bit [3, 2, 1, 0] : 0000 = Undefined 0001 = RDIMM (width = 133.35 mm nom) 0010 = UDIMM (width = 133.35 mm nom) 0011 = SO-DIMM (width = 68.60 mm nom) 0100 = LRDIMM (width = 133.35 mm nom) All others reserved
Definitions: RDIMM: Registered Dual In-Line Memory Module UDIMM: Unbuffered Dual In-Line Memory Module SO-DIMM: Unbuffered Small Outline Dual In-Line Memory Module LRDIMM: Load Reduced Dual In-Line Memory Module	

Byte 4 (0x004): SDRAM Density and Banks

This byte defines the total density of the DDR4 SDRAM, in bits, and the number of internal banks and bank groups into which the memory array is divided. These values come from the DDR4 SDRAM data sheet.

Bits 7~6	Bits 5~4	Bits 3~0
Bank Group Bits	Bank Address Bits ¹	Total SDRAM capacity, in megabits
Bits [7, 6]: 00 = 0 (no bank groups) 01 = 1 (2 bank groups) 10 = 2 (4 bank groups) 11 = reserved	Bit [5, 4]: 00 = 2 (4 banks) 01 = 3 (8 banks) All others reserved	Bit [3, 2, 1, 0]: 0000 = 256 Mb 0001 = 512 Mb 0010 = 1 Gb 0011 = 2 Gb 0100 = 4 Gb 0101 = 8 Gb 0110 = 16 Gb 0111 = 32 Gb All others reserved
Note 1 Bank Address Bits determine the number of banks in each Bank Group.		

Byte 5 (0x005): SDRAM Addressing

This byte describes the row addressing and the column addressing in the SDRAM device. Bits 2~0 encode the number of column address bits, and bits 5~3 encode the number of row address bits. These values come from the DDR4 SDRAM data sheet.

Bits 7~6	Bits 5~3	Bits 2~0
Reserved	Row Address Bits	Column Address Bits
Reserved	Bit [5, 4, 3]: 000 = 12 001 = 13 010 = 14 011 = 15 100 = 16 101 = 17 110 = 18 All others reserved	Bit [2, 1, 0]: 000 = 9 001 = 10 010 = 11 011 = 12 All others reserved

Byte 6 (0x006): SDRAM Package Type

This byte describes the type of SDRAM Device on the module.

Bit 7	Bits 6~4	Bits 3~2	Bit 1~0
SDRAM Package Type	Die Count	Reserved	Signal Loading ²
0 = Monolithic DRAM Device 1 = Non-Monolithic Device ¹	000 = Single die 001 = 2 die 010 = 3 die 011 = 4 die 100 = 5 die 101 = 6 die 110 = 7 die 111 = 8 die All others settings reserved.	00	00 = Not specified 01 = Multi load stack 10 = Single load stack (3DS) 11 = Reserved
Note 1 This includes Dual Die, Quad Die, Multi-Die, 3DS, or physically stacked devices - anything that is outside the standard monolithic device Note 2 Refers to loading on signals at the SDRAM balls. Loading on certain signals (CKE, ODT, etc.) per specification of device stacking as defined in JESD79-4			

Terminology:

SDRAM Package Type	Abbreviation	Description	# Electrical Loads ...			
			... On data, mask, and strobe signals	... On address and command signals	... On control signals except CKE	... On CKE signals
Monolithic	SDP	Single die package	1	1	1	1
Multi-load stack	DDP	Dual Die Package	2	2	1	1
	QDP	Quad Die Package	4	4	1	2
Single load stack	2H 3DS	Two SDRAM die single load stack	1	1	1	1
	3H 3DS	Three SDRAM die single load stack	1	1	1	1
	4H 3DS	Four SDRAM die single load stack	1	1	1	1
	5H 3DS	Five SDRAM die single load stack	1	1	1	1
	6H 3DS	Six SDRAM die single load stack	1	1	1	1
	7H 3DS	Seven SDRAM die single load stack	1	1	1	1
	8H 3DS	Eight SDRAM die single load stack	1	1	1	1

Byte 7 (0x007): SDRAM Optional Features

This byte defines support for certain SDRAM features. This value comes from the DDR4 SDRAM data sheet.

Bits 7~6	Bits 5~4	Bits 3~0
Reserved	Maximum Activate Window (tMAW)	Maximum Activate Count (MAC)
Reserved; must be coded as 0	Bits [5, 4]: 00 = 8192 * tREFI 01 = 4096 * tREFI 10 = 2048 * tREFI 11 = Reserved	Bits [3, 2, 1, 0] : 0000 = Untested MAC ¹ 0001 = 700 K 0010 = 600 K 0011 = 500 K 0100 = 400 K 0101 = 300 K 0110 = 200 K 0111 = Reserved 1000 = Unlimited MAC ² All other codes reserved
Note 1 Untested MAC means the device is not tested for tMAW and/or MAC; no particular value should be assumed. Note 2 Unlimited MAC means there is no restriction to the number of activates to a given row in a refresh period providing DRAM timing requirements such as tRCmin and refresh requirements are not violated.		

Byte 8 (0x008): SDRAM Thermal and Refresh Options

This byte describes the module's supported operating temperature ranges and refresh options. These values come from the DDR4 SDRAM data sheet. Please refer to the DDR4 SDRAM data sheet (JESD79-4 or supplier data sheet) for a complete description of these options.

Bits 7~0
Reserved
Reserved; must be coded as 0x00

Byte 9 (0x009): Other SDRAM Optional Features

This byte defines support for certain SDRAM features. This value comes from the DDR4 SDRAM data sheet.

Bits 7~6	Bits 5~0
Post Package Repair (PPR)	Reserved
00: PPR not supported 01: Post package repair supported, one row per bank group 10: Reserved 11: Reserved	Reserved; must be coded as 0

Byte 10 (0x00A):

Reserved, must be coded as 0x00

Byte 11 (0x00B): Module Nominal Voltage, VDD

This byte describes the Voltage Level for DRAM and other components on the module, such as the register or memory buffer, if applicable. Note that SPDs or thermal sensor components are on the VDDSPD supply and are not affected by this byte. Systems are required to parse this byte prior to applying power to the DRAMs to avoid damage to the module or to the system. Systems that do not support the required voltages must reject the module and must not apply power to the DRAMs.

'Operable' is defined as the VDD voltage at which module operation is allowed using the performance values programmed in the SPD.

'Endurant' is defined as the VDD voltage at which the module may be powered without adversely affecting the life expectancy or reliability. Operation is not supported at this voltage.

Byte 11: Module Nominal Voltage, VDD						
Reserved	DRAM VDD TBD2 V		DRAM VDD TBD1 V		DRAM VDD 1.2 V	
Bits 7~6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved; 00	0 = not endurant 1 = endurant	0 = not operable 1 = operable	0 = not endurant 1 = endurant	0 = not operable 1 = operable	0 = not endurant 1 = endurant	0 = not operable 1 = operable
Note 1 Systems are required to verify valid supply voltages before applying power to the DRAMs.						

Examples:

A value on bits 5~0 of 000011 defines DRAM support of a nominal operable voltage of 1.2 V only.

A value on bits 5~0 of 001111 defines DRAM support of a nominal operable voltage of TBD1 V or 1.2 V.

A value on bits 5~0 of 001110 defines DRAM support of a nominal operable voltage of TBD1 V but DRAMs are endurant at 1.2 V, while not operable at 1.2 V.

A value on bits 5~0 of 111000 defines DRAM support of a nominal operable voltage of TBD2 V, endurant but not operable at TBD1 V, and neither operable nor endurant at 1.2 V.

Byte 12 (0x00C): Module Organization

This byte describes the organization of the SDRAM module. Bits 2~0 encode the device width of the SDRAM devices. Bits 5~3 encode the number of package ranks on the module.

Bits 7~6	Bits 5~3	Bits 2~0
Reserved	Number of Package Ranks per DIMM	SDRAM Device Width
Reserved; 00	Bit [5, 4, 3] : 000 = 1 Package Rank 001 = 2 Package Ranks 010 = 3 Package Ranks 011 = 4 Package Ranks All others reserved	Bit [2, 1, 0] : 000 = 4 bits 001 = 8 bits 010 = 16 bits 011 = 32 bits All others reserved

“Package ranks per DIMM” refers to the collections of devices on the module sharing common chip select signals (across the data width of the DIMM), either from the edge connector for unbuffered modules or from the outputs of a registering clock driver for RDIMMs and LRDIMMs.

“Logical rank” refers the individually addressable die in a 3DS stack and has no meaning for monolithic or multi-load stacked SDRAMs; however, for the purposes of calculating the capacity of the module, one should treat monolithic and multi-load stack SDRAMs as having one logical rank per package rank.

SDRAM Package Type	# Package Ranks per DIMM	# Logical Ranks per Package Rank (for calculation only)	# Logical Ranks per DIMM
SDP	1	1	1
	2		2
DDP	2		2
	4		4
QDP	4		4
2H 3DS	1	2	2
	2		4
4H 3DS	1	4	4
	2		8
8H 3DS	1	8	8
	2		16
Logical Ranks per DIMM = # Package Ranks per DIMM * # Logical Ranks per Package Rank			

Byte 13 (0x00D): Module Memory Bus Width

This byte describes the width of the SDRAM memory bus on the module. Bits 2~0 encode the primary bus width. Bits 4~3 encode the bus extensions such as parity or ECC.

Bits 7~5	Bits 4~3	Bits 2~0
Reserved	Bus width extension, in bits	Primary bus width, in bits
00	Bit [4, 3] : 000 = 0 bits (no extension) 001 = 8 bits All others reserved	Bit [2, 1, 0] : 000 = 8 bits 001 = 16 bits 010 = 32 bits 011 = 64 bits All others reserved

Examples:

- 64 bit primary bus, no parity or ECC (64 bits total width): xxx 000 011
- 64 bit primary bus, with 8 bit ECC (72 bits total width): xxx 001 011

Calculating Module Capacity

The total memory capacity of the module may be calculated from SPD values. For example, to calculate the total capacity, in megabytes or gigabytes, of a typical module:

$$\text{Total} = \text{SDRAM Capacity} \div 8 * \text{Primary Bus Width} \div \text{SDRAM Width} * \text{Logical Ranks per DIMM}$$

where:

- SDRAM Capacity = SPD byte 4 bits 3~0
- Primary Bus Width = SPD byte 13 bits 2~0
- SDRAM Width = SPD byte 12 bits 2~0
- Logical Ranks per DIMM =

for SDP, DDP, QDP: = SPD byte 12 bits 5~3

for 3DS: = SPD byte 12 bits 5~3 times SPD byte 6 bits 6~4

Examples:

2 package ranks per DIMM using monolithic SDRAMs, 2 Gb per die, with x4 organization on a module with a 64 bit primary bus:

- Total = 2 Gb $\div$ 8 * 64 $\div$ 4 * 2 * 1 = 8 GB

2 package ranks per DIMM using DDP SDRAMs, 4 Gb per die, with x4 organization on a module with a 64 bit primary bus:

- $\text{Total} = 4 \text{ Gb} \div 8 * 64 \div 4 * 2 = 16 \text{ GB}$

2 package ranks per DIMM using 4H 3DS SDRAMs, 2 Gb per die, having a x8 organization on a module with a 64 bit primary bus:

- $\text{Total} = 2 \text{ Gb} \div 8 * 64 \div 8 * 2 * 4 = 16 \text{ GB}$

Commonly, parity or ECC are not counted in total module capacity, though they can also be included by adding the bus width extension in SPD byte 13 bits 4~3 to the primary bus width in the previous examples.

Byte 14 (0x00E): Module Thermal Sensor

This byte describes the module's supported thermal options.

Bit 7	Bits 6~0
Thermal Sensor ¹	Reserved
0 = Thermal sensor not incorporated onto this assembly 1 = Thermal sensor incorporated onto this assembly	0 = Undefined All others settings to be defined.
Note 1 Thermal sensor compliant with TSE2004av specifications.	

Bytes 15~16 (0x00F~0x010):

Reserved, must be coded as 0x00

Byte 17 (0x011): Timebases

This byte defines a value in picoseconds that represents the fundamental timebase for fine grain and medium grain timing calculations. These values are used as a multiplier for formulating subsequent timing parameters.

Bits 7~4	Bits 3~2	Bits 1~0
Reserved	Medium Timebase (MTB)	Fine Timebase (FTB)
Reserved; 0000	Bits [3, 2]: 00 = 125 ps All other values reserved	Bits [0, 1]: 00 = 1 ps All other values reserved

Relating the MTB and FTB

When a timing value tXX cannot be expressed by an integer number of MTB units, the SPD must be encoded using both the MTB and FTB. The Fine Offsets are encoded using a two's complement value which, when multiplied by the FTB yields a positive or negative correction factor. Typically, for safety and for legacy compatibility, the MTB portion is rounded UP and the FTB correction is a negative value. The general algorithm for programming SPD values is:

```

Temp_val = tXX / MTB           // Calculate as real number
Remainder = Temp_val modulo 1   // Determine if integer # MTBs
Fine_Correction = 1 - Remainder // If needed, what correction
if (Remainder == 0) then        // Integer # MTBs?
    tXX(MTB) = Temp_val         // Convert to integer
    tXX(FTB) = 0                // No correction needed
else                             // Needs correction
    tXX(MTB) = ceiling (Temp_val) // Round up for safety in legacy systems
    tXX(FTB) = Fine_Correction * MTB / FTB // Correction is negative offset
endif

```

To recalculate the value of tXX from the SPD values, a general formula BIOSes may use is:

$$tXX = tXX(MTB) * MTB + tXX(FTB) * FTB$$

Example:

t _{CKAVG} min SPD Calculations Using MTB and FTB			
Speed Bin	t _{CKAVG} min Value Decimal	SPD byte 18 Decimal (Hexadecimal)	SPD byte 125 Decimal (Hexadecimal)
DDR4-1866	1.071 ns	9 (0x09)	-54 (0xCA)
	=	(9 * 0.125) + (-54 * 0.001)	
Note 1 Examples assume MTB of 0.125 ns and FTB of 0.001 ns			

Timing parameters using both MTB and FTB are:

Table 2 — MTB and FTB Timing Parameters

Parameter	MTB Byte(s)	FTB Byte
$t_{CKAVGmin}$	18 (0x012)	125 (0x07D)
$t_{CKAVGmax}$	19 (0x013)	124 (0x07C)
t_{AAmin}	24 (0x018)	123 (0x07B)
t_{RCDmin}	25 (0x019)	122 (0x07A)
t_{Rpmin}	26 (0x01A)	121 (0x079)
t_{RCmin}	27, 29 (0x01B, 0x01D)	120 (0x078)
t_{RRD_Smin}	39 (0x027)	119 (0x077)
t_{RRD_Lmin}	40 (0x028)	118 (0x076)

The encoding of two's complement fine timebase offsets:

Coding		Value (Dec)	Value (Hex)	FTB Timebase
Bit 7	Bits 6~0			1 ps
0	1111111	+127	7F	+127 ps
0	1111110	+126	7E	+126 ps
...	...	...	...	
0	0000001	+1	01	+1 ps
0	0000000	0	00	0
1	1111111	-1	FF	-1 ps
1	1111110	-2	FE	-2 ps
...	...	...	...	
1	0000000	-128	80	-128 ps

Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33... MHz, or a clock period of 1.0714... ns. Similarly, a system with a memory clock frequency of 1066.66... MHz yields mathematically a clock period of 0.9375... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the SPD establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of memory module performance without violating device parameters. These algorithms rely on results that are within guardbands on device testing and specification to avoid losing performance due to rounding errors.

These rules are:

1. Clock periods such as t_{CKAVG_min} are rounded to the nearest picosecond of accuracy; for example, 0.9375... ns is rounded to 938 ps and 1.0714... ns is rounded to 1071 ps.
2. Parameters programmed in systems in numbers of clocks (nCK) but expressed in the SPD in units of time (ns or ps) are divided by the clock period, a guardband factor of 0.01 clocks is subtracted, then the result is rounded up to the nearest integer number of clocks. Examples:

DDR4 Bin	Parameter	Value	@ t_{CKAVG_min}	Temp Result	- Guardband	Rounding Result
		ps	ps	nCK	nCK	nCK
1600	$t_{RRD_L_min}$	7500	1250	6.000	5.990	6
1600	$t_{RRD_L_min}$	7500	1071	7.002	6.992	7
2133	$t_{RRD_L_min}$	6400	1250	5.120	5.110	6
1866	$t_{RRD_L_min}$	5300	1071	4.948	4.938	5

Byte 18 (0x012): SDRAM Minimum Cycle Time ($t_{CKAVGmin}$)

This byte defines the minimum cycle time for the SDRAM module, in medium timebase (MTB) units. This number applies to all applicable components on the module. This byte applies to SDRAM and support components as well as the overall capability of the DIMM. This value comes from the DDR4 SDRAM and support component data sheets.

Bits 7~0
Minimum SDRAM Cycle Time ($t_{CKAVGmin}$) MTB Units
Values defined from 1 to 255

If $t_{CKAVGmin}$ cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for $t_{CKAVGmin}$ (SPD byte 125) used for correction to get the actual value.

Examples:

$t_{CKAVGmin}$ (MTB units)		MTB (ns)	$t_{CKAVGmin}$ Offset (FTB units) ¹		FTB (ns)	$t_{CKAVGmin}$ Result (ns)	Use
10	0x0A	0.125	0	0	0.001	1.25	DDR4-1600 (800 MHz clock)
9	0x09	0.125	-54	0xCA	0.001	1.071	DDR4-1866 (933 MHz clock)
8	0x08	0.125	-63	0xC1	0.001	0.938	DDR4-2133 (1067 MHz clock)
7	0x07	0.125	-42	0xD6	0.001	0.833	DDR4-2400 (1200 MHz clock)
6	0x06	0.125	0	0	0.001	0.750	DDR4-2666 (1333 MHz clock)
5	0x05	0.125	0	0	0.001	0.625	DDR4-3200 (1600 MHz clock)

Note 1 See SPD byte 125.

Byte 19 (0x013): SDRAM Maximum Cycle Time ($t_{CKAVGmax}$)

This word defines the maximum cycle time for the SDRAM module, in medium timebase (MTB) units. This number applies to all applicable components on the module. This byte applies to SDRAM and support components as well as the overall capability of the DIMM. This value comes from the DDR4 SDRAM and support component data sheets.

Bits 7~0	
Minimum SDRAM Cycle Time ($t_{CKAVGmax}$)	
MTB Units	
Values defined from 1 to 255	

If $t_{CKAVGmax}$ cannot be divided evenly by the MTB, this byte must be rounded up to the next larger integer and the Fine Offset for $t_{CKAVGmax}$ (SPD byte 124) used for correction to get the actual value.

Examples:

$t_{CKAVGmax}$ (MTB units)		MTB (ns)	$t_{CKAVGmax}$ Offset (FTB units) ¹		FTB (ns)	$t_{CKAVGmax}$ Result (ns)	Use
12	0x0C	0.125	0	0	0.001	1.500	DDR4-1600 (800 MHz clock)
12	0x0C	0.125	0	0	0.001	1.500	DDR4-1866 (933 MHz clock)
12	0x0C	0.125	0	0	0.001	1.500	DDR4-2133 (1067 MHz clock)
12	0x0C	0.125	0	0	0.001	1.500	DDR4-2400 (1200 MHz clock)
		0.125			0.001	tbd	DDR4-2666 (1333 MHz clock)
		0.125			0.001	tbd	DDR4-3200 (1600 MHz clock)

Note 1 See SPD byte 124.

Byte 20 (0x014): CAS Latencies Supported, First Byte

Byte 21 (0x015): CAS Latencies Supported, Second Byte

Byte 22 (0x016): CAS Latencies Supported, Third Byte

Byte 23 (0x017): CAS Latencies Supported, Fourth Byte

These bytes define which CAS Latency (CL) values are supported. The range is from CL = 7 through CL = 24 with one bit per possible CAS Latency. A 1 in a bit position means that CL is supported, a 0 in that bit position means it is not supported. These values come from the DDR4 SDRAM data sheet, JESD79-4.

Byte 20: CAS Latencies Supported, First Byte							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CL = 14	CL = 13	CL = 12	CL = 11	CL = 10	CL = 9	CL = 8	CL = 7
0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Byte 21: CAS Latencies Supported, Second Byte							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CL = 22	CL = 21	CL = 20	CL = 19	CL = 18	CL = 17	CL = 16	CL = 15
0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1	0 or 1
Byte 22: CAS Latencies Supported, Third Byte							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CL = 24	CL = 23
0	0	0	0	0	0	0 or 1	0 or 1
Byte 23: CAS Latencies Supported, Fourth Byte							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0	0	0	0	0	0	0	0

For each bit position, 0 means this CAS Latency is not supported, 1 means this CAS Latency is supported.

Example:

Byte 20 = 0xB4 (= 1011 0100) -- first byte

Byte 21 = 0x05 (= 0000 0101) -- second byte

Byte 22 = 0x00 (= 0000 0000) -- third byte

Byte 23 = 0x00 (= 0000 0000) -- fourth byte

CAS Latencies	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7
CL Mask	0	0	0	0	0	1	0	1	1	0	1	1	0	1	0	0
CAS Latencies	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	24	23
CL Mask	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Results: Actual CAS Latencies supported = 9, 11, 12, 14, 15, 17