JESD 21-C Section Title: Annex M: Serial Presence Detect (SPD) for LPDDR3 and LPDDR4 SDRAM Modules
Committee Document Reference Title: LPDDR3 and LPDDR4 SPD Document Release 1
Device Type Identifier: LP-DIMM Revision 1.0

1 Scope

This Annex describes the serial presence detect (SPD) values for all LPDDR modules. Differences between module types are encapsulated in subsections of this annex. These presence detect values are those referenced in the SPD standard document for 'Specific Features'. The following SPD fields will be documented in the order presented in Section 2, with the exception of bytes 128~255 which are documented in separate sections, one for each family of module types. Further description of Byte 2 is found in Annex A of the SPD standard.

All unused entries will be coded as 0x00. All unused bits in defined bytes will be coded as 0 except where noted.

Timing parameters in the SPD represent the operation of the module including all Drams and support devices at the lowest supported supply voltage (see SPD byte 11), and are valid from t_{CKAVG}min to t_{CKAVG}max (see SPD bytes 18 and 19).

To allow for maximum flexibility as devices evolve, SPD fields described in this document may support device configuration and timing options that are not included in the JEDEC LPDDR SDRAM data sheet (JESD79-4). Please refer to DRAM supplier data sheets or JESD79-4 to determine the compatibility of components.

2 Address map

The following is the SPD address map for all LPDDR modules. It describes where the individual lookup table entries will be held in the serial EEPROM. Consistent with the definition of LPDDR generation SPD devices which have four individual write protection blocks of 128 bytes in length each, the SPD contents are aligned with these blocks as shown in Table 1.

Table 1 — Address Map

Block	Range		Description
0	0~127	0x000~0x07F	Base Configuration and DRAM Parameters
1	128~255	0x080~0x0FF	Module Specific Parameters -- See annexes for details
2	256~319	0x100~0x13F	Hybrid Memory Parameters
	320~383	0x140~0x17F	Manufacturing Information
3	384~511	0x180~0x1FF	End User Programmable

2.1 Block Descriptions

2.1.1 Block 0: Base Configuration and DRAM Parameters

Table 2 details the location of each byte in this block.

Table 2 — Block 0: Base Configuration and DRAM Parameters

Byte Number		Function Described	Notes
0	0x000	Number of Serial PD Bytes Written / SPD Device Size	1, 2
1	0x001	SPD Revision	
2	0x002	Key Byte / DRAM Device Type	
3	0x003	Key Byte / Module Type	
4	0x004	SDRAM Density and Banks	3
5	0x005	SDRAM Addressing	3

NOTE 1 Number of SPD bytes written will typically be programmed as 384 bytes.
NOTE 2 Size of SPD device will typically be programmed as 512 bytes.
NOTE 3 From LPDDR SDRAM data sheet.
NOTE 4 These are optional, in accordance with the JEDEC specification.

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2 Address Map (Cont'd)
2.1 Block Descriptions (Cont'd)

Table 2 — Block 0: Base Configuration and DRAM Parameters (Cont'd)

Byte Number		Function Described	Notes
6	0x006	SDRAM Package Type	3
7	0x007	SDRAM Optional Features	3
8	0x008	SDRAM Thermal and Refresh Options	3
9	0x009	Other SDRAM Optional Features	3
10	0x00A	Reserved -- must be coded as 0x00	
11	0x00B	Module Nominal Voltage, VDD	3
12	0x00C	Module Organization	
13	0x00D	Bus Width	
14	0x00E	Module Thermal Sensor	
15	0x00F	Extended module type	
16	0x010	Signal Loading	3
17	0x011	Timebases	
18	0x012	SDRAM Minimum Cycle Time (t_{CKAVG}min)	3
19	0x013	SDRAM Maximum Cycle Time (t_{CKAVG}max)	3
20	0x014	CAS Latencies Supported, First Byte	3
21	0x015	CAS Latencies Supported, Second Byte	3
22	0x016	CAS Latencies Supported, Third Byte	3
23	0x017	CAS Latencies Supported, Fourth Byte	3
24	0x018	Minimum CAS Latency Time (t_{AA}min)	3
25	0x019	Read & Write Latency Set Options	
26	0x01A	Minimum RAS to CAS Delay Time (t_{RCD}min)	3
27	0x01B	Minimum Row Precharge Delay Time (t_{RPab}min)	3
28	0x01C	Minimum Row Precharge Delay Time (t_{RPpb}min)	
29	0x01D	Minimum Refresh Recovery Delay Time (t_{RFCab}min), LSB	3
30	0x01E	Minimum Refresh Recovery Delay Time (t_{RFCab}min), MSB	3
31	0x01F	Minimum Refresh Recovery Delay Time (t_{RFCpb}min), LSB	3
32	0x020	Minimum Refresh Recovery Delay Time (t_{RFCpb}min), MSB	3
33~59	0x029~0x03B	Reserved -- must be coded as 0x00	
60~77	0x03C~0x04D	Connector to SDRAM Bit Mapping	
78~119	0x04E~0x074	Reserved -- must be coded as 0x00	
120	0x078	Fine Offset for Minimum Row Precharge Delay Time (t_{RPpb}min)	3
121	0x079	Fine Offset for Minimum Row Precharge Delay Time (t_{RPab}min)	3
122	0x07A	Fine Offset for Minimum RAS to CAS Delay Time (t_{RCD}min)	3
123	0x07B	Fine Offset for Minimum CAS Latency Time (t_{AA}min)	3
124	0x07C	Fine Offset for SDRAM Maximum Cycle Time (t_{CKAVG}max)	3
125	0x07D	Fine Offset for SDRAM Minimum Cycle Time (t_{CKAVG}min)	3
126	0x07E	CRC for Base Configuration Section, Least Significant Byte	
127	0x07F	CRC for Base Configuration Section, Most Significant Byte	

NOTE 1 Number of SPD bytes written will typically be programmed as 384 bytes.
NOTE 2 Size of SPD device will typically be programmed as 512 bytes.
NOTE 3 From LPDDR SDRAM data sheet.
NOTE 4 These are optional, in accordance with the JEDEC specification.

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2.1.2 Block 1: Module Specific Parameters

Bytes 128~255 (0x080~0x0FF). Parameters in this block are specific to the module type as selected by the contents of SPD Key Byte 3 bits 3~0. Refer to the appropriate annex for detailed byte descriptions.

2.1.3 Block 2, lower half: Hybrid Memory Parameters

Bytes 256~319 (0x100~0x13F). Parameters in this block are specific to the hybrid memory type as selected by the contents of SPD Key Byte 3 bits 7~4. Refer to the appropriate annex for detailed byte descriptions.

2.1.4 Block 2, upper half: Manufacturing Information

Bytes 320~383 (0x140~0x17F). Table 3 details the location of each byte in this block.

Table 3 — Block 2, upper half: Manufacturing Information

Byte Number		Function Described	Notes
320	0x140	Module Manufacturer's ID Code, Least Significant Byte	
321	0x141	Module Manufacturer's ID Code, Most Significant Byte	
322	0x142	Module Manufacturing Location	
323~324	0x143~0x144	Module Manufacturing Date	
325~328	0x145~0x148	Module Serial Number	
329~348	0x149~0x15C	Module Part Number	
349	0x15D	Module Revision Code	
350	0x15E	DRAM Manufacturer's ID Code, Least Significant Byte	
351	0x15F	DRAM Manufacturer's ID Code, Most Significant Byte	
352	0x160	DRAM Stepping	
353~381	0x161~0x17D	Module Manufacturer's Specific Data	
382~383	0x17E~0x17F	Reserved; must be coded as 0x00	

2.1.5 Block 3: End User Programmable

Bytes 384~511 (0x180~0x1FF) Bytes in this block are reserved for use by end users.

3 Details of Each Byte

3.1 General Configuration Section: Bytes 0~127 (0x000~0x07F)

This section contains defines parameters that are common to all LPDDR module types.

3.1.1 Byte 0 (0x000): Number of Bytes Used / Number of Bytes in SPD Device

Byte 0 (0x000) is shown in Table 4. The least significant nibble of this byte describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data. Bits 6~4 describe the total size of the serial memory used to hold the Serial Presence Detect data

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Table 4 — Byte 0 (0x000): Number of Bytes Used / Number of Bytes in SPD Device

Bit 7	Bits 6~4	Bits 3~0
Reserved	**SPD Bytes Total**	**SPD Bytes Used**
Reserved; must be coded as 0	Bit [6, 5, 4] : 000 = Undefined 001 = 256 010 = 512 All others reserved	Bit [3, 2, 1, 0] : 0000 = Undefined 0001 = 128 0010 = 256 0011 = 384 0100 = 512 All others reserved

NOTE Typical programming of bits 3~0 will be 0011 (384 bytes).

3.1.2 Byte 1 (0x001): SPD Revision

This byte, shown in Table 5, describes the compatibility level of the encoding of the bytes contained in the SPD EEPROM, and the current collection of valid defined bytes. Software should examine the upper nibble (Encoding Level) to determine if it can correctly interpret the contents of the module SPD. The lower nibble (Additions Level) can optionally be used to determine which additional bytes or attribute bits have been defined; however, since any undefined additional byte must be encoded as 0x00 or undefined attribute bit must be defined as 0, software can safely detect additional bytes and use safe defaults if a zero encoding is read for these bytes.

Table 5 — Byte 1 (0x001): SPD Revision

Production Status	SPD Revision	Encoding Level				Additions Level				Hex
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Pre-production	Revision 0.0	0	0	0	0	0	0	0	0	00
	Revision 0.1	0	0	0	0	0	0	0	1	01
	...	.	.	.	.	.	.	.	.	.
	Revision 0.9	0	0	0	0	1	0	0	1	09
Production	Revision 1.0	0	0	0	1	0	0	0	0	10
	Revision 1.1	0	0	0	1	0	0	0	1	11
	...	.	.	.	.	.	.	.	.	...
Undefined	Undefined	1	1	1	1	1	1	1	1	FF

The Additions Level is never reduced even after an increment of the Encoding Level. For example, if the current SPD revision level were 1.2 and a change in Encoding Level were approved, the next revision level would be 2.2. If additions to revision 2.2 were approved, the next revision would be 2.3. Changes in the Encoding Level are extremely rare, however, since they can create incompatibilities with older systems.

The exceptions to the above rule are the SPD revision levels used during development prior to the Revision 1.0 release. Revisions 0.0 through 0.9 are used to indicate sequential pre-production SPD revision levels, however the first production release will be Revision 1.0.

This document allows for SPD contents for multiple families of LPDDR memory modules, with a separate annex for each family that defines the bytes in SPD locations 128~255 (0x080~0x0FF). These module families and their respective appendices are:

- Annex M.1: LP-DIMM Memory Modules
- (at this time, no other LPDDR module families are defined)

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The SPD revision level for each module family type is independent. This allows changes to be made to a new module family annex, for example, without necessarily changing the revision of LP-DIMMs. In this context, the SPD revision value corresponds to all SPD bytes *for that DIMM type*. It also means that over time, the revisions for each module type may vary. Note that changes to a DIMM specific annex does not affect the revisions of other module types, but changes in the General Section of the SPD affect all DIMM types. The example in Table 6 suggests a possible historical progression:

Table 6 — Hypothetical Historic Progression of SPD Revisions by DIMM Type

Event	LP-DIMM
Pre-standard SPD release	0.5
Initial SPD release	1.0
SPD additions made	1.1
SPD encoding change made	2.1

3.1.3 Byte 2 (0x002): Key Byte / DRAM Device Type

This byte, shown in Table 7, is the key byte used by the system BIOS to determine how to interpret all other bytes in the SPD EEPROM. The BIOS must check this byte first to ensure that the EEPROM data is interpreted correctly. Any DRAM or Module type that requires significant changes to the SPD format (beyond defining previously undefined bytes or bits) also requires a new entry in the key byte table below.

Table 7 — Byte 2 (0x002): Key Byte / DRAM Device Type

Line #	Hex	SDRAM / Module Type Corresponding to Key Byte
0	00	Reserved
1	01	Fast Page Mode
2	02	EDO
3	03	Pipelined Nibble
4	04	SDRAM
5	05	ROM
6	06	DDR SGRAM
7	07	DDR SDRAM
8	08	DDR2 SDRAM
9	09	DDR2 SDRAM FB-DIMM
10	0A	DDR2 SDRAM FB-DIMM PROBE
11	0B	DDR3 SDRAM
12	0C	DDR4 SDRAM
13	0D	Reserved
14	0E	DDR4E SDRAM
15	0F	LPDDR3 SDRAM
16	10	LPDDR4 SDRAM
-	-	-
253	FD	Reserved
254	FE	Reserved
255	FF	Reserved

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The DRAM Device Type byte defines an interface compatibility family more than it identifies a specific memory device. For example, where an LP memory module may expose the devices directly to the edge connector contacts, a load reduced memory module presents the interfaces of registering clock drivers and data buffers to the edge connector contacts. There may be memory modules with completely different devices, such as non-volatile memories, however these may define themselves as a base memory type such as LPDDR SDRAM for interface compatibility with the memory controller. The memory controller must be aware of its capabilities when parsing the SPD.

3.1.4 Byte 3 (0x003): Key Byte / Module Type

This byte, shown in Table 8, is a Key Byte used to index the module specific section of the SPD from bytes 128~255 and bytes 256~319. Byte 3 bits 3~0 identifies the SDRAM memory module type.

Bits 7~4 identifies the architecture of the secondary memory type, if any, present on the module in addition to the base DRAM. These secondary hybrid architectures may apply to any Base Module Type. The index in bits 7~4 is used to index the hybrid memory architecture specific section of the SPD from bytes 256~319.

System software supporting hybrid memory modules should parse the DRAM attributes per the Base Module Type and combine the indexed information per the Hybrid Memory Type to determine the combined memory module capabilities.

Where base memory parameters apply to this class of hybrid module, these will be documented with those bytes in the base section. Extended parameters are encoded in SPD bytes 256~319. When a module has no base memory present, the special coding 1111 shall be used in bits 3~0 of byte 2.

Table 8 — Byte 3 (0x003): Key Byte / Module Type

Bit 7	Bits 6~4	Bits 3~0
Hybrid	**Hybrid Media**	**Base Module Type**
0 = Not hybrid (Module is DRAM only) 1 = Hybrid module (See bits 6~4 for hybrid type)	Bits [6, 5, 4]: 000 = Not hybrid 001 = Reserved All other codes reserved	Bits [3, 2, 1, 0]: 0000 = Extended DIMM type, see byte 15 (0x00F) 0111 = LP-DIMM 1110 = Non-DIMM Solution 1111 = Reserved
Base Module Type Definitions: LP-DIMM: Low Power Unbuffered Small Outline Dual In-Line Memory Module, 64-bit data bus Non-DIMM Solution: Used to define when the SDRAM Devices may be placed on the main board rather than on a module. NOTE No hybrid LPDDR compatible modules are defined at this time.		

Examples:

0x07 = LP-DIMM, no hybrid memory present

0x0E = soldered down memory, no hybrid memory present

NOTE LP-DIMMs incorporate two independent 32 bit channels per module. Non-DIMM solutions such as solder down applications may incorporate any number of channels, yet use SPD codes to simplify software configuration for the application.

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3.1.5 Byte 4 (0x004): SDRAM Density and Banks

This byte, shown in Table 9, defines the total density of each LPDDR SDRAM, in bits, and the number of internal banks and bank groups into which the memory array is divided. These values come from the LPDDR SDRAM data sheet.

Table 9 — Byte 4 (0x004): SDRAM Density and Banks

Bits 7~6	Bits 5~4	Bits 3~0
Bank Group Bits	**Bank Address Bits[1]**	**Total SDRAM capacity, per die, in Gigabits**
Bits [7, 6]: 00 = 0 (no bank groups) 01 = 1 (2 bank groups) 10 = 2 (4 bank groups) 11 = reserved	Bit [5, 4] : 00 = 2 (4 banks) 01 = 3 (8 banks) All others reserved	Bit [3, 2, 1, 0] : 0000 = Reserved 0001 = Reserved 0010 = 1 Gb 0011 = 2 Gb 0100 = 4 Gb 0101 = 8 Gb 0110 = 16 Gb 0111 = 32 Gb 1000 = 12 Gb 1001 = 24 Gb 1010 = 3 Gb 1011 = 6 Gb 1100 = 18 Gb All others reserved

3.1.6 Byte 5 (0x005): SDRAM Addressing

This byte, shown in Table 10, describes the row addressing and the column addressing in each SDRAM device. Bits 2~0 encode the number of column address bits, and bits 5~3 encode the number of row address bits. These values come from the LPDDR SDRAM data sheet.

Table 10 — Byte 5 (0x005): SDRAM Addressing

Bits 7~6	Bits 5~3	Bits 2~0
Reserved	**Row Address Bits**	**Column Address Bits**
Reserved; must be coded as 00	Bit [5, 4, 3] : 000 = 12 001 = 13 010 = 14 011 = 15 100 = 16 101 = 17 110 = 18 All others reserved	Bit [2, 1, 0] : 000 = 9 001 = 10 010 = 11 011 = 12 All others reserved

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3.1.7 Byte 6 (0x006): SDRAM Package Type

This byte, shown in Table 11, describes the type of SDRAM Device on the module.

Table 11 — Byte 6 (0x006): SDRAM Package Type

Bit 7	Bits 6~4	Bits 3~2	Bit 1~0
SDRAM Package Type	**Die per SDRAM Package**	**Channels per SDRAM Package**	**Signal Loading Index[2]**
0 = Monolithic DRAM Device 1 = Non-Monolithic Device[1]	000 = 1 die 001 = 2 die 010 = 3 die 011 = 4 die 100 = 5 die 101 = 6 die 110 = 7 die 111 = 8 die All others reserved.	00 = 1 Channel 01 = 2 Channels 10 = 4 Channels 11 = Reserved	00 = Not specified 01 = Byte 16 Signal Loading Matrix 1 10 = Reserved 11 = Byte 16 Signal Loading Matrix 2

NOTE 1 This includes Dual Die, Quad Die, Multi-Die, or physically stacked devices - anything that is outside the standard monolithic device
NOTE 2 Index into SPD byte 16, Signal Loading. Selects one matrix of signal loads.
NOTE 3 Monolithic devices (bit 7 = 0) should code bits 1~0 as 00.

3.1.8 Byte 7 (0x007): SDRAM Optional Features

This byte, shown in Table 12, defines support for certain SDRAM features. This value comes from the LPDDR SDRAM data sheet.

Table 12 — Byte 7 (0x007): SDRAM Optional Features

Bits 7~6	Bits 5~4	Bits 3~0
Reserved	**Maximum Activate Window (tMAW)**	**Maximum Activate Count (MAC)**
Reserved; must be coded as 00	Bits [5, 4]: 00 = 8192 * tREFI 01 = 4096 * tREFI 10 = 2048 * tREFI 11 = Reserved	Bits [3, 2, 1, 0] : 0000 = Untested MAC[1] 0001 = 700 K 0010 = 600 K 0011 = 500 K 0100 = 400 K 0101 = 300 K 0110 = 200 K 0111 = Reserved 1000 = Unlimited MAC[2] All others reserved

NOTE 1 Untested MAC means the device is not tested for tMAW and/or MAC; no particular value should be assumed.
NOTE 2 Unlimited MAC means there is no restriction to the number of activates to a given row in a refresh period providing DRAM timing requirements such as tRCmin and refresh requirements are not violated.

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3.1.9 Byte 8 (0x008): SDRAM Thermal and Refresh Options

This byte, shown in Table 13, describes the module's supported operating temperature ranges and refresh options. These values come from the LPDDR SDRAM data sheet. Please refer to the LPDDR SDRAM data sheet (JESD79-4 or supplier data sheet) for a complete description of these options.

Table 13 — Byte 8 (0x008): SDRAM Thermal and Refresh Options

Bits 7~0
Reserved
Reserved; must be coded as 0x00

3.1.10 Byte 9 (0x009): Other SDRAM Optional Features

This byte, shown in Table 14, defines support for certain SDRAM features. This value comes from the LPDDR SDRAM data sheet.

Table 14 — Byte 9 (0x009): Other SDRAM Optional Features

Bits 7~6	Bit 5	Bits 4~0
Post Package Repair (PPR)	**Soft PPR**	**Reserved**
00: PPR not supported 01: Post package repair supported, one row per bank group 10: Reserved 11: Reserved	0 = Soft PPR not supported 1 = Soft PPR supported	Reserved; must be coded as 00000

3.1.11 Byte 10 (0x00A):

Reserved, must be coded as 0x00

3.1.12 Byte 11 (0x00B): Module Nominal Voltage, VDD

Reserved, must be coded as 0x00

3.1.13 Byte 12 (0x00C): Module Organization

This byte, shown in Table 15, describes the organization of the SDRAM module. Bits 2~0 encode the device width of the SDRAM devices. Bits 5~3 encode the number of package ranks on the module.

Table 15 — Byte 12 (0x00C): Module Organization

Bits 7~6	Bits 5~3	Bits 2~0
Reserved	**Package Ranks per Channel**	**Device Data Width**
Reserved; must be coded as 00	Bit [5, 4, 3] : 000 = 1 Package Rank 001 = 2 Package Ranks 010 = 3 Package Ranks 011 = 4 Package Ranks All others reserved	Bit [2, 1, 0] : 000 = 4 bits 001 = 8 bits 010 = 16 bits 011 = 32 bits All others reserved

"Package ranks per channel" refers to the number of common chip select signals across the data width of the channel such that assertion of each chip select enables a number of DRAM devices equivalent to the width of the channel.
LP-DIMMs incorporate two independent channels per module, each with a unique set of chip selects; bits 5~3 represent the number of chip selects on each channel.

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3.1.14 Byte 13 (0x00D): Bus Width

This byte, shown in Table 16, describes the width of the SDRAM memory bus for each channel. Bits 2~0 encode the primary bus width. Bits 4~3 encode the bus width extension such as parity or ECC (not currently supported for LPDDR solutions). Bits 7~5 describe the number of LPDDR channels represented by this SPD.

Table 16 — Byte 13 (0x00D): Bus Width

Bits 7~5	Bits 4~3	Bits 2~0
Number of Channels[2]	**Bus Width Extension[1], in bits**	**Channel Bus Width[2], in bits**
Bits [7, 6, 5]: 000 = 1 channel 001 = 2 channels 010 = 3 channels 011 = 4 channels All others reserved	Bit [4, 3] : 00 = 0 bits (no extension) 01 = Reserved All others reserved	Bit [2, 1, 0] : 000 = 8 bits 001 = 16 bits 010 = 32 bits 011 = 64 bits All others reserved

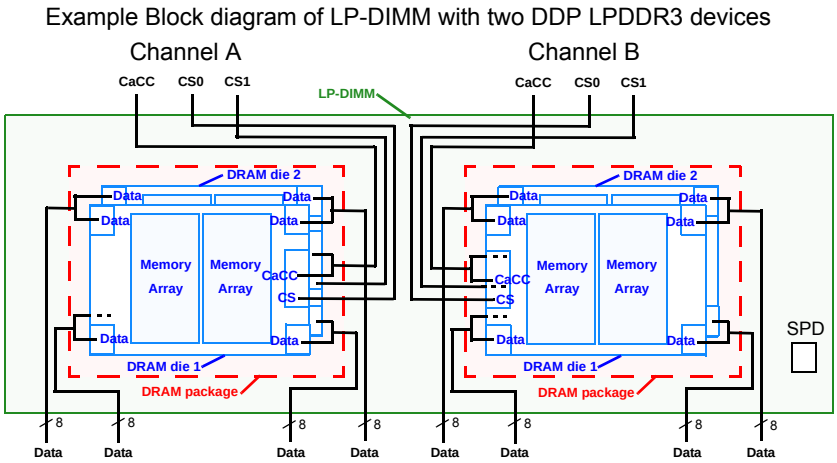
NOTE 1 LPDDR modules have no ECC option defined.
NOTE 2 Standard LP-DIMMs define two 32 bit wide channels per module.
NOTE 3 Solution width (e.g., DIMM width) = (Channel Bus Width + Bus Width Extension) * Number of Channels

Examples:

- One 32 bit channel, no parity or ECC (32 bits total width): 000 000 010
- Two 32 bit channels, no parity or ECC (64 bits total width): 001 000 010
- One 64 bit channel, no parity or ECC (64 bits total width): 000 000 011

3.1.14.1 Calculating Total Solution Capacity

The LPDDR SPD supports solder down or module solutions, so calculating total solution capacity combines calculating the per-channel capacity multiplied by the number of channels. The SPD assumes that all channels have equivalent capacity and configuration. JEDEC standard LPDDR memory modules have two 32-bit channels, so the configuration of such modules is used to describe the terminology used to calculate module capacity, as shown in Figures 1 and 2.



Number of die per package = 2
Number of chip selects per channel = 2
Number of package ranks per channel = 2
SDRAM device width = 32
Channel bus width = 32
Number of channels = 2

CaCC = Command, address, control, clocks
CS = chip select

Figure 1 — Example Block Diagram of LP-DIMM with two DDP LPDDR3 Devices

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