

4.1.4 Definition of the TSE2002av Serial Presence Detect (SPD) EEPROM with Temperature Sensor (TS) for Memory Module Applications

1. SCOPE

This standard defines the specifications of interface parameters, signaling protocols, and features for Serial Presence Detect (SPD) EEPROMs and Temperature Sensor (TS) as used for memory module applications. The designation TSE2002av refers to the family of devices specified by this document.

The purpose is to provide a standard for the TSE2002av SPD + TS devices for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE: The designation TSE2002av refers to the part of the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2. DEVICE STANDARD

2.1 Description

The TSE2002av is a combination 256-byte EEPROM and Temperature Sensor device designed to operate in one of three voltage ranges, 1.7-3.6 V, 2.3-3.6 V, or 3.0-3.6 V. All devices meet the thermal performance characteristics, and the 2.3-3.6 V or 3.0-3.3 V nominal devices shall operate the I²C bus at a 400 kHz maximum. Both devices are intended to interface to I²C buses which have multiple devices on a shared bus, and must be uniquely addressed on this bus. A substantial reduction in supply current may be achieved using the software programmed shutdown mode. The device family contains two temperature grades designated with a second letter appended to the part number.

Common Features summary:

TSE2002av Variations						
Base part number		a	Sensor Accuracy		v	Single Supply Voltage
TSE2002		B	0.5 °C typ from 75-95 °C		1	1.7 to 3.6 V
			1.0 °C typ from 40-125 °C		2	2.3 to 3.6 V
			2.0 °C typ from -20-125 °C		3	3.0 to 3.6 V
		C	1.0 °C typ from 75-95 °C			
			2.0 °C typ from 40-125 °C			
			3.0 °C typ from -20-125 °C			
Example: TSE2002C2 is an SPD with Thermal Sensor having 1.0 °C typical accuracy from 75-95 °C and a single supply voltage range from 2.3 to 3.6 V.						

- Low operating current:
 - < 100 uA maximum with SPD in Standby and TS in Shutdown mode
 - ~1 mA typical with SPD in Standby mode and TS active
 - ~2 mA typical with TS and SPD enabled at 3.3 V input
- Two Wire I²C Serial Interface
- Up to 100 kHz Transfer Rate below 2.2 V
- Up to 400 kHz Transfer Rate at or above 2.2 V
- Packages: TSSOP-8, Thermally Enhanced TSSOP-8 (MO-187), PSON-8, SOIC-8, MSOP-8,

SPD Features summary:

- Permanent and Reversible Software Data Protection for Lower 128 Bytes
- Byte and Page (up to 16 Bytes) Write Operation
- Random and Sequential Read modes
- Self-Timed Write Cycle
- Schmitt trigger on bus inputs
- Noise filter on bus inputs
- Automatic Address Incrementing

TS Features summary:

- Typical accuracy of 1.0 °C accuracy for the active range from 70 ~ 95 °C
- Typical accuracy of 2.0 °C for other monitor ranges from 40 ~ 125 °C
- Support for higher accuracy of 0.5 °C (typical) over the active range, where available
- Ambient temperature (TA) sense through an operating range of -20 to +125 °C
- Temperature sample rate minimum of 8 samples/s
- Selectable 0, 1.5 °C, 3 °C, 6 °C Hysteresis on set point

The SPD section of the TSE2002av is a 2 Kbit serial EEPROM organized as a 256 byte memory. The device is able to lock permanently the data in the lower sector (from location 0x00 to 0x7F), designed specifically for use in DRAM DIMMs (Dual Inline Memory Modules) with Serial Presence Detect. All the information concerning the DRAM module configuration (such as its access speed, its size, its organization) can be kept write protected in the first half of the memory.

Locking the lower sector of the SPD may be accomplished using one of two software write protection mechanisms. By sending the device a specific I²C sequence, the first 128 bytes of the memory become write protected, either permanently or resettable.

The TS section of the TSE2002av continuously monitors the temperature and updates the temperature data minimum of eight times per second. Temperature data is latched internally by the device and may be read by software from the bus host at any time.

Internal registers are used to configure both the TS performance and response to over-temperature conditions. The device contains programmable high, low, and critical temperature limits. Finally, the device EVENT# pin can be configured as active high or active low and can be configured to operate as an interrupt or as a comparator output.

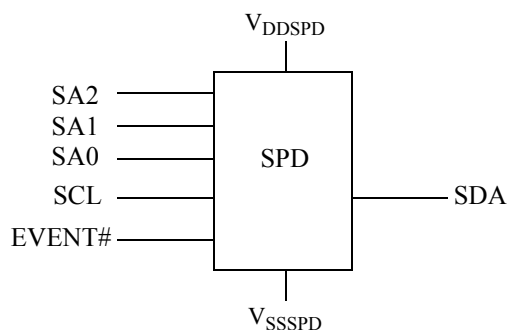


Figure 1 — Device Diagram

2.2 Device Interface

The TSE2002av behaves as a slave device in the I²C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and R/W# bit (as described in Table 2 on page 5), terminated by an acknowledge bit. TSE2002av family devices shall not initiate clock stretching, which is an optional I²C bus feature.

In accordance with the I²C bus definition, the device uses three (3) built-in, 4-bit Device Type Identifier Codes (DTIC) and the state of SA0, SA1, and SA2 to generate an I²C Slave Address. The SPD memory may be accessed using a DTIC of (1010), and to perform the PSWP, CSWP, or PSWP operations a DTIC of (0110) is required. The TS registers are accessed using a DTIC of (0011).

When writing data to the memory, the SPD inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Bus Master generated STOP condition after an Ack for WRITE, and after a NoAck for READ.

The TS section of the device uses a pointer register to access all registers in the device. Additionally, all data transfers to and from this section of the device are performed as block read/write operations. The data is transmitted/received as 2 bytes, Most Significant Byte (MSB) first, and terminated with a NoAck and STOP after the Least Significant byte (LSB). Data and address information is transmitted and received Most Significant Bit first

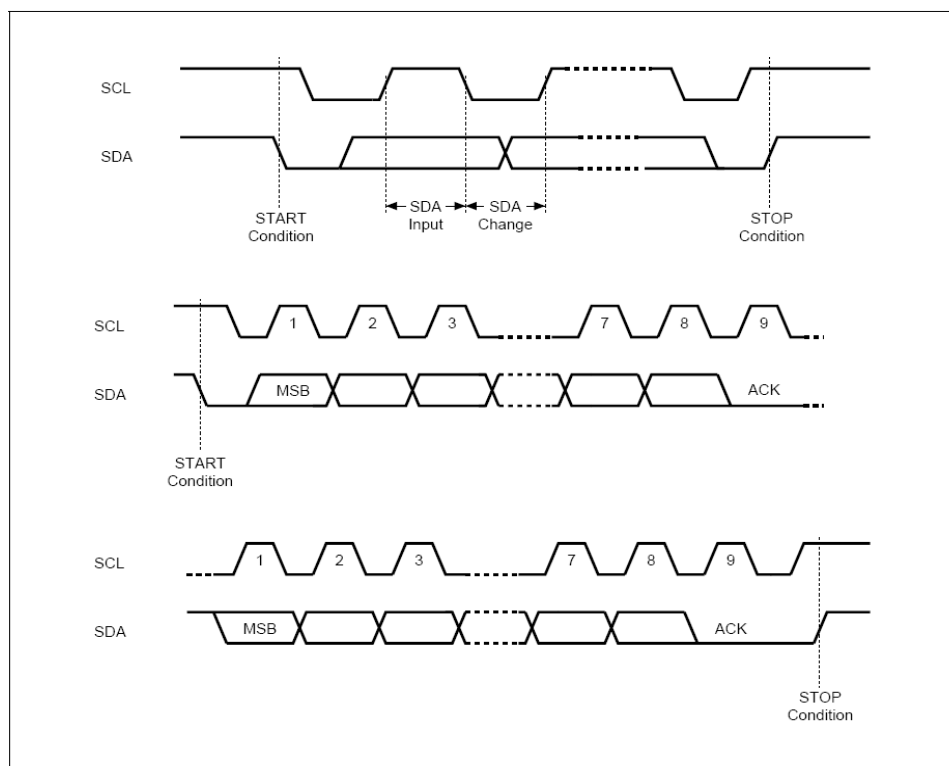


Figure 2 — I²C Bus Protocol

Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

Stop Condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the SPD into Standby mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle for the SPD. Neither of these conditions changes the operation of the TS section.

Acknowledge Bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

No Acknowledge Bit (NACK)

The no-acknowledge bit is used to indicate the completion of a block read operation, or an attempt to modify a write-protected register. The bus master releases Serial Data (SDA) after sending eight bits of data, and during the 9th clock pulse period, and does not pull Serial Data (SDA) Low.

Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change only when Serial Clock (SCL) is driven Low.

Memory Addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in Table 1 on page 5 (on Serial Data (SDA), most significant bit first).

Table 1 — Device Select Code

Memory Area Function	Device Type Identifier				Select Address Signals			R/W#	SA0 Pin
	b7 ¹	b6	b5	b4	b3	b2	b1	b0	
Read/Write SPD memory	1	0	1	0	SA2	SA1	SA0	R/W#	0 or 1
Set Reversible Write Protection (SWP)	0	1	1	0	0	0	1	0	V _{HV}
Clear Reversible Write Protection (CWP)					0	1	1	0	V _{HV}
Read Reversible Write Protection Status					0	0	1	1	V _{HV}
Permanently Set Write Protection (PSWP) ²					SA2	SA1	SA0	0	0 or 1
Read Permanent Write Protection Status ²					SA2	SA1	SA0	1	0 or 1
Read/Write Temperature registers	0	0	1	1	SA2	SA1	SA0	R/W#	0 or 1
Note 1: The most significant bit, b7, is sent first. Note 2: SA0, SA1, and SA2 are compared against the respective external pins on the TSE2002av. Note 3: 0 = V _{SSSPD} , 1 = V _{DDSPD} , V _{HV} = High Voltage									

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Select Address (SA2, SA1, SA0). To address the memory array, the 4-bit Device Type Identifier is 1010b; to access the write-protection settings, it is 0110b; and to access the Temperature Sensor settings is 0011b. Additionally, reading or writing the reversible write protect requires that SA0 be raised to the V_{HV} voltage level; setting the permanent write protect may be done with SA0 at either V_{SSSPD} or V_{DDSPD} levels.

Up to eight memory devices can be connected on a single I²C bus. Each one is given a unique 3-bit code on the Chip Enable (SA0, SA1, SA2) inputs. When the Device Select Code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (SA0, SA1, SA2) inputs.

The 8th bit is the Read/Write bit (R/W#). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the SPD Device Select code, the SPD section deselects itself from the bus, and goes into Standby mode. The I²C operating modes are detailed in Table 2 on page 5.

Table 2 — I²C Operating Modes

Mode	R/W# Bit	Bytes	Initial Sequence
SPD Current Address Read	1	1	START, Device Select, R/W# = 1
SPD Random Address Read	0	1	START, Device Select, R/W# = 0, Address
	1		reSTART, Device Select, R/W# = 1
SPD Sequential Read	1	≥ 1	Similar to Current or Random Address Read
SPD Byte Write	0	1	START, Device Select, R/W# = 0, data, STOP
SPD Page Write	0	≤ 16	START, Device Select, R/W# = 0, data, STOP
TS Write	0	2	START, Device Select, R/W#=0, pointer, data, STOP
TS Read	1	2	START, Device Select, R/W#=1, pointer, data, STOP

2.3 Device Pin Definition

Table 3 — Pin Description for TSE2002av

Pin #	Pin Name	Definition
1	SA0	Select Address 0
2	SA1	Select Address 1
3	SA2	Select Address 2
4	V _{SSSPD}	Ground
5	SDA	Serial data
6	SCL	Serial clock
7	EVENT#	Temperature Event
8	V _{DDSPD}	Supply voltage

2.4 Pin Functional Description

Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to V_{DDSPD}. (Figure 3 on page 7 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-ORed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to the most positive V_{DDSPD} in the I²C chain. (Figure 3 on page 7 indicates how the value of the pull-up resistor can be calculated).

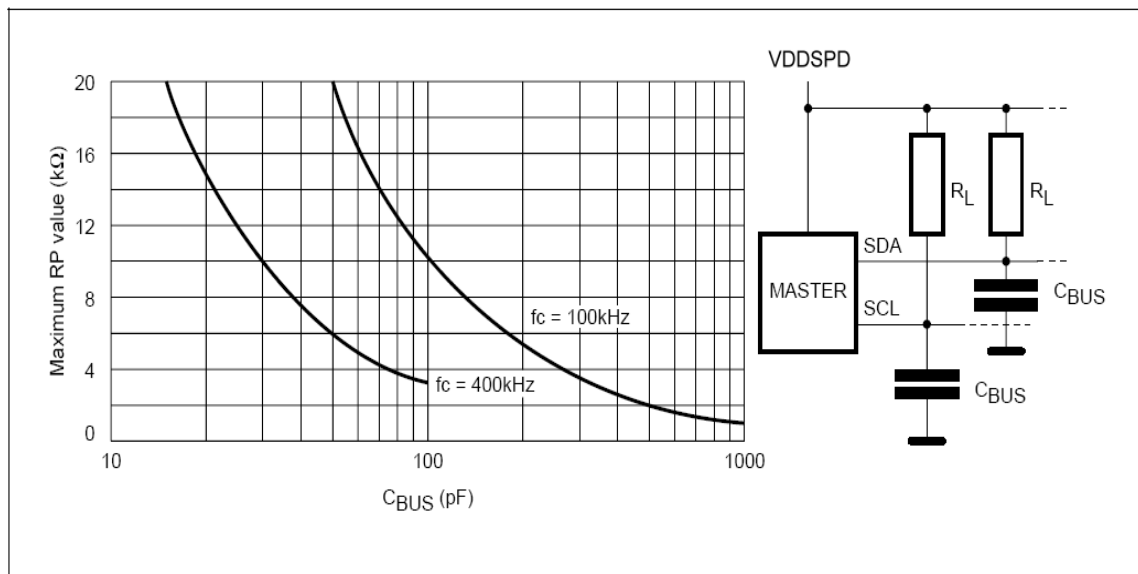


Figure 3 — Maximum R_L Value Versus Bus Capacitance (C_{BUS}) for an I²C Bus

Select Address (SA0, SA1, SA2)

These input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit Slave Address. In the end application, SA0, SA1 and SA2 must be directly (not through a pull-up or pull-down resistor) connected to V_{DDSPD} or V_{SSSPD} to establish the Slave Address. When these inputs are not connected, an internal pull-down circuitry makes (SA0, SA1, SA2) = (0, 0, 0).

The SA0 input is used to detect the V_{HV} voltage, when decoding an SWP or CWP instruction. Refer to Table 2 on page 5 for decode details.

EVENT#

The TSE2002av EVENT# pin is an open drain output that requires a pull-up to V_{DDSPD} on the system motherboard or integrated into the master controller. EVENT# has three operating modes, depending on configuration settings and any current out-of-limit conditions. These modes are Interrupt, Comparator, or TCRIT Only.

In Interrupt Mode the EVENT# pin will remain asserted until it is released by writing a '1' to the "Clear Event" bit in the Status Register. The value to write is independent of the EVENT# polarity bit.

In Comparator Mode the EVENT# pin will clear itself when the error condition that caused the pin to be asserted is removed. When the temperature is compared against the TCRIT limit, then this mode is always used.

Finally, in the TCRIT Only Mode the EVENT# pin will only be asserted if the measured temperature exceeds the TCRIT Limit. Once the pin has been asserted, it will remain asserted until the temperature drops below the TCRIT Limit minus the TCRIT hysteresis. Figure 4 on page 8 illustrates the operation of the different modes over time and temperature.

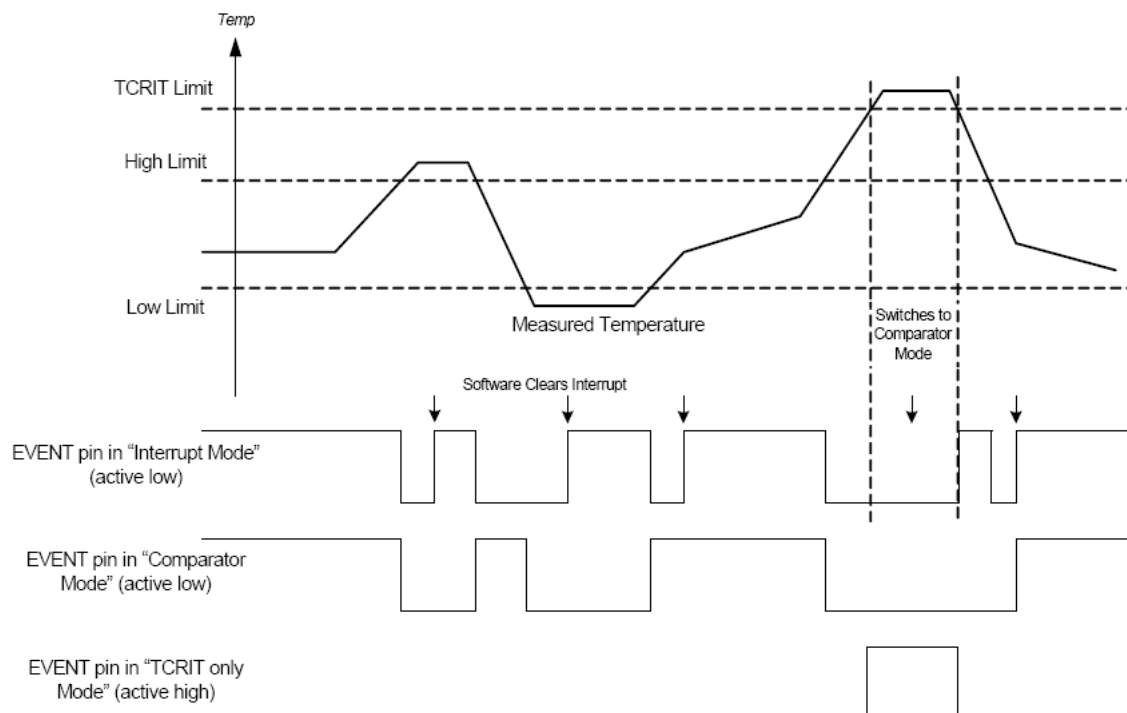


Figure 4 — EVENT# Pin Mode functionality

Systems that use the active high mode for EVENT# must be wired point to point between the TSE2002av and the sensing controller. Wire-OR configurations should not be used with active high EVENT# since any device pulling the EVENT# signal low will mask the other devices on the bus. Also note that the normal state of EVENT# in active high mode is a 0 which will constantly draw power through the pull-up resistor.

2.5 Device Reset and Initialization

In order to prevent inadvertent Write operations during Power-up, a Power On Reset (POR) circuit is included.

At Power-up (phase during which V_{DDSPD} is lower than $V_{DDSPDmin}$ but increases continuously), the device will not respond to any instruction until V_{DDSPD} has reached the Power On Reset threshold voltage (this threshold is lower than the minimum V_{DDSPD} operating voltage defined in the DC AND AC PARAMETERS tables). Once V_{DDSPD} has passed the POR threshold, the device is reset. The actual POR threshold voltage will be implementation dependent, and is not defined in this document.

The device is delivered with all bits in the EEPROM memory array set to '1' (each byte contains 0xFF).

Prior to selecting the memory and issuing instructions, a valid and stable V_{DDSPD} voltage must be applied. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

At Power-down (phase during which V_{DDSPD} decreases continuously), as soon as V_{DDSPD} drops from the normal operating voltage below the minimum operating voltage, the device stops responding to commands, and remains in reset until the POR threshold voltage is reached.

2.6 Software Write Protect

The TSE2002av has three software write-protection features, allowing the bottom half of the memory area (addresses 0x00 to 0x7F) to be temporarily or permanently write protected.

Software write-protection is handled by three instructions:

- SWP: Set Write Protection
- CWP: Clear Write Protection
- PSWP: Permanently Set Write Protection

The level of write-protection (set or cleared) that has been defined using these instructions, remains defined even after a power cycle.

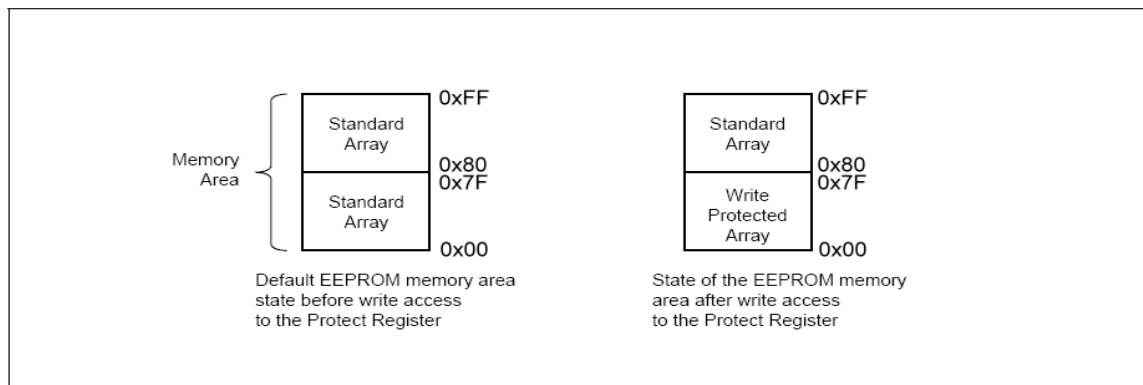


Figure 5 — Result of Setting the Write Protection

SWP and CWP

If the software write-protection has been set with the SWP instruction, it can be cleared again with a CWP instruction.

The two instructions (SWP and CWP) have the same format as a Byte Write instruction, but with a different Device Type Identifier (as shown in Table 2 on page 5). Like the Byte Write instruction, it is followed by an address byte and a data byte, but in this case the contents are all “Don't Care” (Figure 6 on page 10). Another difference is that the voltage, V_{HV} , must be applied on the SA0 pin, and specific logical levels must be applied on the other two (SA1 and SA2, as shown in Table 2 on page 5).

PSWP

If the software write-protection has been set with the PSWP instruction, the first 128 bytes of the memory are permanently write-protected. This write-protection cannot be cleared by any instruction, or by power-cycling the device. Also, once the PSWP instruction has been successfully executed, the TSE2002av no longer acknowledges any instruction (with a Device Type Identifier of 0110) to access the write-protection settings.

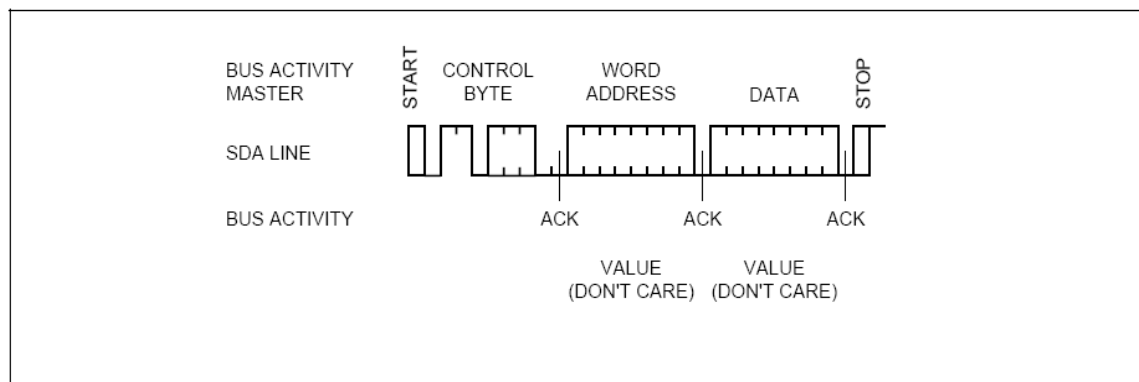


Figure 6 — Setting the Write Protection

Reading Write Protection Status

The status of software write protection can be determined using these instructions:

- Read SWP: Read Write Protection Status
- Read PSWP: Read Permanently Set Write Protection Status

Read SWP

The controller issues a Read SWP command. If Software Write Protection has not been set, the device replies to the data byte with an Ack. If Software Write Protection has been set, the device replies to the data byte with a NoAck.

Read PSWP

The controller issues a Read PSWP command. If Permanent Software Write Protection has not been set, the device replies to the data byte with an Ack. If Permanent Software Write Protection has been set, the device replies to the data byte with a NoAck.

2.7 Write Operations

Following a Start condition the bus master sends a Device Select Code with the R/W# bit reset to 0. The device acknowledges this, as shown in Table 7 on page 11, and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

When the bus master generates a Stop condition immediately after the Ack bit (in the “10th bit” time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored, and the device does not respond to any requests.

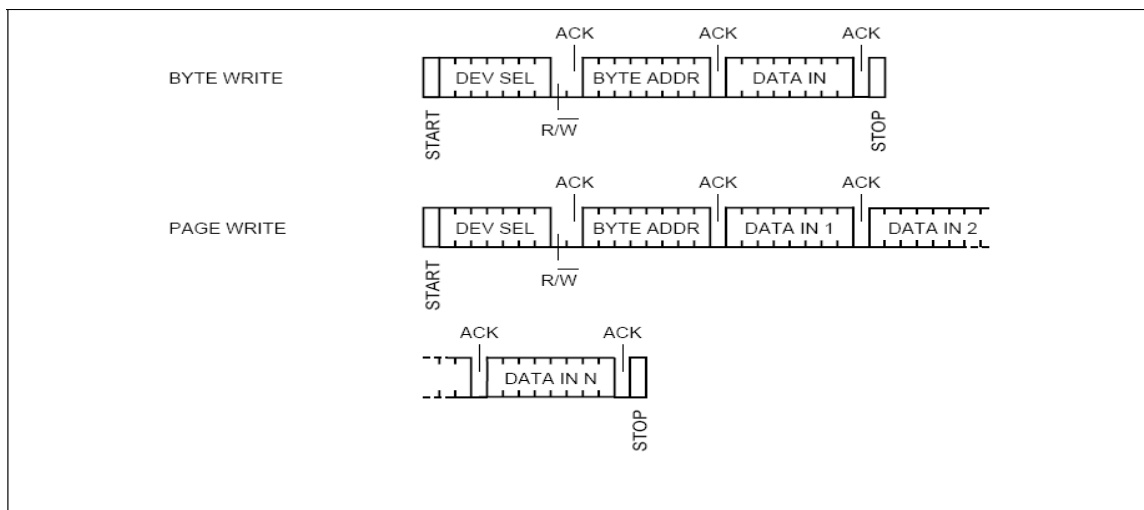


Figure 7 — Write Mode Sequences in a Non-Write Protected Area

Byte Write

After the Device Select Code and the address byte, the bus master sends one data byte. If the addressed location is write-protected, the device replies to the data byte with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in Figure 7 on page 11.

Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as “roll-over” occurs. This should be avoided, as data starts to be over-written in an implementation dependent fashion.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device. If the addressed location is write-protected, the device replies to the data byte with NoAck, and the locations are not modified. After each byte is transferred, the internal byte address counter is incremented. The transfer is terminated by the bus master generating a Stop condition.

2.8 Write Cycle Polling Using ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_W) is shown in Table 24 on page 30, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.