

4.1.6 Definitions of the EE1004-v 4 Kbit Serial Presence Detect (SPD) EEPROM and TSE2004av 4 Kbit SPD EEPROM with Temperature Sensor (TS) for Memory Module Applications

1. SCOPE

This standard defines the specifications of interface parameters, signaling protocols, and features for Serial Presence Detect (SPD) EEPROM (EE) and Temperature Sensor (TS) as used for memory module applications. The designations EE1004-v and TSE2004av refer to the families of devices specified by this document.

The purpose is to provide a standard for the EE1004-v and TSE2004av devices for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

A single specification document for both families of devices is written to establish and maintain the commonality of these devices and promote the interchangeability of devices in target applications that may require the EE and TS for some uses and EE only for other uses. When a portion of this specification refers to both classes of devices, the abbreviation EE/TSE is used.

NOTE: The designations EE1004-v and TSE2004av refer to the part of the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2. DEVICE STANDARD

2.1. Description

The EE1004-v is a 512-byte EEPROM device. The TSE2004av is a combination 512-byte EEPROM and Temperature Sensor device. The EE/TSE devices are designed to operate in one of two voltage ranges, 1.7-3.6 V or 2.2-3.6 V. All EE/TSE 2.2-3.6 V nominal devices shall operate the I²C Bus up to 1 MHz maximum (Fast Mode+). Operation to 100 KHz compliant with SMBus 2.0 operation. EE/TSE devices are intended to interface to I²C Buses which have multiple devices on a shared bus, and must be uniquely addressed on this bus. A substantial reduction in supply current may be achieved using the software programmed shutdown mode.

2.2. Common Features summary:

EE1004-v Variations						
Base part number					v	Single Supply Voltage
EE1004					1	1.7 to 3.6 V
					2	2.2 to 3.6 V
TSE2004av Variations						
Base part number		a	Sensor Accuracy		v	Single Supply Voltage
TSE2004		B	0.5 °C typ from 75-95 °C		1	1.7 to 3.6 V
			1.0 °C typ from 40-125 °C		2	2.2 to 3.6 V
			2.0 °C typ from -20-125 °C			
Examples:						
1. EE1004-1 is a 512-byte SPD with a single supply voltage range from 1.7 to 3.6 V.						
2. TSE2004B2 is a 512-byte SPD with Thermal Sensor having 0.5 °C typical accuracy from 75-95 °C and a single supply voltage range from 2.2 to 3.6 V.						

- Low operating current:
 < 100 uA maximum with EE in Standby and TS in Shutdown mode
 ~1 mA typical with EE in Standby mode and TS active
 ~2 mA typical with TS and EE enabled at 3.3 V input
- Two Wire I²C Bus Serial Interface
- Up to 100 kHz Transfer Rate below 2.2 V compliant with SMBus 2.0
- Up to 1 MHz Transfer Rate (Fast Mode+ I²C Bus compliant) at or above 2.2 V
- Package: Thermally Enhanced PSON-8 standard for all JEDEC module applications

EE Features summary(EE/TSE):

- Individual Reversible Software Data Protection for all four 128 Byte Blocks
- Byte and Page (up to 16 Bytes) Write Operation
- Random and Sequential Read modes
- Self-Timed Write Cycle
- Automatic Address Incrementing

TS Features summary (TSE2004av only):

- Typical accuracy of 0.5 °C accuracy for the active range from 75 ~ 95 °C
- Typical accuracy of 1.0 °C for other monitor ranges from 40 ~ 125 °C
- Ambient temperature (TA) sense through an operating range of -20 to +125 °C
- Temperature sample rate minimum of 8 samples/s
- Selectable 0, 1.5 °C, 3 °C, 6 °C Hysteresis on set point

The EE/TSE devices include a 4 Kbit serial EEPROM organized as two pages of 256 bytes each, or 512 bytes of total memory. Each page is comprised of two 128 byte blocks. The devices are able to selectively lock the data in any or all of the four 128-byte blocks. Designed specifically for use in DRAM DIMMs (Dual Inline Memory Modules) with Serial Presence Detect, all the information concerning the DRAM module configuration (such as its access speed, its size, its organization) can be kept write protected in one or more of the blocks of memory.

The EE/TSE devices are protocol compatible with previous generation 2 Kbit devices such as the EE1002(A) and TSE2002av. The page selection method allows commands used with legacy devices such as EE1002(A) and TSE2002av to be applied to the lower or upper pages of the EE/TSE. In this way, the EE/TSE may be used in legacy applications without software changes. Minor exceptions to this compatibility, such as elimination of the Permanent Write Protect feature, are documented.

Individually locking a 128-byte block of the EE may be accomplished using a software write protection mechanism in conjunction with a high input voltage V_{HV} on input SA0. By sending the device a specific I²C Bus sequence, each block may be protected from writes until write protection is electrically reversed using a separate I²C Bus sequence which also requires V_{HV} on input SA0. Write protection for all four blocks is cleared simultaneously, and write protection may be re-asserted after being cleared.

The Thermal Sensor (TS) section of the TSE2004av continuously monitors the temperature and updates the temperature data a minimum of eight times per second. Temperature data is latched internally by the device and may be read by software from the bus host at any time.

Internal registers are used to configure both the TS performance and response to over-temperature conditions. The device contains programmable high, low, and critical temperature limits. Finally, the device EVENT_n pin can be configured as active high or active low and can be configured to operate as an interrupt or as a comparator output.

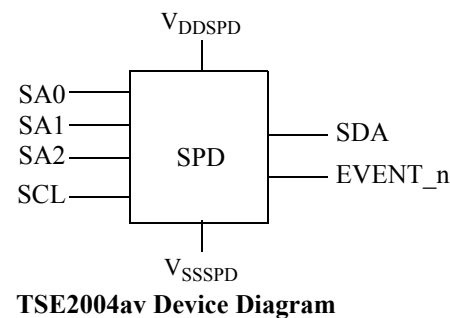
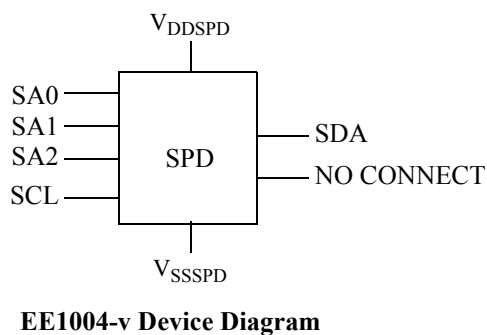


Figure 1 — Device Diagrams

2.3. Device Interface

The EE/TSE behaves as a slave device in the I²C Bus protocol, with all operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and R/W_n bit (as described in Table 3 on page 7), terminated by an acknowledge bit. EE/TSE family devices shall not initiate clock stretching, which is an optional I²C Bus feature.

In accordance with the I²C Bus definition, the EE/TSE devices use three (3) built-in, 4-bit Device Type Identifier Codes (DTIC) and a 3-bit Select Address to generate an I²C Bus Slave Address. The EE memory may be accessed using a DTIC of (1010), and to perform the SWPn, RSPn, or CSWP operations, a DTIC of (0110) is required. The TS registers of the TSE2004av are accessed using a DTIC of (0011).

EE and TS portions of TSE devices are designed to operate in parallel. Accesses to each portion of the device may be interleaved as long as the command protocol is followed.

2.3.1. EE/TSE Serial Address Selection

Inputs SA0, SA1, and SA2 inputs are directly combined with the DTIC and the EE page address bit to qualify I²C Bus addresses. Each of the SA pins is tied to V_{DDSPD} or V_{SSSPD} and the Logical Serial Address (LSA) is equal to the code on the Serial Address pins.

Table 1 — I²C Bus Addressing Modes

Logical Serial Address (LSA)	SA2	SA1	SA0
000	0	0	0
001	0	0	1
010	0	1	0
011	0	1	1
100	1	0	0
101	1	0	1
110	1	1	0
111	1	1	1
Note 1: 0 = V _{SSSPD} , 1 = V _{DDSPD}			

2.4. Interface Protocol

When writing data to the memory, the EE/TSE inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Bus Master generated STOP condition after an Ack for WRITE, and after a NoAck for READ.

Violations of the command protocol result in unpredictable operation.

The TS section of the TSE2004av device uses a pointer register to access all registers in the device. Additionally, all data transfers to and from this section of the device are performed as block read/write operations. The data is transmitted/received as 2 bytes, Most Significant Byte (MSB) first, and terminated with a NoAck and STOP after the Least Significant byte (LSB). Data and address information is transmitted and received Most Significant Bit first.

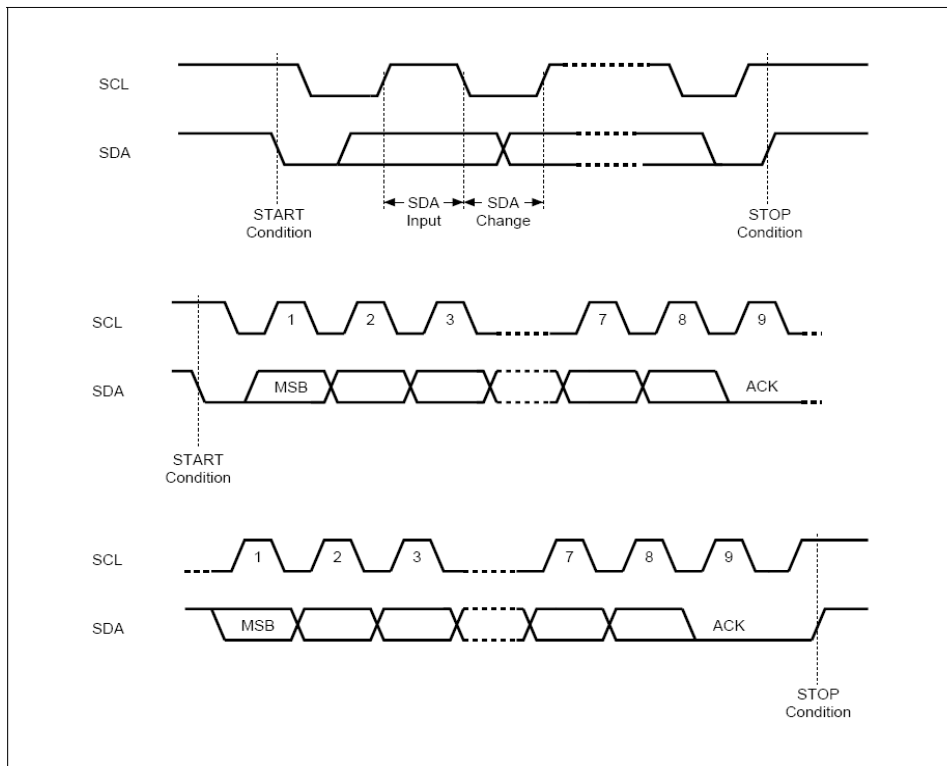


Figure 2 — I²C Bus Protocol

Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

Stop Condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the EE into Standby mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle for the EE. Neither of these conditions changes the operation of the TS section of a TSE2004av.

Acknowledge Bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

No Acknowledge Bit (NACK)

The no-acknowledge bit is used to indicate the completion of a block read operation, or an attempt to modify a write-protected register. The bus master releases Serial Data (SDA) after sending eight bits of data, and during the 9th clock pulse period, and does not pull Serial Data (SDA) Low.

Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change only when Serial Clock (SCL) is driven Low.

Memory Addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in Table 2 (on Serial Data (SDA), most significant bit first).

Table 2 — Device Select Code

Function	Abbr	Device Type Identifier ¹				Select Address ^{2, 4}			R/ W_n	SA0 Pin ³
		b7	b6	b5	b4	b3	b2	b1	b0	
Read Temperature registers ⁸	RTR	0	0	1	1	LSA2	LSA1	LSA0	1	0 or 1
Write Temperature registers ⁸	WTR								0	
Read EE memory	RSPD	1	0	1	0	LSA2	LSA1	LSA0	1	0 or 1
Write EE memory	WSPD								0	
Set Write Protection, block 0	SWP0	0	1	1	0	0	0	1	0	V _{HV}
Set Write Protection, block 1	SWP1					1	0	0	0	V _{HV}
Set Write Protection, block 2	SWP2					1	0	1	0	V _{HV}
Set Write Protection, block 3	SWP3					0	0	0	0	V _{HV}
Clear All Write Protection	CWP					0	1	1	0	V _{HV}
Read Protection Status, block 0	RPS0					0	0	1	1	0, 1 or V _{HV}
Read Protection Status, block 1	RPS1					1	0	0	1	0, 1 or V _{HV}
Read Protection Status, block 2	RPS2					1	0	1	1	0, 1 or V _{HV}
Read Protection Status, block 3	RPS3					0	0	0	1	0, 1 or V _{HV}
Set EE Page Address to 0 ^{5, 10}	SPA0					1	1	0	0	0, 1 or V _{HV}
Set EE Page Address to 1 ^{5, 10}	SPA1					1	1	1	0	0, 1 or V _{HV}
Read EE Page Address ⁶	RPA					1	1	0	1	0, 1 or V _{HV}
Reserved	--					All Other Encodings				

Note 1: The most significant bit, b7, is sent first.

Note 2: Logical Serial Addresses (LSA) are generated by the combination of inputs on the SA pins; see Figure 2 on page 6.

Note 3: SA0 pin is driven to 0 = V_{SSPD}, 1 = V_{DDSPD}, or V_{HV}.

Note 4: For backward compatibility with previous devices, the order of block select bits (b3 and b1) are not a simple binary encoding of the block number.

Note 5: Set EE page address to 0 selects the lower 256 bytes of EEPROM, setting to 1 selects the upper 256 bytes of EEPROM. Subsequent Read EE or Write EE commands operate on the selected EE page.

Note 6: Reading the EE page address results in Ack when the current page is 0 and NoAck when the current page is 1.

Note 7: Permanent Write Protect features of the EE1002(A) and TSE2002av have been eliminated from the EE/TSE devices.

Note 8: TSE2004av only.

Note 9: Don't Care values for word address and data fields following commands may result in Ack or No_Ack responses from EE/TSE devices. See Figure 6, "Protocol for Commands SWPn, CWP, RPSn, SPAn, RPA," on page 12.

Note 10: No delay is required after switching pages via the SPAn commands before accessing the device.

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Select Address. To address the EE memory array, the 4-bit Device Type Identifier is 1010b; to access the write-protection settings or EE page address, it is 0110b; and to access the Temperature Sensor settings is 0011b (TSE2004av only). Additionally, writing or clearing the reversible EE write protect requires that SA0 be raised to the V_{HV} voltage level.

Up to eight EE/TSE devices can be connected on a single I²C Bus. Each one is given a unique 3-bit Logical Serial Address code. The LSA is a decoding of information on the SA pins SA0, SA1, and SA2 as described in Table 2 on page 6. When the Device Select Code is received, the device only responds if the Select Address is the same as the Logical Serial Address.

Write Protection commands SWPn, CWP, and RPSn, and the EE Page Address commands SPAn and RPA, do not use the Select Address or Logical Serial Address, therefore all devices on the I²C Bus will act on these commands simultaneously. Since it is impossible to determine which device is responding to RPSn or RPA commands, for example, these functions are primarily used for external device programmers rather than in-system applications.

The 8th bit is the Read/Write bit (R/W_n). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the EE Device Select code, the EE section deselects itself from the bus, and goes into Standby mode. The I²C Bus operating modes are detailed in Table 3.

Table 3 — I²C Bus Operating Modes

Mode	R/W _n Bit	Bytes	Initial Sequence
EE Current Address Read	1	1	START, Device Select, R/W _n = 1
EE Random Address Read	0	1	START, Device Select, R/W _n = 0, Address
	1		reSTART, Device Select, R/W _n = 1
EE Sequential Read	1	≥ 1	Similar to Current or Random Address Read
EE Byte Write	0	1	START, Device Select, R/W _n = 0, data, STOP
EE Page Write	0	≤ 16	START, Device Select, R/W _n = 0, data, STOP
TS Write ¹	0	2	START, Device Select, R/W _n =0, pointer, data, STOP
TS Read ¹	1	2	START, Device Select, R/W _n =1, pointer, data, STOP
Note:			
1. TSE2004av only			

2.5. Device Pin Definition

Table 4 — Pin Description for EE/TSE

Pin #	Pin Name	Type	Definition
1	SA0	Input	Select Address 0
2	SA1	Input	Select Address 1
3	SA2	Input	Select Address 2
4	V _{SSSPD}	Supply	Ground
5	SDA	Input/Open Drain Output	Serial data
6	SCL	Input	Serial clock
7	EVENT_n	Open Drain Output	TSE2004av temperature event
	No Connect	No Connect	EE1004-v does not use this pin
8	V _{DDSPD}	Supply	Supply voltage
Note: Thermal sensing devices also have a heat paddle, typically connected to the application ground plane			

2.6. Pin Functional Description

Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to V_{DDSPD}. (Figure 3 on page 9 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-ORed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to the most positive V_{DDSPD} in the I²C Bus chain. (Figure 3 on page 9 indicates how the value of the pull-up resistor can be calculated).

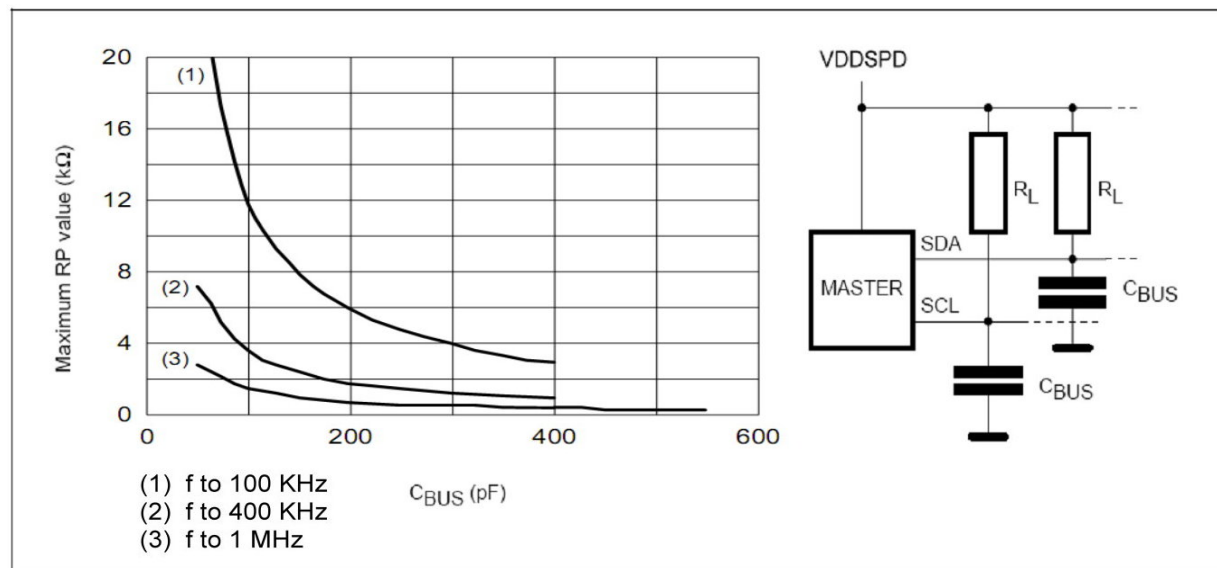


Figure 3 — Maximum R_L Value Versus Bus Capacitance (C_{BUS}) for an I²C Bus

Serial Address SA (SA0, SA1, SA2)

These input signals are used to create the Logical Serial Address LSA that is compared to the three least significant bits (b3, b2, b1) of the 7-bit Slave Address. See Table 1 on page 4 for details on LSA encoding.

The SA0 input is also used to detect the V_{HV} voltage when decoding an SWPn or CWP instruction. Refer to Table 3 on page 7 for decode details.

EVENT_n (TSE2004av only)

The TSE2004av EVENT_n pin is an open drain output that requires a pull-up to V_{DDSPD} on the system motherboard or integrated into the master controller. EVENT_n has three operating modes, depending on configuration settings and any current out-of-limit conditions. These modes are Interrupt, Comparator, or TCRIT Only.

In Interrupt Mode the EVENT_n pin will remain asserted until it is released by writing a '1' to the "Clear Event" bit in the Status Register. The value to write is independent of the EVENT_n polarity bit.

In Comparator Mode the EVENT_n pin will clear itself when the error condition that caused the pin to be asserted is removed. When the temperature is compared against the TCRIT limit, then this mode is always used.

Finally, in the TCRIT Only Mode the EVENT_n pin will only be asserted if the measured temperature exceeds the TCRIT Limit. Once the pin has been asserted, it will remain asserted until the temperature drops below the TCRIT Limit minus the TCRIT hysteresis. Figure 5 illustrates the operation of the different modes over time and temperature.

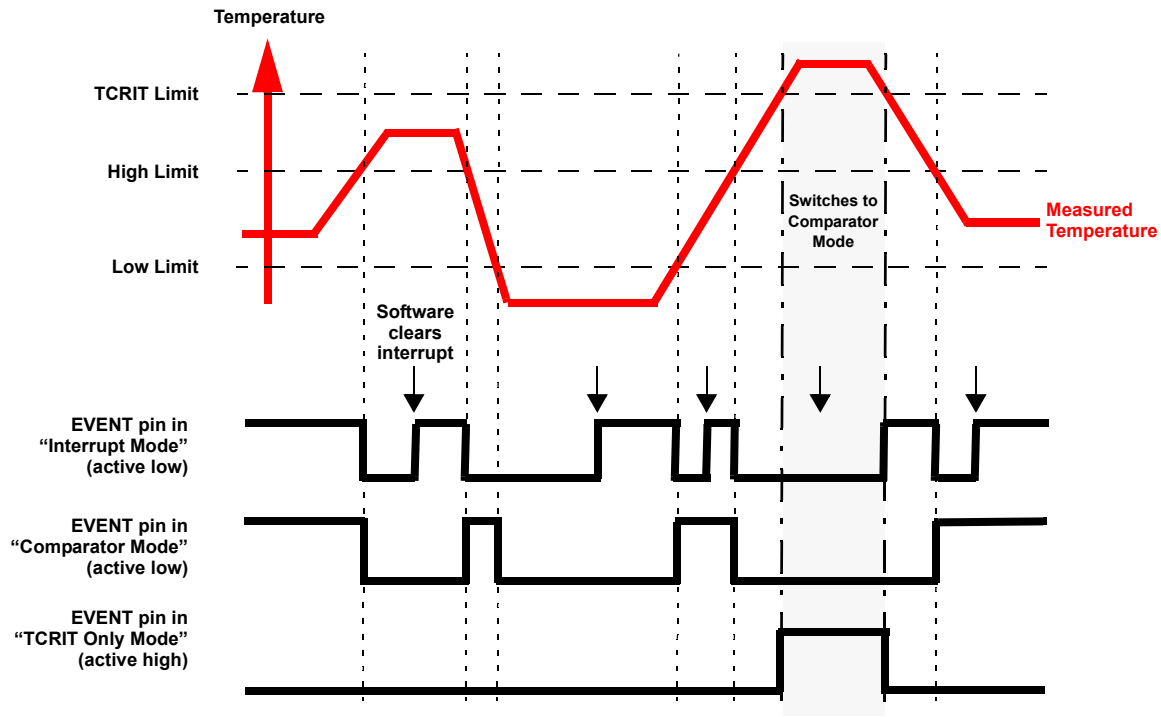


Figure 4 — EVENT_n Pin Mode functionality

Systems that use the active high mode for EVENT_n must be wired point to point between the TSE2004av and the sensing controller. Wire-OR configurations should not be used with active high EVENT_n since any device pulling the EVENT_n signal low will mask the other devices on the bus. Also note that the normal state of EVENT_n in active high mode is a 0 which will constantly draw power through the pull-up resistor.

2.7. EE/TSE Device Reset and Initialization

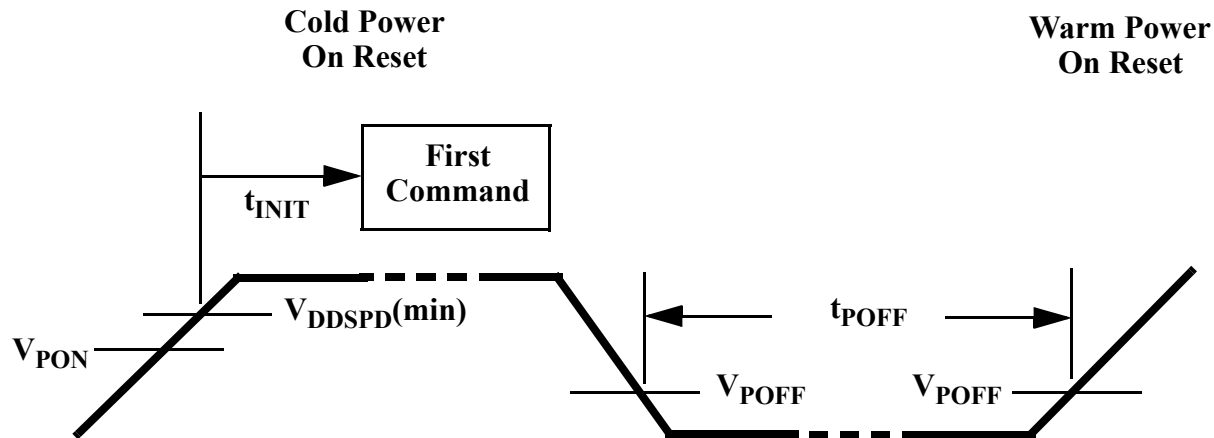


Figure 5 — V_{DDSPD} Ramp Up and Ramp Down

In order to prevent inadvertent operations during power up, a Power On Reset (POR) circuit is included. On cold power on, V_{DDSPD} must rise monotonically between V_{PON} and $V_{DDSPD(min)}$ without ringback to ensure proper startup. Once V_{DDSPD} has passed the V_{PON} threshold, the device is reset.

Prior to selecting the memory and issuing instructions, a valid and stable V_{DDSPD} voltage must be applied, and no command may be issued to the device for t_{INIT} . The supply voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

At power down (phase during which V_{DDSPD} decreases continuously), as soon as V_{DDSPD} drops from the normal operating voltage below the minimum operating voltage, the device stops responding to commands. On warm power cycling, V_{DDSPD} must remain below V_{POFF} for t_{POFF} , and must meet cold power on reset timing when restoring power.

The EE/TSE devices are delivered with all bits in the EEPROM memory array set to '1' (each byte contains 0xFF).

2.8. EE/TSE Software Write Protect

The EE/TSE devices have three software commands for setting, clearing, or interrogating the write-protection status.

- SWPn: Set Write Protection for Block n
- CWP: Clear Write Protection for all blocks
- RPSn: Read Protection Status for Block n

There are four independent memory blocks, and each block may be independently protected. The memory blocks are:

- Block 0 = memory addresses 0x00 to 0x7F (decimal 0 to 127), SPD Page Address = 0
- Block 1 = memory addresses 0x80 to 0xFF (decimal 128 to 255), SPD Page Address = 0