

3.7 Static Random Access Memory (SRAM)

The following SRAM standards were developed by Committees JC–42.1 and JC–42.3. Starting in Release 11, Committee JC–42.2 has been assigned responsibility for developing new standards and maintaining old ones. The devices described are compatible with one of several logic circuit families as defined. The device standards require that the memory devices must operate with signal levels and power supply voltages that are consistent with those used in the logic family(s) specified. More recent standards have been for MOS devices. These standards are located in sections along with the TTL device standards. The nominal power supply voltages for the four families in use are as follows:

TTL, $V_{CC} = 5.0\text{ V}$

MOS, V_{DD} varies depending on the technology being used at the time.

10K ECL, $V_{EE} = 5.2\text{ V}$

100K ECL, $V_{EE} = 4.5\text{ V}$

The standards described on this page are applicable to multiple device configurations as noted in the individual standards.

The sub-sections of the SRAM section are as follows:

3.7.1 – Bit Wide TTL

3.7.2 – Bit Wide ECL

3.7.3 – Nibble Wide TTL

3.7.4 – Nibble Wide ECL

3.7.5 – Byte Wide TTL & MOS

3.7.6 – Byte Wide ECL

3.7.7 – Word Wide TTL & MOS

3.7.8 – Double Word Wide MOS

3.7.9 – Quad Word Wide MOS

3.7–1 – JTAG Extension to Revolutionary Pinout SRAM Devices

This standard establishes a convention to provide uniform guidance when it is desired to add the IEEE 1149.1 Boundary Scan feature (JTAG) to a device with a pinout that follows the JEDEC SRAM Revolutionary pinout (RPO, devices with redundant centered power pins). The convention shown in Fig. 3.7–1 shows the convention for this addition. This convention applies to all existing and future RPO SRAM devices in DIP, SOJ, TSOP2, and any other two-sided packages that might be used in the future.

3.7–2 – State Diagram for Pipelined Burst SRAM

This standard identifies the functionality of a register-register Synchronous Burst SRAM using the State Diagram format. The standard contains the State Diagram plus a reference key truth table.

