

3.7.3 Nibble Wide TTL SRAM

All of the following standards are for devices which operate with TTL interface levels and power voltages.

3.7.3.1 – 16 BY 4, INVERTING AND NON INVERTING TTL SRAM IN DIP & SCC

CAPACITY—16 WORDS OF 4 BITS

LOGIC FEATURES—This part is available in DATA non inverting and inverting versions

There are two package versions of this part: one in DIP and the other in SCC

PACKAGE—16 PIN DIP, 0.300" WIDE

PIN ASSIGNMENT—Fig. 3.7.3-1

PACKAGE—20 PAD (PIN) SCC, 0.350" BY 0.350"

PIN ASSIGNMENT—Fig. 3.7.3-2

This standard was developed by Committee 42.1.

3.7.3.2 – .25K BY 4 TTL SRAM IN DIP & RCC

CAPACITY—.25K WORDS OF 4 BITS

FAMILY—TTL

There are two versions of this part: one in DIP and the other in RCC

PACKAGE—22 PIN DIP, 0.400" WIDE

PIN ASSIGNMENT—Fig. 3.7.3-3

PACKAGE—28 PAD (PIN) RCC, 0.350" BY 0.550"

PIN ASSIGNMENT—Fig. 3.7.3-4

This standard was developed by Committee 42.1.

3.7.3.3 – 256 BY 4 TTL SRAM WITH G IN SCC

256 WORDS OF 4 BITS

LOGIC FEATURES—SEPARATE DATA INPUT & OUTPUT PINS

PACKAGE—24 PAD (PIN) SCC, 0.4" X 0.4"

PIN ASSIGNMENT—Fig. 3.7.3-5

This standard was developed by Committee 42.1.

3.7.3.4 – 4K TO 64K BY 4 TTL SRAM WITHOUT G FAMILY IN DIP

4K, 16K, 64K WORDS OF 4 BITS

PACKAGE—20, 22, or 24 PIN DIP, 0.3" WIDE

PIN ASSIGNMENT—Fig. 3.7.3-6

3.7.3.5 – 4K BY 4 TTL SRAM IN RCC

CAPACITY—4K WORDS OF 4 BITS

PACKAGE—20 PAD (PIN) RCC, 0.290" BY 0.425 "

PIN ASSIGNMENT—Fig. 3.7.3-7

3.7.3.6 – 4K TO 1M BY 4 TTL SRAM WITH G FAMILY IN DIP

4K, 16K, 64K, 256K, & 1M WORDS OF 4 BITS

LOGIC FEATURES—Output Enable, G

PACKAGE—22, 24 PIN DIP, 0.3" WIDE

—28 PIN DIP, 0.4" WIDE

—32 PIN DIP, UNDEFINED

PIN ASSIGNMENT—Fig. 3.7.3-8

3.7.3.7 – 16K TO 256K BY 4 TTL SRAM WITH AND WITHOUT G FAMILY IN RCC

16K, 64K, 256K WORDS OF 4 BITS

LOGIC FEATURES—Optional Output Enable

PACKAGE—28 PAD (PIN) RCC, 0.350" X 0.550"

PIN ASSIGNMENT—Fig. 3.7.3-9

3.7.3.8 – 16K & 64K BY 4 TTL SRAM IN RCC

CAPACITY—16K & 64K WORDS OF 4 BITS

PACKAGE—22 PAD (PIN) RCC, 0.290" X 0.490"

PIN ASSIGNMENT—Fig. 3.7.3-10

3.7.3.9 – 4K TO 1M BY 4 TTL SRAM WITH AND WITHOUT G FAMILY IN SOJ

CAPACITY—4K, 16K, 64K, 256K, & 1M WORDS OF 4 BITS

LOGIC FEATURES—Optional Output Enable for some densities
—COMMON DATA INPUT & OUTPUT PINS

PACKAGE—24 or 28 PIN SOJ, 0.3" WIDE
—28 PIN SOJ, 0.3" or 0.4" WIDE
—32 PIN SOJ, UNDEFINED

Release 5 adds approval for the 64 X 4 part to be supplied in a 0.3" SOJ or TSOP-2
PIN ASSIGNMENT—Fig. 3.7.3-11

3.7.3.10 – 64K TO 4M BY 4 TTL SRAM IN DIP, SOJ, AND TSOP-2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT

LOGIC FEATURES—COMMON DATA INPUT & OUTPUT PINS
—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES

PACKAGE—28, 32, or 36 PIN SOJ, & TSOP-2, 0.3", 0.4", or 0.5" WIDE with PP=0.05"
—28 Or 32 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".

SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.3-12

3.7.3.11 – 64K TO 4M BY 4 TTL SRAM WITH SEPARATE DATA I/O IN DIP, SOJ, AND TSOP-2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT

LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
—OPTIONAL OUTPUT ENABLE FOR SOME DENSITIES

PACKAGE—32 or 36 or 40 PIN SOJ, & TSOP2, 0.3", 0.4", or 0.5" WIDE with PP=0.05"
—32 Or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".

CAPACITY—32K, 64K, 128K, 256K WORDS OF 8 BITS
SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.3-13

3.7.3.12 – 64K TO 4M BY 4 SYNCHRONOUS SRAM (SSRAM) IN DIP, SOJ, AND TSOP-2

CAPACITY—64K, 256K, 1M, AND 4M WORDS OF 4 BIT

LOGIC FEATURES—SEPARATE DATA INPUT AND OUTPUT PINS
—OUTPUT ENABLE FOR ALL DENSITIES

PACKAGE—32, 36, or 40 PIN SOJ, & TSOP2, 0.3", 0.4", or 0.5" WIDE with PP=0.05"
—32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".

SPECIAL FEATURES—REDUNDANT CENTERED POWER PINS
PIN ASSIGNMENT—Fig. 3.7.3-14

3.7.3.13 – 4K AND 16K BY 4 CACHE TAG SRAM IN DIP AND SOJ

CAPACITY—4K, 16K WORDS OF 4 BIT

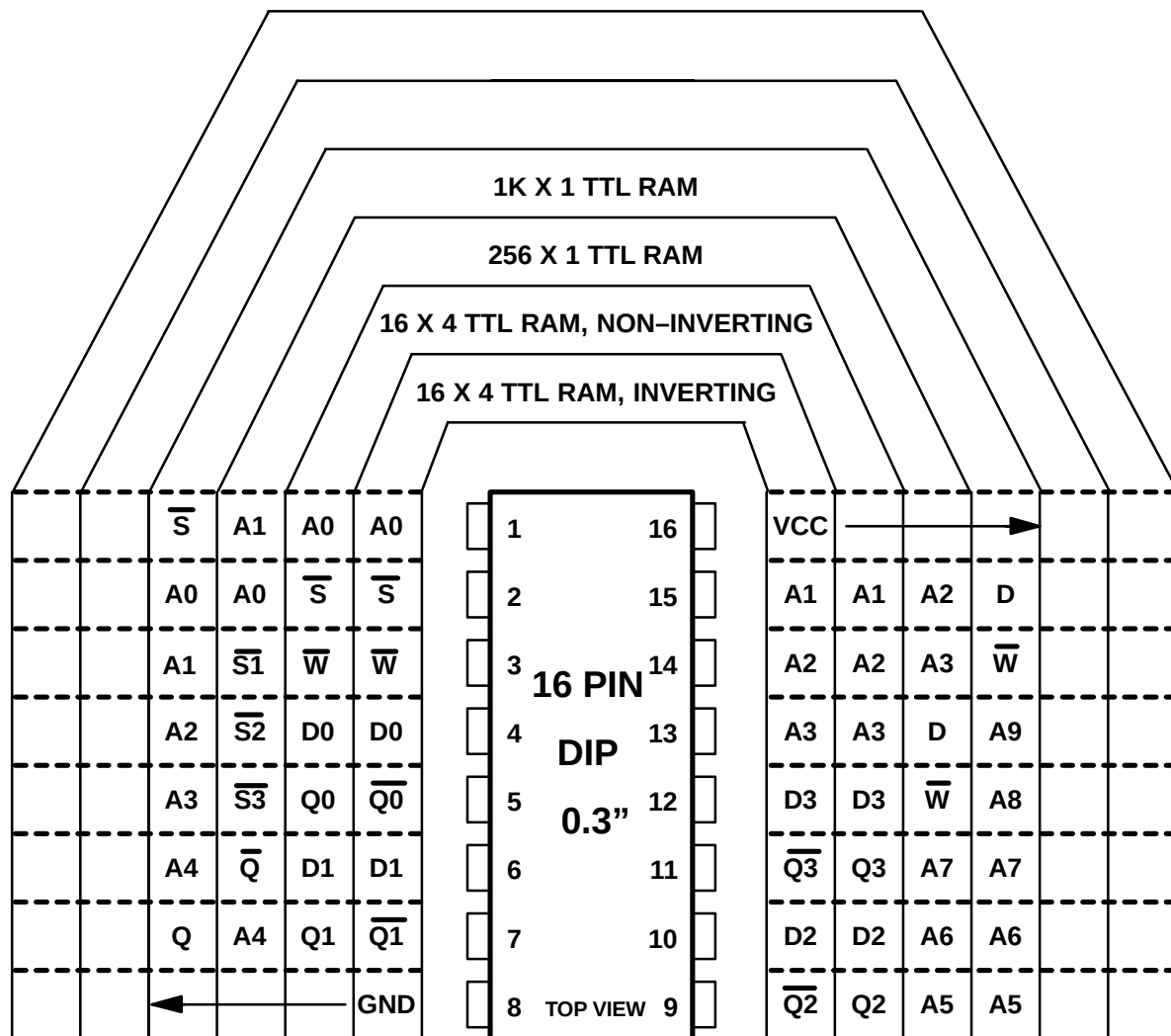
LOGIC FEATURES—OPTIONAL ASYNCHRONOUS CLEAR INPUT

PACKAGE—4K X 4, 22 PIN DIP AND SOJ, 0.3"
—16K X 4, 24 PIN DIP AND SOJ, 0.3"

PIN ASSIGNMENT—Fig. 3.7.3-15

3.7.3.14 – 4M AND 16M SRAM, CONFIGURABLE TO X1 OR X4 IN DIP AND SOJ

SEE PAR. 3.7.1.9 AND FIG. 3.7.1-9 FOR DETAILS OF THIS STANDARD



NC OR F

FIGURE 3.7.3-1
16 BY 4 INVERTING AND NON-INVERTING TTL SRAM IN DIP
Release 1

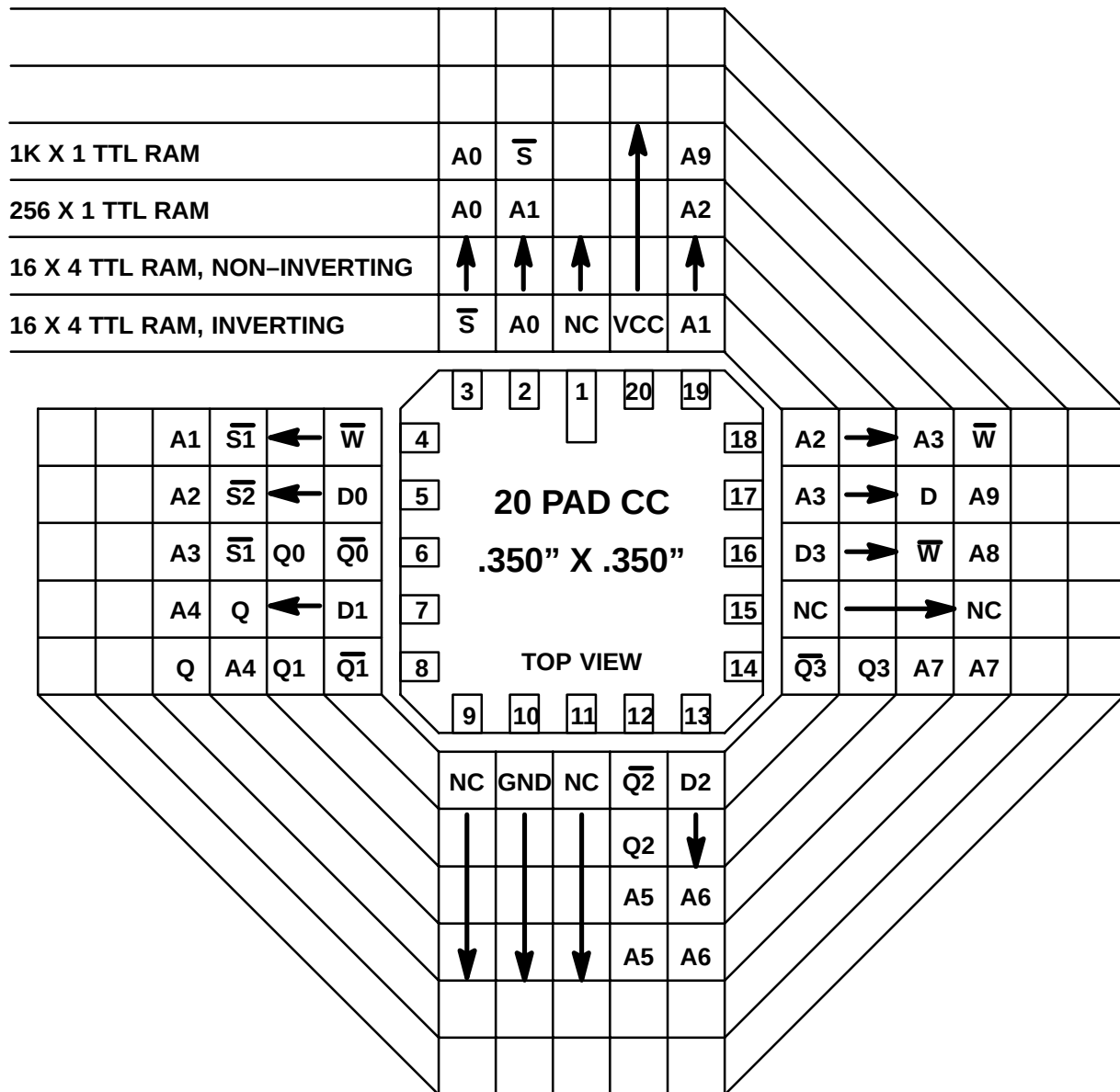


FIGURE 3.7.3-2
16 BY 4 INVERTING AND NON-INVERTING TTL SRAM IN SCC