

3.7.5 Byte Wide TTL and MOS SRAM

All of the following standards are for devices which operate with TTL or MOS interface levels and power voltages.

3.7.5.1 - 64 BY 9 TTL SRAM IN SCC

CAPACITY--64 WORDS OF 9 BITS
PACKAGE--28 PAD (PIN) SCC, 0.450" X 0.450"
PIN ASSIGNMENTS--Fig. 3.7.5-1
This standard was developed by Committee 42.1.

3.7.5.2 - 1K & 2K BY 8 TTL SRAM IN DIP

CAPACITY--1K, 2K WORDS OF 8 BITS
PACKAGE--24 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.7.5-2

3.7.5.3 - 2K & 4K BY 8 TTL SRAM IN RCC

CAPACITY--2K, 4K WORDS OF 8 BITS
PACKAGE--32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT--Fig. 3.7.5-3
These parts are CC equivalents of 24 Pin DIP devices.

3.7.5.4 - 2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ,

CAPACITY--2K, 4K, 8K, 16K, & 32K WORDS OF 8 BITS,
PACKAGE--28 PIN DIP, 0.6" WIDE
--28 PIN DIP, 0.3" WIDE OPTIONAL FOR 8K & 32K DEVICES
PIN ASSIGNMENT--Fig. 3.7.5-4

3.7.5.5 - .5K TO 32K BY 8 TTL SRAM FAMILY IN RCC

CAPACITY--.5K, 1K, 2K, 4K, 8K, 16K, 32K WORDS OF 8 BITS
PACKAGE--32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT--Fig. 3.7.5-5

3.7.5.6 - 32K TO 512K BY 8 TTL SRAM FAMILY IN SOJ or TSOP-2,

CAPACITY--32K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE--28 OR 32 PIN SOJ, 0.3", 0.4" WIDE OR NOT DEFINED
--32 PIN TSOP-2 (see Fig. 3.7.5-6 for package approvals)
PIN ASSIGNMENT--Fig. 3.7.5-6

3.7.5.7 - 64K TO 512K BY 8 TTL SRAM FAMILY IN DIP,

CAPACITY--64K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE--32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.7.5-7

3.7.5.8 - 32K TO 256K BY 9 TTL SRAM FAMILY IN DIP,

CAPACITY--32K, 64K, 128K, 256K WORDS OF 9 BITS,
PACKAGE--32 PIN DIP, 0.6" WIDE
--OPTIONAL 32 PIN DIP & SOJ, 0.3" WIDE FOR 32K DEVICE
PIN ASSIGNMENT--Fig. 3.7.5-8

3.7.5.9 - 32K TO 2M BY 8 AND 512K TO 2M BY 9 TTL SRAM IN DIP, SOJ, AND TSOP-2

CAPACITY--32K, 128K, 512K, 2M WORDS OF 8 BIT AND 512K, 2M WORDS OF 9 BITS
LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS
--OUTPUT ENABLE FOR ALL DENSITIES
PACKAGE--32, 36, or 40 PIN SOJ, & TSOP-2, 0.3", 0.4", or 0.5" WIDE with PP=0.05"
--32 or 36 PIN DIP, 0.3", 0.4" with PP=0.1", or 0.6" with PP=0.07".
SPECIAL FEATURES--MULTIPLE CENTERED POWER PINS
PIN ASSIGNMENT--Fig. 3.7.5-9

3.7.5.10 - 32K and 128K BY 8 TTL SSRAM IN DIP AND SOJ

CAPACITY--32K, & 128K WORDS OF 8 BIT
LOGIC FEATURES--SEPARATE DATA INPUT & OUTPUT PINS
--OUTPUT ENABLE
PACKAGE--40 PIN DIP, 0.6" wide
--40 PIN SOJ, UNDEFINED
SPECIAL FEATURES--MULTIPLE CENTERED POWER PINS
PIN ASSIGNMENT--Fig. 3.7.5-10

3.7.5.11 - 2K TO 32K BY 9 DPSRAM FAMILY IN 68 SCC

CAPACITY--2K, 8K, 32K WORDS OF 9 BITS,
LOGIC FEATURES--Two identical access ports
PACKAGE--68 PAD (PIN) SCC, 0.950" X 0.950"
PIN ASSIGNMENT--Fig. 3.7.5-11
This part contains two identical ports for access to the storage array. These ports include full sets of address, data, and control signals.

3.7.5.12 - 32K BY 9 CACHE SRAM IN 44 SCC

CAPACITY--32K WORDS OF 9 BITS,
LOGIC FEATURES--Internal CACHE data compare logic
PACKAGE--44 TERMINAL SCC, 0.500" X 0.500"
PIN ASSIGNMENT--Fig. 3.7.5-12
This part contains specialized logic functions which allow it to be used to implement the CACHE memory function conveniently.

3.7.5.13 - 128K BY 8 SRAM IN TSOP1

CAPACITY--128K WORDS OF 8 BITS
PACKAGE--32 PIN TSOP1, 20 mm X 8 mm, 0.5 mm PIN PITCH
PIN ASSIGNMENTS--Fig. 3.7.5-13

3.7.5.14 - 128K BY 8 & 9 SSRAM IN SOJ

CAPACITY--128K WORDS OF 8 BITS
PACKAGE--32 PIN SOJ, 0.400"
PIN ASSIGNMENTS--Fig. 3.7.5-14

3.7.5.15 - 1K AND 2K BY 8 DPSRAM FAMILY IN 48 DIP

CAPACITY--1K, 2K WORDS OF 8 BITS,
LOGIC FEATURES--Two identical access ports
PACKAGE--48 PIN DIP, 0.600"
PIN ASSIGNMENT--Fig. 3.7.5-15

This part contains two identical ports for access to the storage array. These ports include full sets of address, data, and control signals.

3.7.5.16 - 128K TO 512K BY 8 SRAM FAMILY IN 32 CDSO-N

CAPACITY--128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE--32 PIN LEADLESS CERAMIC SO, 0.400"
PIN ASSIGNMENT--Fig. 3.7.5-16

This family of parts is based on the evolutionary SRAM pinout family described in Sec. 3.7.5.7

3.7.5.17 - 128K TO 512K BY 8 & 9 SSRAM AND 128K BY 9 SRAM IN 33 DIP, TSOP2, AND SOJ

CAPACITY--128K & 512K WORDS OF 8 OR 9 BITS,
LOGIC FEATURES--Both Synchronous and Asynchronous versions of the 128K part
PACKAGE--36 PIN DIP, TSOP2, or SOJ, 0.400" or 0.600",
-- See Fig. 3.7.5-17 for specific package approvals and dimensions.
PIN ASSIGNMENT--Fig. 3.7.5-17

Release 7

3.7.5.18 - 128K TO 2M BY 8/9 BURST SRAM IN BGA

CAPACITY--128K, 256K, 512K, 1M, 2M WORDS OF 8 OR 9 BITS,

PACKAGE--7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED

PIN ASSIGNMENT--Fig. 3.7.5-18

These parts contain BURST addressing capability.

3.7.5.19 - 128K TO 2M BY 8/9 SSRAM IN BGA

CAPACITY--128K, 256K, 512K, 1M, 2M WORDS OF 8 OR 9 BITS,

PACKAGE--7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED

PIN ASSIGNMENT--Fig. 3.7.5-19

Included with this standard is a table of the BOUNDARY SCAN ORDER to be used in testing the parts.

BOUNDARY SCAN ORDER TABLE--Fig. 3.7.5-20

3.7.5.20 - 32K BY 8 SRAM IN TSOP1

CAPACITY--32K WORDS OF 8 BITS

PACKAGE--32 PIN TSOP1, 8 mm X 11.8 mm, 0.55 mm PP

PIN ASSIGNMENTS--Fig. 3.7.5-21

3.7.5.21 - 128K TO 16M BY 9 SYNC SEPARATE I/O SRAM IN 209 BGA

CAPACITY--128K, 256k, 512k, 1M, 2M, 4M, 8M, 16M WORDS OF 9 BITS

PACKAGE--7 X 17 BALL BGA 14 mm X 22 mm, 1 mm Bump Pitch

PIN ASSIGNMENTS--Fig. 3.7.5-22

3.7.5.22 - 128K TO 16M BY 9 SYNC SEPARATE I/O SRAM IN 221 BGA

CAPACITY--128K, 256k, 512k, 1M, 2M, 4M, 8M, 16M WORDS OF 9 BITS

PACKAGE--13 X 17 BALL BGA 13 mm X 15 mm, 0.8 mm Bump Pitch

PIN ASSIGNMENTS--Fig. 3.7.5-23

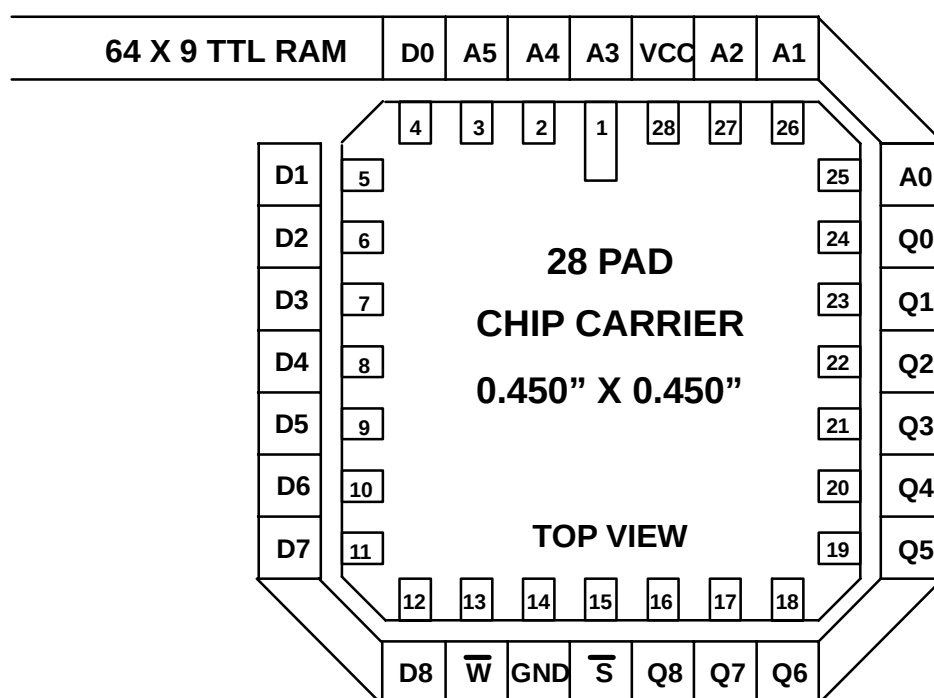


FIGURE 3.7.5-1
64 BY 9 SRAM IN SCC

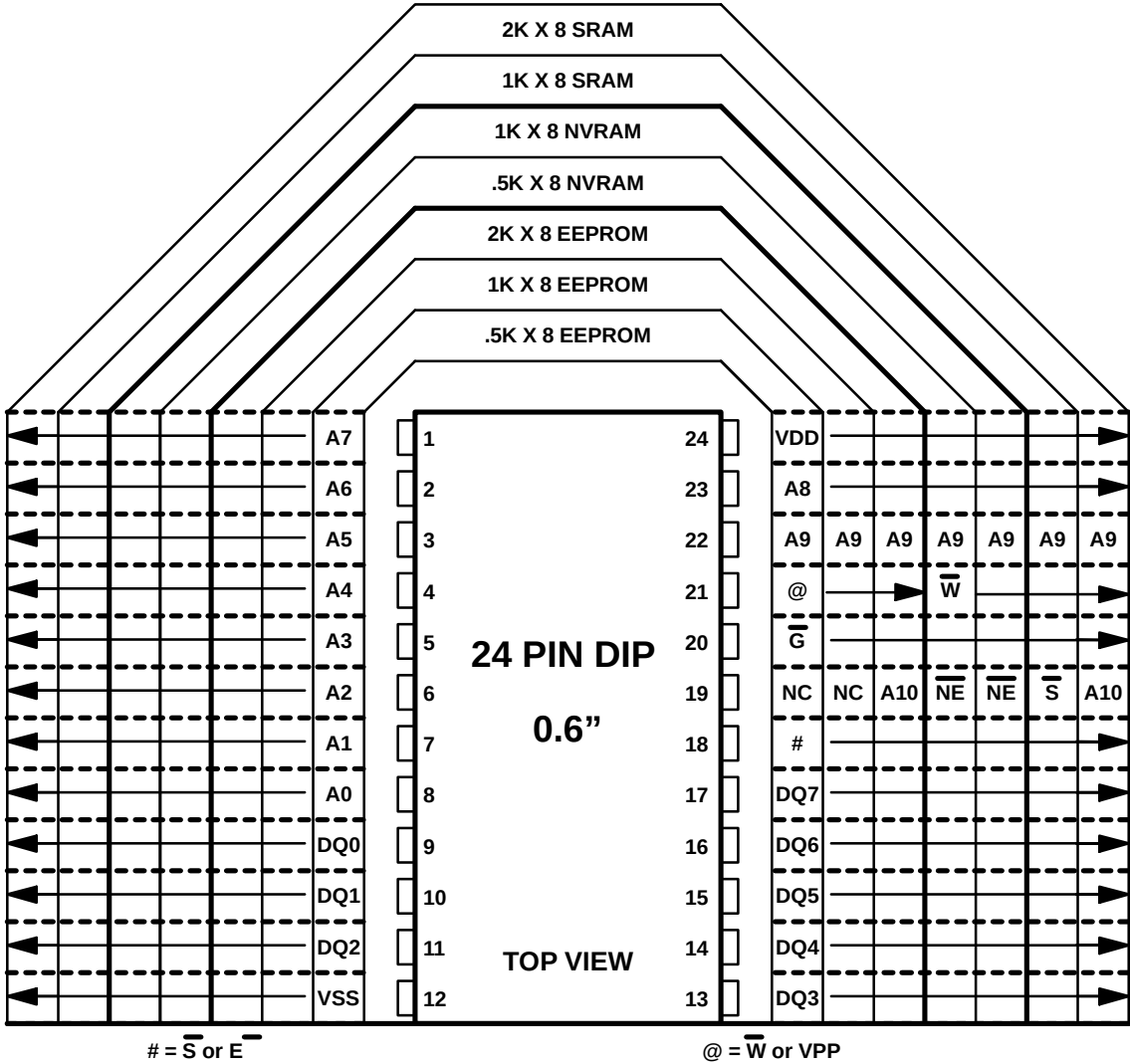


FIGURE 3.7.5-2
1K & 2K BY 8 TTL SRAM IN DIP

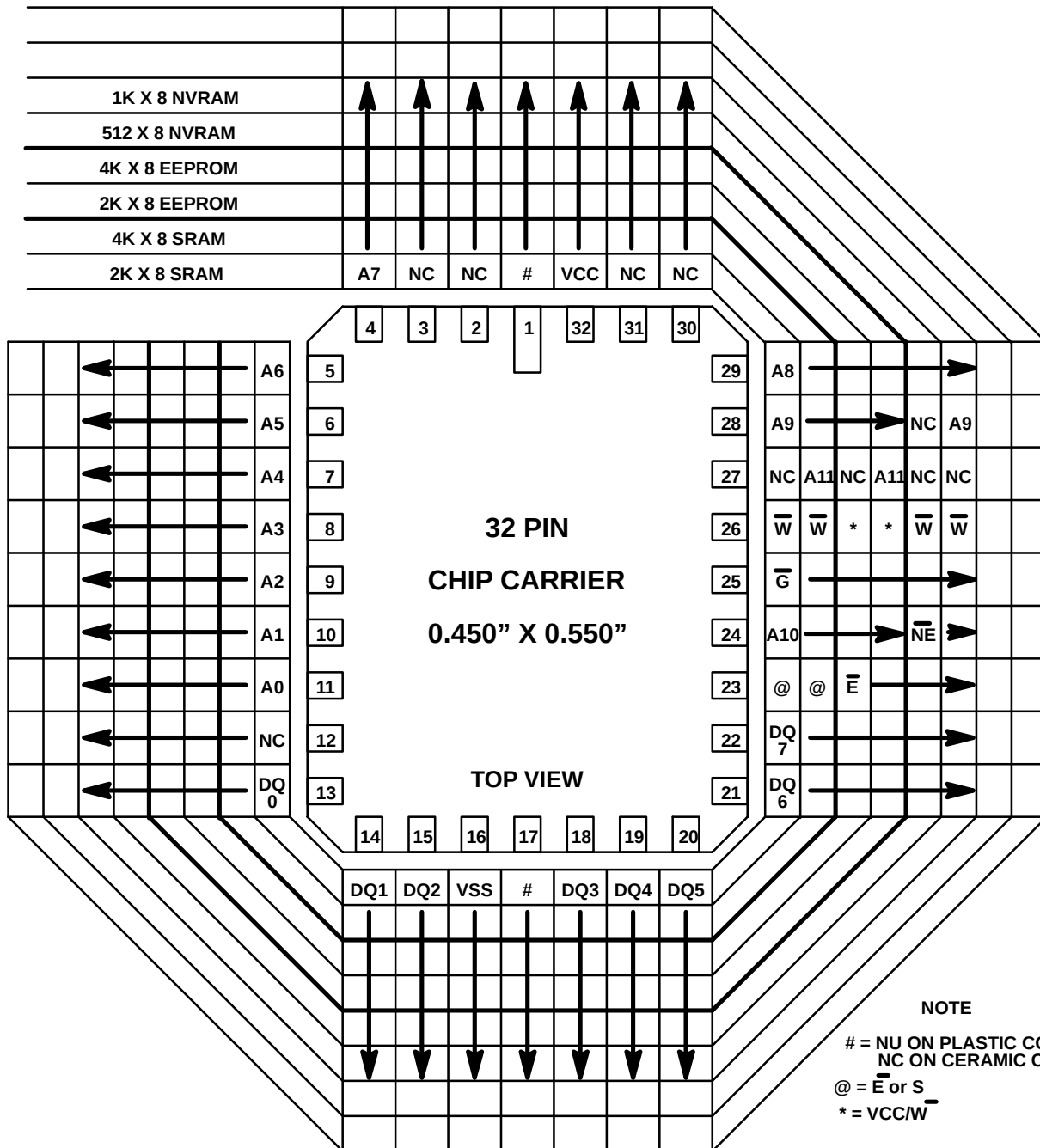


**FIGURE 3.7.5-3
2K & 4K BY 8 TTL SRAM IN RCC**

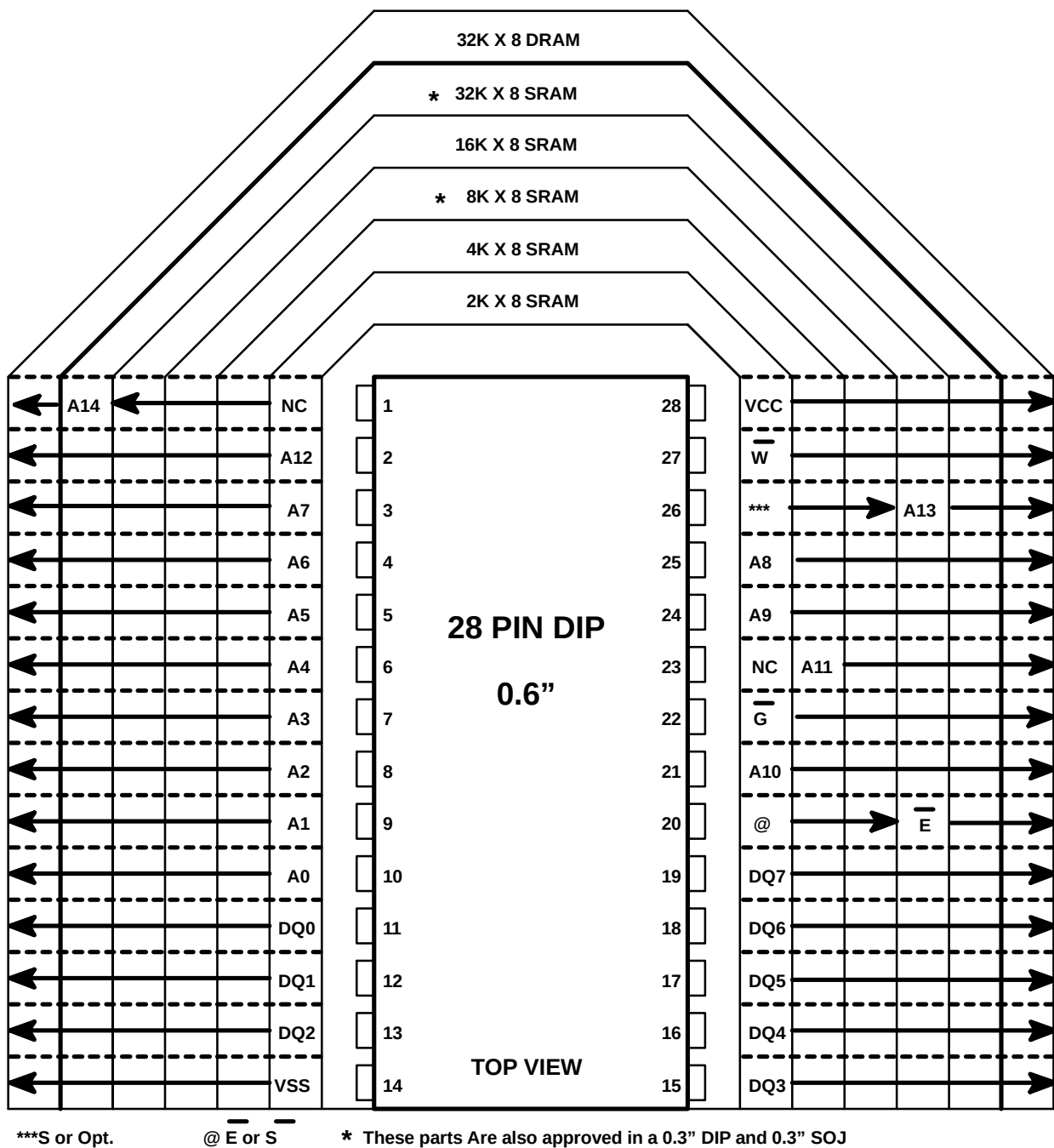


FIGURE 3.7.5-4
2K TO 32K BY 8 TTL SRAM FAMILY IN DIP & SOJ

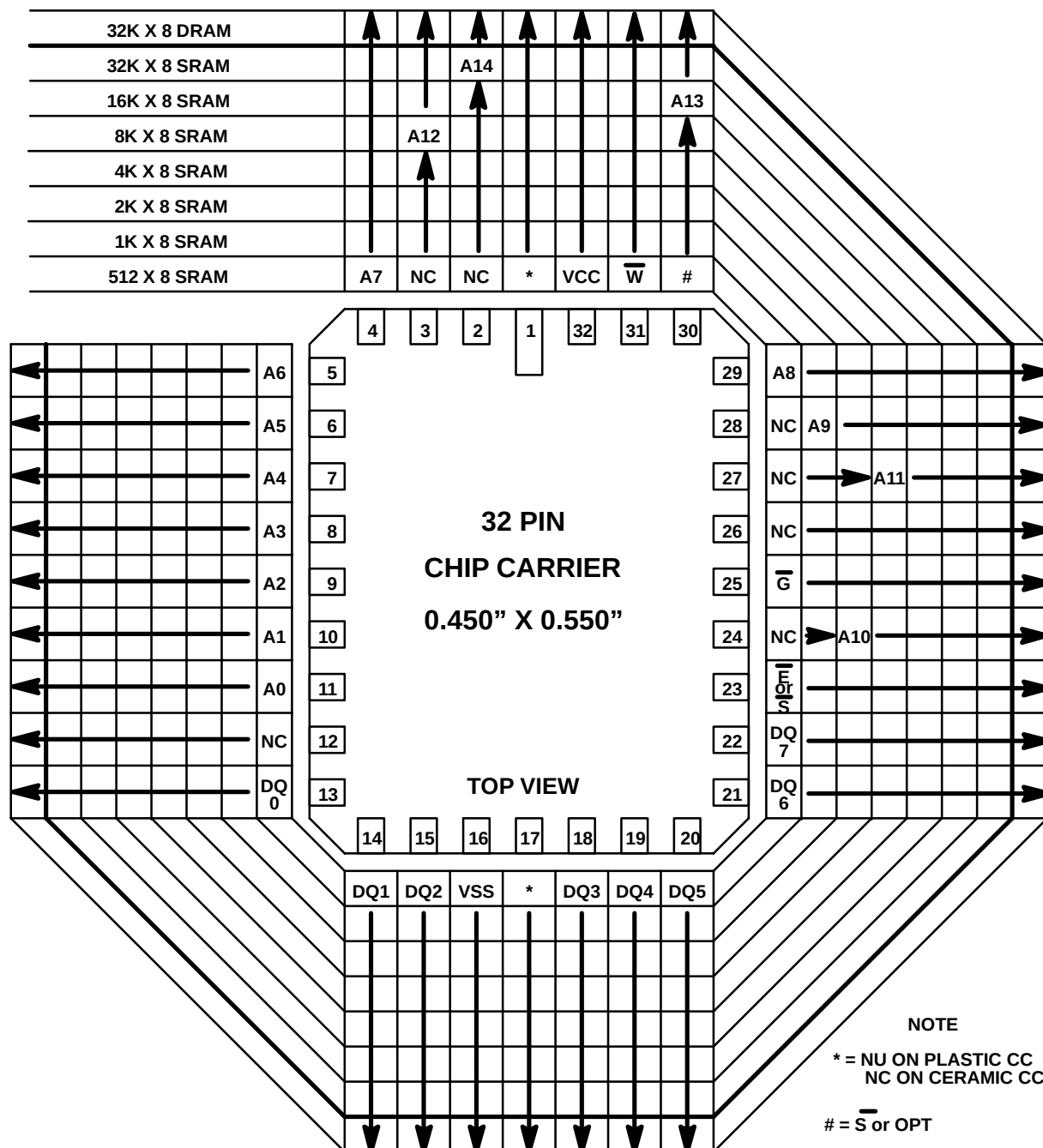


FIGURE 3.7.5-5
0.5K TO 32K BY 8 TTL SRAM FAMILY IN RCC

Release 1