

3.7.7 Word Wide (X16/18) TTL and MOS SRAM

All of the following standards are for devices which operate with TTL or MOS interface levels and power voltages.

3.7.7.1 - 4K TO 64K BY 16 TTL SRAM IN DIP

CAPACITY--4K TO 64K WORDS OF 16 BITS,
ELECTRICAL INTERFACE--TTL
PACKAGE--40 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS--Fig. 3.7.7-1

3.7.7.2 - 4K TO 256K BY 16 TTL SRAM IN SCC

CAPACITY--4K TO 256K WORDS OF 16 BITS,
PACKAGE--44 PAD (PIN) RCC, 0.650" X 0.650"
PIN ASSIGNMENTS--Fig. 3.7.7-2

3.7.7.3 - 16K TO 256K BY 16 ADDRESS/DATA MX TTL SRAM IN DIP

CAPACITY--16K TO 256K WORDS OF 16 BITS,
LOGIC FEATURES--Address and Data MULTIPLEXED onto common pins.
PACKAGE--28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENTS--Figs. 3.7.7-3

3.7.7.4 - 16K TO 256K BY 16 ADDRESS/DATA MX TTL SRAM IN RCC

CAPACITY--16K TO 256K WORDS OF 16 BITS,
LOGIC FEATURES--Address and Data MULTIPLEXED onto common pins.
PACKAGE--32 PIN (PAD) RCC, 0.450" X 0.550"
PIN ASSIGNMENTS--Figs. 3.7.7-4

3.7.7.5 - 16K AND 64K BY 18 SRAM IN SCC

CAPACITY--16K, 64K WORDS OF 18 BITS,
LOGIC FEATURES--ASYNCHRONOUS ADDRESS LATCH
--UPPER BYTE AND LOWER BYTE SELECTABLE
PACKAGE--52 TERMINAL SCC, 0.750" X 0.750"
PIN ASSIGNMENTS--Figs. 3.7.7-5

3.7.7.6 - 64K BY 16 & 18 SRAM IN 44 SOJ

CAPACITY--64K WORDS OF 16 OR 18 BITS,
LOGIC FEATURES--ASYNCHRONOUS WITH OPTIONAL ADDRESS LATCH
--UPPER BYTE AND LOWER BYTE SELECTABLE
--COMMON DATA I/O
PACKAGE--44 PIN SOJ, TBD
PIN ASSIGNMENT--Fig. 3.7.7-6

3.7.7.7 - 32K AND 64K BY 16 & 18 SRAM AND SSRAM IN 52 SCC WITH LOGIC FEATURES

CAPACITY--32K, 64K WORDS OF 16 OR 18 BITS,
NOTE: These parts are optimized for use as CACHE memory for Microprocessors and come in 5 versions, each with a different set of logic features that are optimized for different environments. In addition, there are features common to all parts.
LOGIC FEATURES--ALL VERSIONS ARE UPPER AND LOWER BYTE SELECTABLE
--ALL VERSIONS HAVE COMMON DATA I/O
--SYNCHRONOUS WITH NO SPECIAL LOGIC FEATURES.
--ASYNCHRONOUS WITH DATA LATCH ENABLE.
--SYNCHRONOUS WITH DATA LATCH ENABLE.
--SYNCHRONOUS WITH BURST MODE.
--SYNCHRONOUS WITH BURST MODE, BASE ADDRESS LATCH(S) AND WRITE CLOCK (KW). SEE FIG. 3.7.7-8 FOR KW TIMING.
PACKAGE--52 TERMINAL SCC, 0.750" X 0.750" WITH A 0.050" LEAD PITCH
PIN ASSIGNMENT--Fig. 3.7.7-7

3.7.7.8 - 64K TO 64M BY 16 & 18 SRAM AND SSRAM FAMILIES IN 100 TQFP

CAPACITY--64K, 128K, 256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, OR 64M WORDS OF 16 OR 18 BITS,

LOGIC FEATURES --There are two version of this part available:

--SYNCHRONOUS WITH ADDRESS LATCH OR ASYNCHRONOUS

--UPPER BYTE AND LOWER BYTE SELECTABLE

--COMMON DATA I/O

PACKAGE--100 PIN TQFP, 20 mm v 14 mm

PIN ASSIGNMENT--Fig. 3.7.7-8

3.7.7.9 - 64K TO 64M BY 16/18 BURST SRAM IN 119 BGA

CAPACITY--64K, 128K, 256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, OR 64M WORDS OF 16 OR 18 BITS,

PACKAGE--7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED

PIN ASSIGNMENT--Fig. 3.7.7-9

These parts contain BURST addressing capability.

3.7.7.10 - 128K TO 64M BY 16/18 NETWORK SSRAM IN 119 BGA

CAPACITY--128K, 256K, 512K, 1M, 2M, 4M, 8M, 16M, 32M, OR 64M WORDS OF 16 OR 18 BITS,

PACKAGE--7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED

PIN ASSIGNMENT--Fig. 3.7.7-10

.Included with this standard is a table of the BOUNDARY SCAN ORDER to be used in testing the parts.

BOUNDARY SCAN ORDER TABLE--Fig. 3.7.7-11

3.7.7.11 - 64K TO 16M BY 16/18 BURST SRAM IN QFP OR TQFP

CAPACITY--64K, 128K, 256K, 512K, 1M, 2M, 4M, 8M, OR 16M WORDS OF 16 OR 18 BITS,

PACKAGE--100 PIN QFP or TQFP, 20 mm X 14 mm, 0.65 mm Pin Pitch

PIN ASSIGNMENT--Fig. 3.7.7-12

These parts contain BURST addressing capability.

3.7.7.12 - 256K AND 1M BY 16 and 18 SRAM IN TSOP2

CAPACITY--16K, 64K WORDS OF 18 BITS,

LOGIC FEATURES--UPPER BYTE AND LOWER BYTE SELECTABLE

PACKAGE--54 P TSOP2, 10.16 mm or 12.70 mm, 0.8 mm Pin Pitch

PIN ASSIGNMENTS--Figs. 3.7.7-13

3.7.7.13 - 1Mb TO 128Mb Density, BY 16 or 18 BURST SRAM IN 221 BGA

CAPACITY--64K to 8M WORDS OF 16 or 18 BITS

LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS

PACKAGE--11 x 19 BALL BGA WITH 0.8 mm Ball Pitch.

SPECIAL FEATURES--BURST SRAM Architecture

PIN ASSIGNMENT--Fig. 3.7.7-14

3.7.7.14 - 1Mb TO 1Gb Density, BY 16 or 18 SIGMA SRAM IN 209 BGA, with Common I/O

CAPACITY--64K to 64M WORDS OF 16 or 18 BITS

LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS

PACKAGE--11 x 19 Ball BGA WITH 1 mm Ball Pitch.

SPECIAL FEATURES--SIGMA SRAM Architecture

PIN ASSIGNMENT--Fig. 3.7.7-15

3.7.7.15 - 1Mb TO 128Mb Density, BY 16 or 18 SIGMA SRAM IN 221 BGA, with Common I/O

CAPACITY--64K to 8M WORDS OF 16 or 18 BITS

LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS

PACKAGE--13 x 11 Ball BGA WITH 0.8 mm Ball Pitch.

SPECIAL FEATURES--SIGMA SRAM Architecture

PIN ASSIGNMENT--Fig. 3.7.7-16

3.7.7.16 - 1Mb TO 128Mb Density, BY 18 SIGMA SRAM IN 209 BGA, with Separate I/O

CAPACITY--64K to 8M WORDS OF 18 BITS

LOGIC FEATURES--SEPARATE DATA INPUT & OUTPUT PINS

PACKAGE--11 x 19 Ball BGA WITH 1 mm Ball Pitch.

SPECIAL FEATURES--SIGMA SRAM Architecture

PIN ASSIGNMENT--Fig. 3.7.7-17

3.7.7.17 - 1Mb TO 128Mb Density, BY 18 SIGMA SRAM IN 221 BGA, with Separate I/O

CAPACITY--64K to 8M WORDS OF 18 BITS

LOGIC FEATURES--SEPARATE DATA INPUT & OUTPUT PINS

PACKAGE--13 x 11 Ball BGA WITH 0.8 mm Ball Pitch.

SPECIAL FEATURES--SIGMA SRAM Architecture

PIN ASSIGNMENT--Fig. 3.7.7-18

3.7.7.18 - 8Mb TO 128Mb Density, BY 18 SRAM IN 165 BGA, with Separate I/O

CAPACITY--512K to 8M WORDS OF 18 BITS

LOGIC FEATURES--SEPARATE DATA INPUT & OUTPUT PINS

PACKAGE--11 x 15 Ball BGA WITH 0.8 mm Ball Pitch.

PIN ASSIGNMENT--Fig. 3.7.7-19

3.7.7.19 - 2Mb TO 1Gb Density, BY 16 or 18 Burst SRAM IN 165 BGA, with Common I/O

CAPACITY--128K to 64M WORDS OF 16 or 18 BITS

LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS

PACKAGE--11 x 15 Ball BGA WITH 1 mm Ball Pitch.

SPECIAL FEATURES--Burst SRAM Architecture

PIN ASSIGNMENT--Fig. 3.7.7-20

3.7.7.20 - 2Mb TO 1Gb Density, BY 16 or 18 Network SRAM IN 165 BGA, with Common I/O

CAPACITY--128K to 64M WORDS OF 16 or 18 BITS

LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS

PACKAGE--11 x 15 Ball BGA WITH 1 mm Ball Pitch.

SPECIAL FEATURES--Network SRAM Architecture

PIN ASSIGNMENT--Fig. 3.7.7-21

3.7.7.21 - 52-Pin TSOP II Pin Assignment for Low Power SRAMs

CAPACITY--4M to 256M WORDS OF 16 BITS

LOGIC FEATURES--UPPER BYTE AND LOWER BYTE SELECTABLE

PACKAGE--52 P TSOP II, 10.79 mm X 10.40 mm, 0.4 mm Pin Pitch.

PIN ASSIGNMENT--Fig. 3.7.7-22

Release NIL

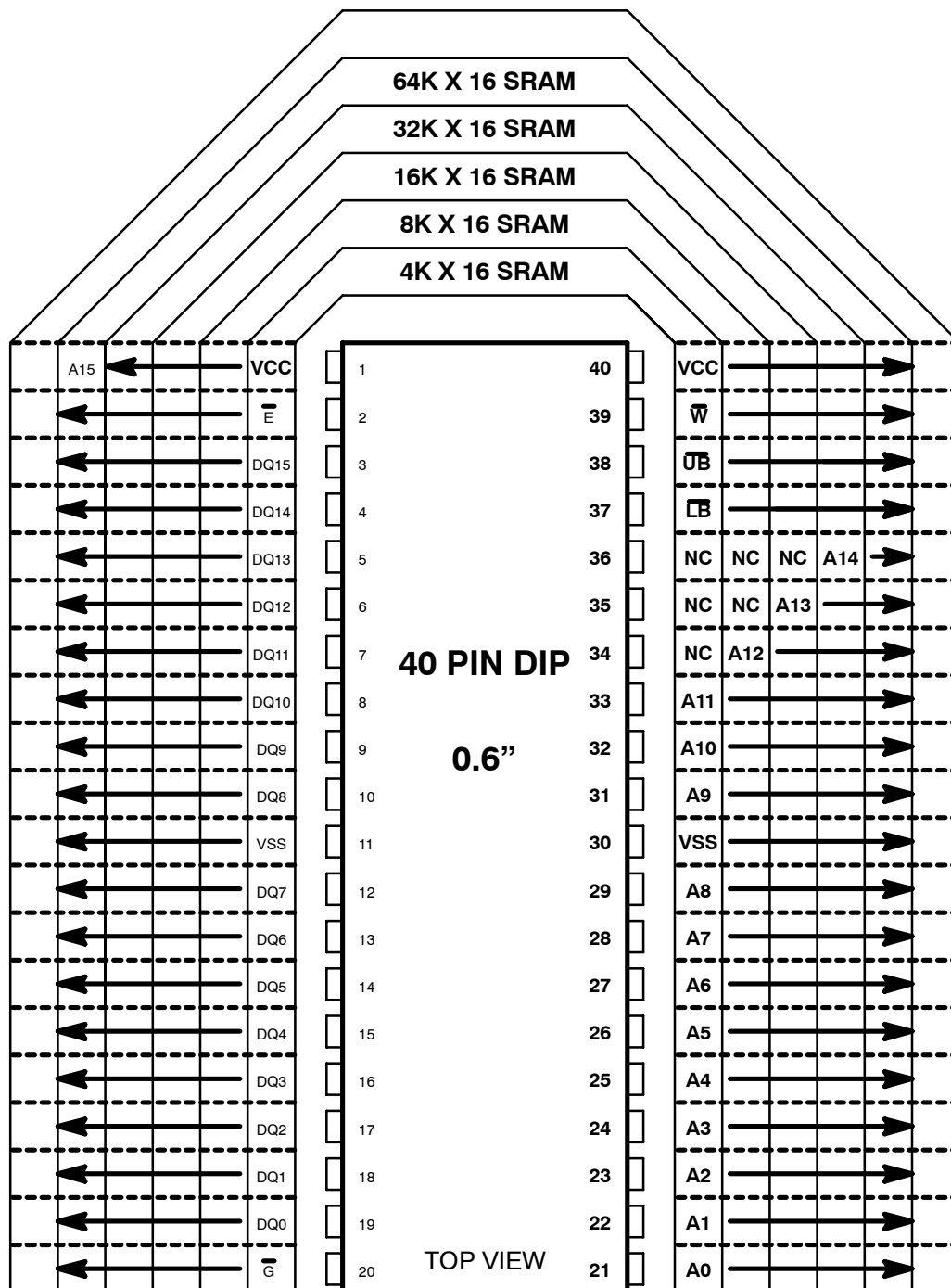


FIGURE 3.7.7-1
4K TO 64K BY 16 TTL SRAM FAMILY IN DIP

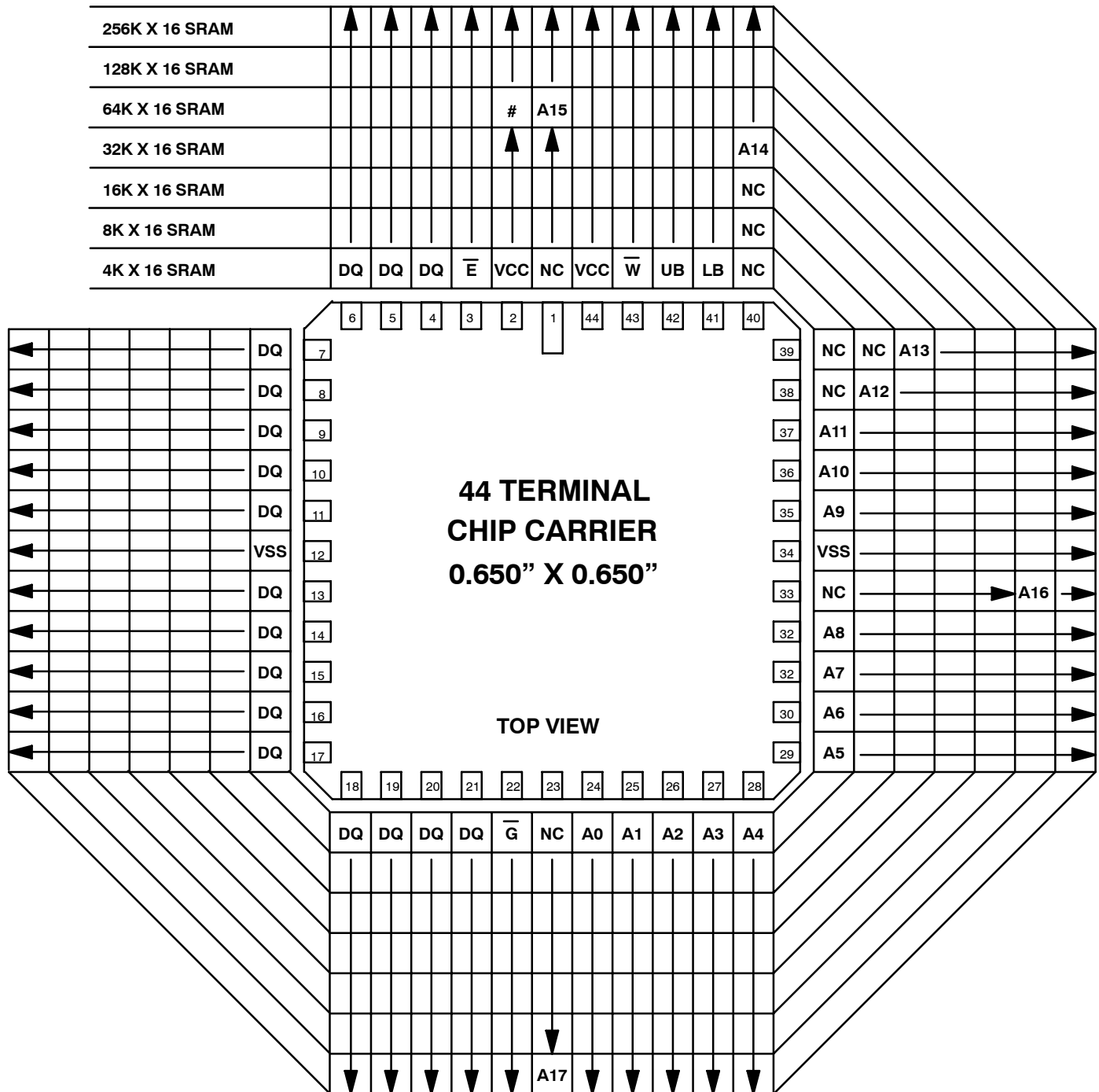
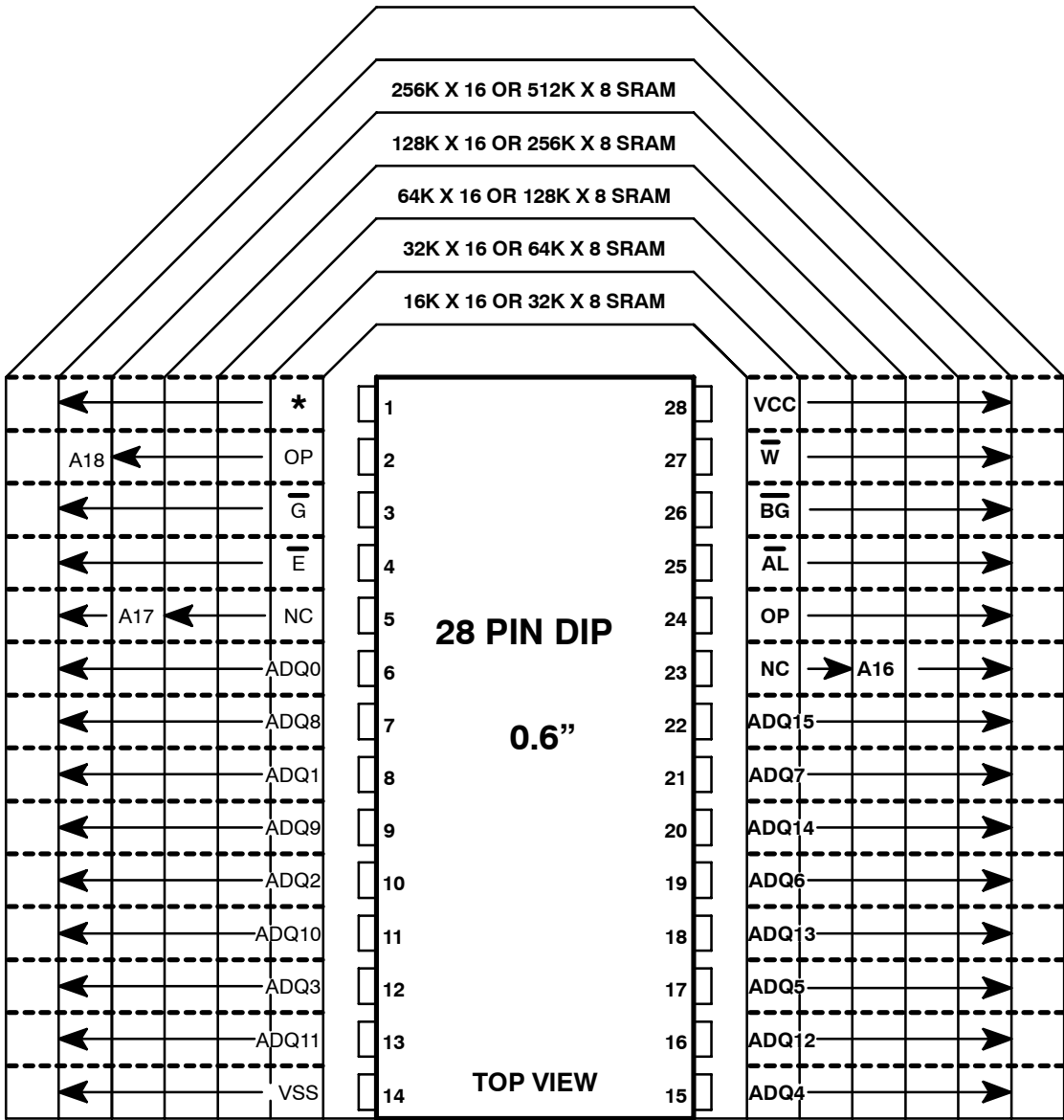


FIGURE 3.7.7-2
4K TO 256K BY 16 TTL SRAM FAMILY IN RCC

Release 1

$\overline{\text{BG}}$	A0	D0-D7	D8-D15	OPERATION
L	L	LOWER BYTE	UPPER BYTE	WORD
L	H		UPPER BYTE	
H	L	LOWER BYTE		BYTE
H	H	UPPER BYTE		BYTE



* NC or VSS

FIGURE 3.7.7-3
16K TO 256K BY 16 ADDRESS/DATA MX SRAM FAMILY IN DIP

$\overline{BG}$	A0	D0-D7	D8-D15	OPERATION
L	L	LOWER BYTE	UPPER BYTE	WORD
L	H		UPPER BYTE	
H	L	LOWER BYTE		BYTE
H	H	UPPER BYTE		BYTE

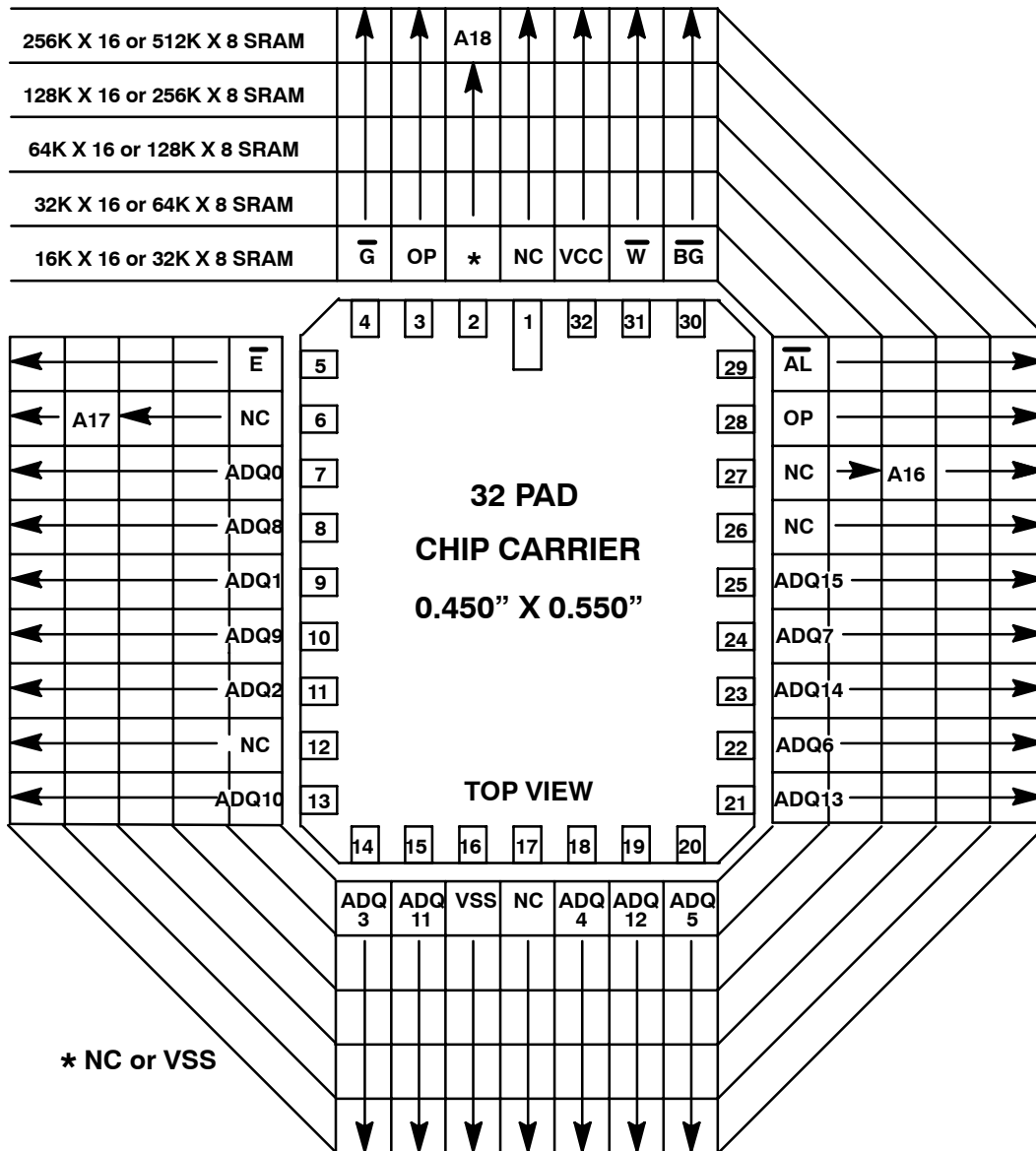


FIGURE 3.7.7-4

16K TO 256K BY 16 ADDRESS/DATA MX SRAM FAMILY IN RCC

Release 1