

3.7.8 Double Word Wide TTL and MOS SRAM

All of the following standards are for devices which operate with TTL or any of the lower voltage MOS interface levels and power supply voltages as defined in the individual standards.

3.7.8.1 - 32K TO 8M BY 32 & 36 BURST SRAM IN TQFP

CAPACITY--32K TO 8M WORDS OF 32 OR 36 BITS,
PACKAGE--100 PIN TQFP, 20 mm X 14 mm WITH 0.65 mm PP
PIN ASSIGNMENT--Fig. 3.7.8-1

These parts combine the features of Synchronous SRAM with BURST addressing capability.
This standard modifies the one published previously in Release 5 ab adding new functions and deleting some that were not used.

3.7.8.2 - 32K TO 32M BY 32 & 36 SRAM AND SSRAM FAMILIES IN 100 TQFP

CAPACITY--32K TO 32M, WORDS OF 32 OR 36 BITS,
LOGIC FEATURES --There are two version of this part available:
--SYNCHRONOUS WITH ADDRESS LATCH OR ASYNCHRONOUS
--UPPER BYTE AND LOWER BYTE SELECTABLE
--COMMON DATA I/O
PACKAGE--100 PIN TQFP, 20 mm X 14 mm 0.65 mm PP
PIN ASSIGNMENT--Fig. 3.7.8-2

3.7.8.3 - 32K TO 32M BY 32 & 36 BURST SRAM IN BGA

CAPACITY--32K TO 32M WORDS OF 32 OR 36 BITS,
PACKAGE--7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT--Fig. 3.7.8-3
These parts contain BURST addressing capability.

3.7.8.4 - 128K TO 32M BY 32 & 36 SSRAM IN 1190 BGA

CAPACITY--128K TO 32M WORDS OF 32 OR 36 BITS,
PACKAGE--7 X 17 BALL BGA 14 mm X 22 mm or UNDEFINED
PIN ASSIGNMENT--Fig. 3.7.8-4

.Included with this standard is a table of the BOUNDARY SCAN ORDER to be used in testing the parts.
BOUNDARY SCAN ORDER TABLE--Fig. 3.7.8-5

3.7.8.5 - 16K TO 64K BY 36 & 72 BURST SRAM IN QFP

CAPACITY--32K, 64K, OR 128K, WORDS OF 32 OR 36 BITS,
PACKAGE--120 PIN TQFP, 20 mm X 14 mm WITH 0.5 mm PP
PIN ASSIGNMENT--Fig. 3.7.8-6
These parts combine the features of Synchronous SRAM with BURST addressing capability.

3.7.8.6 - 16K TO 256K BY 36 & 72 BURST SRAM IN BGA

CAPACITY--16K, 32K, 64K, 128K, OR 256K WORDS OF 32 or 36 BITS,
PACKAGE--15 X 17 BALL BGA 20 mm X 25 mm OR UNDEFINED
PIN ASSIGNMENT--Fig. 3.7.8-7

These parts combine the features of Synchronous SRAM with BURST addressing capability.

3.7.8.7 - 1Mb TO 128Mb Density, BY 32 or 36 BURST SRAM IN 221 BGA

CAPACITY--32K to 4M WORDS OF 32 or 36 BITS
LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS
PACKAGE--15 x 17 Ball BGA WITH 0.8 mm Ball Pitch.
SPECIAL FEATURES--BURST SRAM Architecture
PIN ASSIGNMENT--Fig. 3.7.8-8

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3.7.8.8 - 1Mb TO 128Mb Density, BY 32 or 36 SIGMA SRAM IN 209 BGA, with Common I/O

CAPACITY--32K to 4M WORDS OF 32 or 36 BITS
LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS
PACKAGE--11 x 19 Ball BGA WITH 1 mm Ball Pitch.
SPECIAL FEATURES--SIGMA SRAM Architecture
PIN ASSIGNMENT--Fig. 3.7.8-9

3.7.8.9 - 1Mb TO 128Mb Density, BY 32 or 36 SIGMA SRAM IN 221 BGA, with Common I/O

CAPACITY--32K to 4M WORDS OF 32 or 36 BITS
LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS
PACKAGE--11 x 17 Ball BGA WITH 0.8 mm Ball Pitch.
SPECIAL FEATURES--SIGMA SRAM Architecture
PIN ASSIGNMENT--Fig. 3.7.8-10

3.7.8.10 - 1Mb TO 128Mb Density, BY 36 SIGMA SRAM IN 209 BGA, with Separate I/O

CAPACITY--32K to 4M WORDS OF 36 BITS
LOGIC FEATURES--SEPARATE DATA INPUT & OUTPUT PINS
PACKAGE--11 x 19 Ball BGA WITH 1 mm Ball Pitch.
SPECIAL FEATURES--SIGMA SRAM Architecture
PIN ASSIGNMENT--Fig. 3.7.8-11

3.7.8.11 - 1Mb TO 128Mb Density, BY 36 SIGMA SRAM IN 221 BGA, with Separate I/O

CAPACITY--32K to 4M WORDS OF 36 BITS
LOGIC FEATURES--SEPARATE DATA INPUT & OUTPUT PINS
PACKAGE--11 x 17 Ball BGA WITH 0.8 mm Ball Pitch.
SPECIAL FEATURES--SIGMA SRAM Architecture
PIN ASSIGNMENT--Fig. 3.7.8-12

3.7.8.12 - 16Mb TO 256Mb Density, BY 36 SRAM IN 165 BGA, with Separate I/O

CAPACITY--512K to 8M WORDS OF 36 BITS
LOGIC FEATURES--SEPARATE DATA INPUT & OUTPUT PINS
PACKAGE--11 x 15 Ball BGA WITH 1 mm Ball Pitch.
PIN ASSIGNMENT--Fig. 3.7.8-13

3.7.8.13 - 8Mb TO 128Mb Density, BY 36 DDR SRAM IN 165 BGA, with Common I/O

CAPACITY--128K to 4M WORDS OF 36 BITS
LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS
PACKAGE--11 x 15 Ball BGA WITH 1 mm Ball Pitch.
PIN ASSIGNMENT--Fig. 3.7.8-14

3.7.8.14 - 2Mb TO 1Gb Density, BY 32 or 36 Burst SRAM IN 165 BGA, with Common I/O

CAPACITY--64K to 32M WORDS OF 32 or 36 BITS
LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS
PACKAGE--11 x 15 Ball BGA WITH 1 mm Ball Pitch.
SPECIAL FEATURES--Burst SRAM Architecture
PIN ASSIGNMENT--Fig. 3.7.8-15

3.7.8.15 - 2Mb TO 1Gb Density, BY 32 or 36 Network SRAM IN 165 BGA, with Common I/O

CAPACITY--64K to 32M WORDS OF 32 or 36 BITS

LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS

PACKAGE--11 x 15 Ball BGA WITH 1 mm Ball Pitch.

SPECIAL FEATURES--Network SRAM Architecture

PIN ASSIGNMENT--Fig. 3.7.8-16

Densities 1Mb through 256Mb; Pin Assignment, Top View

[illegible]

The Pins labeled "DQP_x, NC" are intended to be used as parity bits for the x36 parts.
Pin 14: 1 = Pipelined, 0 = Flow Through

FIGURE 3.7.8-1
32K TO 8M BY 32 or 36 BURST SRAM IN TQFP

Densities 1Mb through 1Gb; Pin Assignment, Top View

[illegible]

The Pins labeled "DQP_x, NC" are intended to be used as parity bits for the x36 parts.

M2=FT#, M3-high

M4=FT# for Flow Through and Pipelined Network SRAM

FIGURE 3.7.8-2
32K TO 32M BY 32 & 36 SRAM AND SSRAM IN TQFP