

3.7.9 Eight Byte Wide (X64/72) MOS SRAM

All of the following standards are for devices which operate with TTL or MOS interface levels and power voltages.

3.7.9.1 - 1Mb TO 1Gb Density, BY 64 or 72 BURST SRAM IN 209 BGA

CAPACITY--16K to 16M WORDS OF 64 or 72 BITS
LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS
PACKAGE--209 PIN BGA WITH 1 mm Ball Pitch.
SPECIAL FEATURES--BURST SRAM Architecture
PIN ASSIGNMENT--Fig. 3.7.9-1

3.7.9.2 - 1Mb TO 128Mb Density, BY 64 or 72 BURST SRAM IN 221 BGA

CAPACITY--16K to 2M WORDS OF 64 or 72 BITS
LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS
PACKAGE--221 PIN BGA WITH 1 mm Ball Pitch.
SPECIAL FEATURES--BURST SRAM Architecture
PIN ASSIGNMENT--Fig. 3.7.9-2

3.7.9.3 - 1Mb TO 128Mb Density, BY 64 or 72 SIGMA SRAM IN 209 BGA

CAPACITY--16K to 2M WORDS OF 64 or 72 BITS
LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS
PACKAGE--209 PIN BGA WITH 1 mm Ball Pitch.
SPECIAL FEATURES--SIGMA SRAM Architecture
PIN ASSIGNMENT--Fig. 3.7.9-3

3.7.9.4 - 1Mb TO 128Mb Density, BY 64 or 72 SIGMA SRAM IN 221 BGA

CAPACITY--16K to 2M WORDS OF 64 or 72 BITS
LOGIC FEATURES--COMMON DATA INPUT & OUTPUT PINS
PACKAGE--221 PIN BGA WITH 1 mm Ball Pitch.
SPECIAL FEATURES--SIGMA SRAM Architecture
PIN ASSIGNMENT--Fig. 3.7.9-4

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