JEDEC PUBLICATION

Failure Mechanisms and Models for Semiconductor Devices

JEP122G

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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FAILURE MECHANISMS AND MODELS FOR SEMICONDUCTOR DEVICES

Foreword

This publication provides guidance in the selection of reliability modeling parameters, namely functional form, apparent thermal activation energy values and sensitivity to stresses such as power supply voltage, substrate current, current density, gate voltage, relative humidity, temperature cycling range, mobile ion concentration, etc.

The failure mechanisms described in the several sections of this publication constitute commonly accepted industrial models, validated by a team of reliability experts (SEMATECH/ISMI Reliability Council) and buttressed by citations to the most cogent published literature.

Revisions have been made to reflect technology changes, especially as Cu now supplements Al and low dielectric constant insulators are complementing traditional silica.

Introduction

Accelerated tests are typically used to find and identify potential failure mechanisms in semiconductor devices and to estimate the rate of their occurrence in electronic systems. The historical approach to investigating the relationship between a maximum stress failure rate and a system failure rate is to choose a single representative "equivalent" thermal activation energy for a given product or product group. A single, best-estimate activation energy value facilitates accurate estimation of the acceleration factor for the device failure rate estimation in the system application.

A word about formats within this document: parentheses **( )** enclose equation numbers; square brackets **[ ]** enclose citation numbers. All equation, citation, and figure numbers include the subclause number so that individual clauses can be modified without disturbing other clauses, except for page numbers. Thus, **(5.3.2)** is the 2nd equation in 5.3 and **[5.11.5]** is the 5th citation in 5.11. The citations can be found in Annex A.

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(From JEDEC Board Ballot JCB-01-97, JCB-03-39, JCB-08-61, JCB-09-19, JCB-10-64, and JCB-11-74 formulated under the cognizance of JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

This publication provides a list of failure mechanisms and their associated activation energies or acceleration factors that may be used in making system failure rate estimations when the only available data is based on tests performed at accelerated stress test conditions. The method to be used is the Sum-of-the-Failure-Rates method.

The models apply primarily to the following:

a) Aluminum (doped with small amounts of Cu and/or Si) and copper alloy metallization

b) Refractory metal barrier metals with thin anti-reflection coatings

c) Doped silica or silicon nitride interlayer dielectrics, including low dielectric constant materials

d) Poly silicon or “salicide” gates (metal-rich silicides such as W, Ni & Co to decrease resistivity)

e) Thin SiO_2 gate dielectric

f) Silicon with p-n junction isolation

g) Tin Whisker Growth Kinetics

h) Printed Circuit Board Ionic Mobility

2 Terms and definitions

For the purpose of this publication, the following terms and definitions apply.

acceleration factor (*A*, AF): For a given failure mechanism, the ratio of the time it takes for a certain fraction of the population to fail, following application of one stress or use condition, to the corresponding time at a more severe stress or use condition.

NOTE 1 Times are generally derived from modeled time-to-failure distributions (lognormal, Weibull, exponential, etc.).

NOTE 2 Acceleration factors can be calculated for temperature, electrical, mechanical, environmental, or other stresses that can affect the reliability of a device.

NOTE 3 Acceleration factors are a function of one or more of the basic stresses that can cause one or more failure mechanisms. For example, a plot of the natural log of the time-to-failure for a cumulative constant percentage failed (e.g., 50%) at multiple stress temperatures as a function of $1/kT$, the reciprocal of the product of Boltzmann’s constant in electronvolts per kelvin and the absolute temperature in kelvins, is linear if one and only one failure mechanism is involved. The best-fit linear slope is equal to the apparent activation energy in electronvolts.

NOTE 4 The abbreviation AF is often used in place of the symbol *A*.

acceleration factor, stress (A_f): The acceleration factor due to the presence of some stress (e.g. current density, electric field, humidity, temperature cycling).

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2 Terms and definitions (cont'd)

acceleration factor, temperature (A_T): The acceleration factor due to changes in temperature.

NOTE 1 This is the acceleration factor most often referenced. The Arrhenius equation for reliability is commonly used to calculate the acceleration factor that applies to the acceleration of time-to-failure distributions for microcircuits and other semiconductor devices:

$$A_T = \lambda_{T1}/\lambda_{T2} = \exp[(-E_{aa}/k)(1/T_1 - 1/T_2)] \quad \textbf{(2.1)}$$

where

E_{aa} is the apparent activation energy (eV);
k is Boltzmann's constant (8.62×10^{-5} eV/K);
T_1 is the absolute temperature of test 1 (K);
T_2 is the absolute temperature of test 2 (K);
λ_{T1} is the observed failure rate at test temperature T_1 (h^{-1});
λ_{T2} is the observed failure rate at test temperature T_2 (h^{-1}).

NOTE 2 The best-fit linear slope of a plot of the natural log of the time-to-failure as a function of $1/kT$, the reciprocal of the product of Boltzmann's constant in electronvolts per kelvin and the absolute temperature in kelvins, is equal to the apparent activation energy in electronvolts.

NOTE 3 $\lambda_q = \lambda_o \cdot A_T$, where λ_q is the quoted (predicted) system failure rate at some system temperature T_s, λ_o is the observed failure rate at some test temperature T_t, and A_T is the temperature acceleration factor from T_t to T_s.

activation energy (E_a): The excess free energy over the ground state that must be acquired by an atomic or molecular system in order that a particular process can occur.

NOTE The activation energy is used in the Arrhenius equation for the thermal acceleration of physical reactions. The term "activation energy" is not applicable when describing thermal acceleration of time-to-failure distributions, e.g., in the Arrhenius equation for reliability; hence the need for the term "apparent activation energy".

apparent activation energy (E_{aa}): An energy value, analogous to activation energy, that can be inserted in the Arrhenius equation for reliability to calculate an acceleration factor applicable to changes with temperature of time-to-failure distributions.

NOTE 1 An apparent activation energy should be associated with a specific failure mechanism and an observed time-to-failure distribution to calculate the acceleration factor for converting the observed failure rate to the quoted failure rate at a different temperature.

NOTE 2 An activation energy is a measure of the heat energy needed to establish the rate of reaction for a specific failure mechanism. The reaction rate and other contributing factors, e.g., radiation, voltage, humidity, magnetic fields, determine the unique time-to-failure distribution for the modeled failure mechanism.

NOTE 3 The apparent activation energy is empirically determined from the change in an observed time-to-failure distribution with temperature.

bathtub curve: A plot of failure rate versus time or cycles that exhibits three phases of life: infant mortality (decreasing failure rate), intrinsic or useful life (relatively constant failure rate), and wear-out (increasing failure rate).

Boltzmann's constant (k): A constant equal to 1.38×10^{-23} joule per kelvin or 8.62×10^{-5} electronvolt per kelvin.

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2 Terms and definitions (cont'd)

cumulative distribution function of the time-to-failure; cumulative mortality function [F(*t*)]: The probability that a device will have failed by a specified time t_1, or the fraction of units that have failed by that time.

NOTE 1 The value of this function is given by the integral of f(*t*) from $t = 0$ to $t = t_1$ and is generally expressed in percent (%) or in parts per million (ppm) for a defined early-life failure period. See "probability density functionof the time-to-failure" for f(*t*).

NOTE 2 The abbreviation CDF is often used; however, the symbol F(*t*) is preferred.

cumulative hazard function [H(*t*)]: The fraction of units that have failed referenced to the survivors (not to the initial number of units).

NOTE The value of this function at a specified time t_1 is given by the integral of h(*t*) from $t = 0$ to $t = t_1$. See "instantaneous failure rate; hazard rate" for h(*t*).

cumulative reliability function [R(*t*)]: The probability that a device will still be functional at a specified time t_1, or the fraction of units surviving to that time.

NOTE R(*t*) = 1 – F(*t*). See "cumulative distribution function of the time-to-failure" for F(*t*).

failure mechanism: The physical, chemical, electrical, or other process that has led to a nonconformance.

NOTE 1 See JESD671, Component Quality Problem Analysis and Corrective Action Requirements.

NOTE 2 A failure mechanism may be characterized by how a degradation process proceeds including the driving force, e.g., oxidation, diffusion, electric field, current density. When the driving force is known, a mechanism may be described by an explicit failure rate model; identifying that model with associated parameters is the main objective of this document.

failure mode: (general) The way in which a failure mechanism manifests itself in a failing component.

NOTE 1 Examples of failure modes are a visual blemish, a bent lead, a foreign particle or material, an incorrect dopant profile or grain size, a scratch, an electrical fault (open, short, leakage, inadequate slew rate or noise margin, stuck at high or low, etc.).

NOTE 2 Failure rate distributions for a given failure mode can be modeled only when the failure mechanism and the relevant independent variables (forcing functions) are known.

failure rate (*λ*): The fraction of a population that fails within a specified interval, divided by that interval.

NOTE 1 Standard methods of reporting failure rates of semiconductor devices include 1) percent failed per 1000 hours and 2) FITs.

NOTE 2 The interval may be expressed in operating hours, storage hours, operating cycles, or other units of interval measurement.

NOTE 3 Typically, the term "failure rate" means the instantaneous failure (hazard) rate.

NOTE 4 The statistical upper limit estimate of the failure rate is usually calculated using the χ^2 (chi-squared) function.

failures in time (FITs): The number of failures per 10^9 device hours.

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2 Terms and definitions (cont'd)

instantaneous failure rate; hazard rate [h(*t*)]: The rate at which devices are failing referenced to the survivors (not to the initial number of units).

NOTE h(*t*) = f(*t*)/R(*t*). See "probability density function of the time-to-failure" for f(*t*) and "cumulative reliability function" for R(*t*).

mean-time-between-failures (MTBF): The average time between failures in repairable or redundant systems.

mean-time-to-failure (MTTF): The average time to failure for components or nonrepairable systems.

NOTE The MTTF is often the reciprocal of the hazard rate when the hazard rate is described by the Poisson or equivalent exponential function, e.g., in the constant or flat portion of the useful life region of the bathtub curve.

whisker: A spontaneous columnar or cylindrical filament, usually of monocrystalline metal, emanating from the surface of a finish.

NOTE Whiskers are not to be confused with dendrites, which are fern-like growths on the surface of a material, formed as a result of electromigration of an ionic species or during solidification.

observed failure rate: The failure rate determined from a product or test vehicle subjected to an accelerating stress that may produce failures attributable to one or more failure mechanisms.

PCB component cleanliness: The absence of chemical residues, on or in the surface of components on printed circuit boards, that result from their processing and handling.

NOTE These residues may react with the environmental moisture or processing conditions and have either positive or negative impact on product performance.

planning activation energy (E_{ap}): A psuedo apparent activation energy, derived from Pareto analysis and experience, using the principles of the physical relationship between stress and failure rate.

NOTE 1 E_{ap} can be used to estimate sample sizes and test times.

NOTE 2 The planning activation energy cannot be calculated as the average value of the apparent activation energies of the various failure mechanisms because different failure mechanisms have different weighting factors and the apparent activation energy values affect the acceleration factor exponentially rather than linearly.

potential physical failure mechanism: A physical failure mechanism that (1) has been identified through physical experimentation to exist for similar products or (2) can be linked to these products through the scientific study of the product (process) physical characteristics and the physical requirement found to be necessary for the failure mechanism to occur.

printed circuit board (PCB): A board for mounting of components, on which most connections are made by printed circuitry (Ref. IEEE 100).

NOTE A printed circuit board (PCB) is also known as a printed wiring board (PWB) (Ref. JEDEC JS9703).

probability density function of the time-to-failure [f(*t*)]: The distribution of the probabilities of failure as a function of time.

NOTE The probability of failure during the interval Δt that immediately follows the instant t_1 is given by the integral of f(*t*) from t_1 to ($t_1 + \Delta t$).

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2 Terms and definitions (cont'd)

quoted failure rate: The predicted failure rate for typical operating conditions.

NOTE The quoted failure rate is calculated from the observed failure rate under accelerated stress conditions multiplied by an accelerated factor; e.g., $\lambda_q = \lambda_o \cdot A_T$, where λ_q is the quoted (predicted) system failure rate at some system temperature T_s, λ_o is the observed failure rate at some test temperature T_t, and A_T is the temperature acceleration factor from T_t to T_s. When multiple failure mechanisms and thus multiple acceleration factors are involved, then a proper summation technique, e.g., sum-of-the-failure rates method, is required.

random defect: A physical defect that is correlated to some known process, equipment, or procedure, and can be described by a probability-density function of time or location.

relative humidity (RH): The ratio of the amount of water vapor in the air to the maximum amount of water vapor that volume of air can hold at that temperature and pressure.

NOTE RH is calculated as the quotient of the vapor density (or vapor pressure) in the air and the value of saturated vapor density (or saturated vapor pressure) at that specific temperature and pressure.

time-to-whisker-nucleation (TTWN): The incubation time before whiskers begin to grow.

useful life: The phase in the life of a device during which the hazard rate is relatively constant.

NOTE As typically used with the bathtub curve, the useful life phase is the bottom of the curve.

wearout: The phase in the life of a device during which the mortality function is increasing.

NOTE As typically used with the bathtub curve, the wearout phase follows the useful life of the device.

3 Inclusions, deliberate omissions, and resources

A reader may easily notice that some important issues are not treated in this document. This section is intended to show our rationale for picking what was included, what was not included, and provide references to relevant JEDEC documents.

3.1 What is included

One can readily see in Section 5 which failure mechanisms are covered in this document. The failure mechanisms were sorted in roughly a semiconductor process flow from silicon to a packaged device: Front End of Line (FEoL), Back End of Line (BEoL), and Packaging/Interfacial failure mechanisms. Only failure mechanisms, for which understanding is relatively mature, are included. Also included are sections on Statistics & Modeling Parameter Determination.

3.2 What is not included

Conspicuous by their absence are several failure mechanisms: namely those active for high dieletric constant gate materials (TDDB and carrier mobility) and "metal" gates, other nonvolatile memory technologies (magnetic, cross bar, ferroelectric, etc.), mechanical shock, Single Event Upsets or Soft Error Rate (SEU or SER), ESD/EOS (ElectroStatic Discharge and Electrical OverStress) which might be measured by HBM (Human Body Model) or CDM (Charged Device Model) and Latch-Up (LU).

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3 Inclusions, deliberate omissions, and resources (cont'd)

3.2 What is not included (cont'd)

High dielectric constant materials are under active development and proliferation. The best of the candidates appear to be rare earth oxides (commonly Hafnium) or silicates, sometimes nitrided, but there are still several possibilities and several possible (poorly characterized) reliability failure mechanisms.

Metal gates are also in a considerable state of flux. "Metal" in this context can mean a conductive nitride and is in contrast to the traditional polycrystalline silicon gate. That there might be two different metal gates for a given high dielectric constant gate (one work function for n-type, but a different work function for p-type) adds considerable complexity to characterization and modeling of the relevant failure mechanisms.

New nonvolatile memory materials and architectures are likely in the near future, but existing Si-gate CMOS can scale a little further along the ITRS before the industry would be forced to supplant traditional technology with something completely new. Naturally, there are many unknown factors in process optimization and in reliability modeling for something completely new.

JEDEC document JESD89A shows how one should measure the failure rate for SEU. However, this document doesn't show a reader how to compute an acceleration factor (AF), which is the primary focus of this document. In principle, an SEU acceleration factor would simply be the ratio of the fluxes between one condition and the other.

One could use JEDEC JESD22-A114 or JESD22-C101 to measure vulnerability to ESD, but neither of these documents shows a method to calculate an acceleration factor. Indeed, it may not be possible to calculate an AF for a periodic stress such as ESD. Furthermore, the current state of knowledge does not allow one to compute cumulative damage leading to failure from some number of sub-lethal pulses. Similarly, we would submit that the physics are not well characterized to the point where current, current density, voltage, electric field, stress duration, etc. could be combined into a stress intensity for AF determination.

JESD78A is the JEDEC standard for a methodology to estimate LU sensitivity. The failure mechanisms created during a LU event can look like those caused by ESD or EOS. Generally, issues related to LU are best corrected through proper characterization during process development and implementation of strict design rules and methodologies associated with LU prevention. JESD78A, like the ESD standards, does not utilize an acceleration factor.

As these issues become mature and relevant, it is our intention to include them in this document.

3.3 JEDEC resources

JESD22-A101-B Steady State Temperature Humidity Bias Life Test, April 1997
JESD22-A103C High Temperature Storage Life, November 2004
JESD22-A104C Temperature Cycling, May 2005
JESD22-A105C Power and Temperature Cycling, January 2004
JESD22-A106B Thermal Shock, June 2004
JESD22-A108C Temperature, Bias, and Operating Life, June 2005
JESD22-A110-B Highly Accelerated Temperature and Humidity Stress Test (HAST), February 1999
JESD22-A113E Preconditioning of Plastic Surface Mount Devices Prior to Reliability Testing, March 2006
JESD22-A114E Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM), January 2007

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3 Inclusions, deliberate omissions, and resources (cont'd)

3.3 JEDEC resources (cont'd)

JESD22-A117A	Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance and Data Retention Test, March 2006
JESD22-A118	Accelerated Moisture Resistance - Unbiased Hast, December 2000
JESD22-A119	Low Temperature Storage Life, November 2004
JESD22-A120A	Test Method For The Measurement Of Moisture Diffusivity And Water Solubility In Organic Materials Used In Integrated Circuits, January 2008
JESD22-A121.01	Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes, October 2005
JESD22-B102E	Solderability, October 2007
JESD22-B105C	Lead Integrity, June 2006
JESD22-B112	High Temperature Package Warpage Measurement Methodology, May 2005
JESD22-B115	Solder Ball Pull, May 2007
JESD22-B116	Wire Bond Shear Test, July 1998
JESD22-B117A	Solder Ball Shear, October 2006
JESD22-C101C	Field-Induced Charged-Device Model Test Method For Electrostatic Discharge Withstand Thresholds Of Microelectronic Components, December 2004
JESD28-1	N-Channel MOSFET Hot Carrier Data Analysis, (Addendum to JESD28), September 2001
JESD28-A	Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation Under DC Stress, December 2001
JESD33-B	Standard Method For Measuring And Using The Temperature Coefficient Of Resistance To Determine The Temperature Of A Metallization Line, February 2004
JESD35-1	General Guidelines for Designing Test Structures for the Wafer-Level Testing of Thin Dielectrics, (Addendum No. 1 to JESD35), September 1995
JESD35-2	Test Criteria for the Wafer-Level Testing of Thin Dielectrics, (Addendum No. 2 to JESD35), February 1996
JESD35-A	Procedure for the Wafer-Level Testing of Thin Dielectrics, April 2001
JESD60A	A Procedure For Measuring P-Channel Mosfet Hot-Carrier-Induced Degradation At Maximum Gate Current Under Dc Stress, September 2004
JESD61A.01	Isothermal Electromigration Test Procedure, October 2007
JESD63	Standard Method for Calculating the Electromigration Model Parameters for Current Density and Temperature, February 1998
JESD78A	IC Latch-Up Test, February 2006
JESD87	Standard Test Structures for Reliability Assessment of AlCu Metallizations with Barrier Materials, July 2001
JESD88	Dictionary of Terms for Solid State Technology
JESD89-1A	Test Method For Real-Time Soft Error Rate, October 2007
JESD89-2A	Test Method For Alpha Source Accelerated Soft Error Rate (SER), October 2007
JESD89-3A	Test Method for Beam Accelerated Soft Error Rate, November 2007
JESD89A	Measurement And Reporting Of Alpha Particle And Terrestrial Cosmic Ray Induced Soft Errors In Semiconductor Devices, October 2006

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3 Inclusions, deliberate omissions, and resources (cont'd)

3.3 JEDEC resources (cont'd)

JESD90	A Procedure for Measuring P-Channel MOSFET Negative Bias Temperature Instabilities, November 2004
JESD92	Procedure for Characterizing Time-Dependent Dielectric Breakdown of Ultra-Thin Gate Dielectrics, August 2003
JESD201	Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finished, March 2006
JEP119A	A Procedure For Executing Sweat, August 2003
JEP139	Guideline For Constant Temperature Aging To Characterize Aluminum Interconnect Metallizations For Stress-Induced Voiding, December 2000
J-STD-020D.01	Joint IPC/JEDEC Standard For Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface-Mount Devices, March 2008
JP002	Current Tin Whiskers Theory and Mitigation Practices Guideline, March 2006
IPC 610	PCB Inspection Criteria

4 The basic thermal acceleration equation

When estimating acceleration due to temperature, it is customary to use the expression in equation **(2.1)**. It is an adaptation of the Arrhenius equation and has been used to express both a single failure mechanism's sensitivity to temperature (i.e., its acceleration factor) and also a product's thermal acceleration factor. By measuring parametric change caused by temperature, activation energy in its physical sense can be estimated. When used to estimate the reliability of a product, as shown in equation **(4.1)**, it is also being used to express that product's reliability with respect to temperature and as a function of time.

$$\lambda_{Top} = \lambda_{Tst} / A_T = \lambda_{Tst} / \exp[(-E_{aa} / k)(1 / T_{st} - 1 / T_{op})] \quad \textbf{(4.1)}$$

where

λ_{Top} is the observed failure rate at an operating temperature T_{op} (h^{-1})
λ_{Tst} is the observed failure rate at stress temperature T_{st} (h^{-1})
E_{aa} is the apparent activation energy in electronvolts (eV)
k is Boltzmann's constant (8.62×10^{-5} eV/kelvin)
T_{st} is the absolute temperature of the stress in kelvins
T_{op} is the absolute temperature of an operating condition in kelvins

Equation **(4.1)** (same as 2.1) must be used with caution because this relationship holds only for systems in which the failure rate is constant. However, very few practical situations exist in which the failure rate is truly constant. Nevertheless, the assumption of constant failure rate is still commonly used. An "apparent" activation energy, E_{aa}, may be used for product failure rate estimates in the absence of extensive failure analysis based on root cause and responsible failure mechanisms.

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5 Models for common failure mechanisms

The failure mechanisms described in the several sections of this standard constitute commonly accepted industrial models, validated by a team of reliability experts (from the SEMATECH/ISMI Reliability Council) and buttressed by citations to the most cogent published literature.

5.1 FEoL Failure Mechanisms – Time-Dependent Dielectric Breakdown (TDDB) – Gate Oxide

Time-Dependent Dielectric Breakdown (TDDB) is an important failure mechanism in ULSI devices. The dielectric fails when a conductive path forms in the dielectric, shorting the anode and cathode. It should be noted that TDDB for intermetal diectric is discussed in 5.7. It is important to make a distinction between the empirical models and the physical models developed to explain these empirical models. The experimental data can generally be described by one of four models (see citations **[5.1.1 to 5.1.12]** for historically significant papers):

1) E model or constant field/voltage acceleration exponential model
2) 1/E model or, equivalently, anode hole injection model
3) V model, where failure rate is exponential with voltage
4) Anode hydrogen release for the power-law model

The physical models used to explain the four empirical models are: A) thermo-chemical model, B) anode hole injection, C) bulk trap generation, and D) anode hydrogen release model. While the thermo-chemical and V models adopt the assumption of field-driven mechanism, both anode hole injection and anode hydrogen release models assume a current-driven mechanism in addition to the role of applied voltage or oxide fields depending on the specific conditions.

5.1.1 Constraints and limitations

These models are intended for application to SiO_2 gate dielectric over a large range of oxide thicknesses. Models and parametric values to effectively model “high-k” oxides (based on materials or composites other and silica) are unknown so these materials are not yet treated in this document.

Controversies regarding these models still exist, hence users are encouraged to review literature before they make their own decisions for their unique technologies.

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5.1.2 Models

5.1.2.1 E model [5.13 to 5.1.16]

In the E model for gate oxide thickness greater than 4 nm, the cause of low electric field (<10 MV/cm) TDDB is due to field-enhanced thermal bond breakage at the silicon-silica interface. The E-field serves to reduce the activation energy required for thermal bond breakage and therefore exponentially increases the reaction rate for failure. The time-to-failure (TTF), inverse to reaction rate, decreases exponentially with temperature:

$$TTF = A_o * \exp(-\gamma E_{ox}) * \exp(E_{aa} / kT) \quad \textbf{(5.1.1)}$$

where

A_o = arbitrary scale factor, dependent upon materials & process details

γ = field acceleration parameter in cm/MV, is temperature dependent, γ (T) = a / kT where a is the effective dipole moment for the molecule (see also the note at the end of this clause)

E_{ox} = externally applied electric field across the dielectric in MV/cm. E_{ox} is the quotient of the voltage & the oxide thickness, t_{ox}. Note that t_{ox} should be electrically or physically measured.

E_{aa} = apparent activation energy, typically expressed in electronvolts (eV)

k = Boltzmann's constant

T = temperature in kelvins

Previous work **[5.1.20]** at very large electric field shows that γ has a 1 / T dependence, which affects TTF equivalently to an activation energy that decreases linearly with the electric field,

$$E_{aa} = (\Delta H)_o - a\, E_{ox} \quad \textbf{(5.1.2)}$$

where

E_{aa} = apparent activation energy, typically expressed in electronvolts (eV); E_{aa} may be nearly temperature independent if several types of disturbed bonding states are present in the dielectric and the reaction rates are mixed during high field and/or high temperature TDDB testing

$(\Delta H)_o$ = the enthalpy of activation for bond breakage in the absence of external electric field (~2.0 eV in **[5.1.12, 5.1.24, 5.1.25]**)

a = effective molecular dipole-moment for the breaking bonds (~7.2 eÅ in **[5.1.12, 5.1.24, 5.1.25]**)

E_{ox} = externally applied electric field across the dielectric in MV/cm. The value must be voltage compensated for band bending if an accumulation layer is formed, but no compensation is needed if an inversion layer is formed. E_{ox} is the quotient of the compensated voltage & the oxide thickness, t_{ox}. Note that t_{ox} should be electrically or physically measured.

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5.1.2 Models (cont'd)

5.1.2.1 E model [5.13 to 5.1.16] (cont'd)

For intrinsic failures in SiO_2 dielectrics of thickness ~<10 nm, γ = ~2.5 to 3.5 Naperians per MV/cm (~1.1 to 1.5 decades per MV/cm) and E_{aa} = 0.6 to 0.9 eV. For extrinsic defects, effective oxide thickness can be quite thin, and therefore, the effective field can be very large, which may reduce temperature sensitivity.

Long-term TDDB studies **[5.1.17]** showed that TDDB data were described effectively by the E model **[5.1.13 to 5.1.16]** while TDDB data published in **[5.1.18]** followed the 1/E model **[5.1.19 to 5.1.23]**. All models are now based on fundamental, physical parameters (not empirically fitted parameters) and fit TDDB data quite well **[5.1.17, 5.1.24, 5.1.25]**. The key issue is whether any given model can also obey the Poisson area scaling, which is universally accepted.

The good fit of the physics-based E model to the low field/long-term TDDB data strongly suggests electric field is the dominant degradation driver at low stresses characteristic of customer applications and that constant current stress is NOT relevant to customer application.

5.1.2.1.1 TDDB numerical example using E model

Objective: Calculate the acceleration factor (AF) for gate oxide failure by TDDB for an office environment vs. a test structure accelerated environment.

Assumptions:
Office conditions are: 50°C chip temperature (inside a desktop PC) & an electric field of 4 MV/cm
Accelerated condition (for a test structure) is: 300°C & 8 MV/cm
Field acceleration parameter, γ : 3 Naperians (natural logarithm) per MV/cm
Apparent activation energy, E_{aa}: 0.75 eV (approximate center of the nominal range for E_{aa})

AF, the ratio of the time-to-failure (TTF) values will be:

$$\text{AF (ratio of } TTF_{office} \text{ to } TTF_{accel} \text{ values)} = \exp[-\gamma (E_{office} - E_{accel})] * \exp[(E_{aa} / k)(1 / T_{office} - 1 / T_{accel})]$$

$$AF = \exp[-3/(MV/cm)(4\ MV/cm - 8\ MV/cm)] * \exp[(0.75\ eV / 8.62 \times 10^{-5}\ eV/K)(1 / (273 + 50)K - 1 / (273 + 300)K)]$$

$$AF = 1.6 \times 10^{5} * 1.27 \times 10^{5} = 2 \times 10^{10}$$

Conclusion: So, moving from the accelerated test structure environment to the office environment will increase TTF value to 2×10^{10} times the accelerated stress value, of which 160,000 X is due to electric field and 127,000 X is due to temperature. One must consider whether the same failure mechanisms are active under such a heavily accelerated stress vs ordinary operation.

NOTE Many papers in the literature may use and plot base 10 (rather than base e) when expressing the field acceleration factor. One should be careful to note whether base 10 or natural base e is being used. Some authors, for clarity reasons, will write the field acceleration as decades per MV/cm to emphasize that the base 10 is being used or Naperians per MV/cm to emphasize that the natural base e is being used. Many authors, however, may not emphasize this distinction to the reader, so the reader must be cautious. The conversion factor between base 10 and base e is 2.3:1, i.e., $\gamma_{base\ e} = 2.3 * \gamma_{base\ 10}$. In this document, the natural base e is assumed.

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5.1.2 Models (cont'd)

5.1.2.2 1/E model [5.1.19 to 5.1.23]

The cause of TDDB (even at low fields) is postulated to be due to current through the dielectric by Fowler-Nordheim (F-N) conduction. F-N injected electrons (from the cathode) cause impact ionization damage of the dielectric due to as they accelerate through the dielectric. Additionally, when these accelerated electrons reach the anode, hot holes may be produced that can tunnel back into the dielectric causing damage (hot-hole anode injection mechanism). The time-to-failure is expected to show an exponential dependence on the inverse of electric field, $1 / E_{ox}$:

$$TTF = \tau_o(T) * \exp(G(T) / E_{ox}) \quad \textbf{(5.1.3)}$$

where

$\tau_o(T)$ = temperature dependent pre-factor (~1×10^{-11} s)
$G(T)$ = field acceleration parameter (~350 MV/cm with a weak temperature dependence)
E_{ox} = externally applied electric field across the dielectric in MV/cm. It must be voltage compensated for band bending if an accumulation layer is formed, but no compensation is needed if an inversion layer is formed. E_{ox} is the quotient of the compensated voltage & the oxide thickness, t_{ox}. Note that t_{ox} should be electrically or physically measured.

5.1.2.3 V model [5.1.26 to 5.1.27]

Two papers at 2000 IRPS reported data that showed the E model was no longer valid for gate oxide thickness values <4 nm. It was found that a model exponential with voltage rather than electric field represented the reliability performance well. Thus, the time-to-failure is expressed as:

$$TTF = A_o * \exp(-\beta V) * \exp(E_{aa} / kT) \quad \textbf{(5.1.4)}$$

where

A_o = arbitrary scale factor, dependent upon materials & process details
β = voltage acceleration parameter
V = applied voltage
E_{aa} = apparent activation energy, typically expressed in electronvolts (eV)
k = Boltzmann's constant
T = temperature in kelvins

5.1.2.4 Power-law model [5.1.28 to 5.1.37]

In recent years for gate oxide thickness <2 nm, a power-law for voltage dependence of oxide breakdown is proposed based on extensive experimental database including long-term module stress **[5.1.28]**. Several research groups independently experimentally confirmed this model **[5.1.29 to 5.1.34]**. Work reported at 2006 IRPS demonstrates the power-law voltage dependence remains valid over twelve orders of magnitude from micro second time frames to hundred hours time span **[5.1.32]**.

The power-law model was originally proposed based on the experimental work on ultra-thin oxides below 5 nm **[5.1.28]**. Most importantly, the power-law model preserves important breakdown characteristics, namely Poisson random statistics and weakest link property, which are universally accepted **[5.1.28]**. This model can be extended to describe a large range of oxide thickness up to 10 nm and at stress voltages as large as 12 V **[5.1.35]**. This model is also consistent with the current-driven breakdown property as demonstrated by independent experimental evidence using substrate carrier injection technique **[5.1.36]**. The physical interpretation of power-law voltage dependence has also been advanced by several groups by comparing experimental data with the first-principle theory and STM experiments of hydrogen desorption phenomenon **[5.1.29, 5.1.30, 5.1.35 to 5.1.37]**.

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5.1.2 Models (cont'd)

5.1.2.4 Power-law model [5.1.28 to 5.1.37] (cont'd)

The time-to-breakdown is expressed as:

$$t_{BD} = t_o * V^{-n} \quad \textbf{(5.1.5)}$$

where n is the power-law exponent and t_o is the prefactor.

The exponent of power-law, n, is found to be independent of oxide thickness or only weakly dependent of oxide thickness. On the other hand, temperature dependence of oxide breakdown is generally complicated by many factors **[5.1.29]**. First of all, the power-law exponent is found to depend on temperature. The physics of this temperature dependence of power-law exponent are not clear at this moment **[5.1.34]**. Secondly, temperature dependence of oxide breakdown is shown to follow a non-Arrhenius activation rather than conventionally accepted Arrhenius activation. This suggests that activation energy is temperature dependent **[5.1.14]**, analogous to the voltage dependence of local voltage acceleration factor. Both the temperature dependent exponent and non-Arrhenius activation give rise to a large variety of experimental observations commonly found on ultra-thin oxides and also provide a link to the experimental findings in thick oxides. In practice, for limited range of temperature applications, an Arrhenius temperature activation can be used as an approximate solution for the time-to-breakdown:

$$t_{BD} = t_o * \exp(E_{aa} / kT) \quad \textbf{(5.1.6)}$$

where

t_o = reference time at some reference temperature
E_{aa} = apparent activation energy, typically expressed in electronvolts (eV)
k = Boltzmann's constant
T = temperature in kelvins

For a detailed and more complete discussion of power-law model for voltage and temperature dependence of oxide breakdown, the readers are referred to the reference **[5.1.31]**. Earlier relevant work is shown in citations **[5.1.1 to 5.1.12]**.

5.1.3 Example of Time-Dependent Dielectric Breakdown – gate oxide

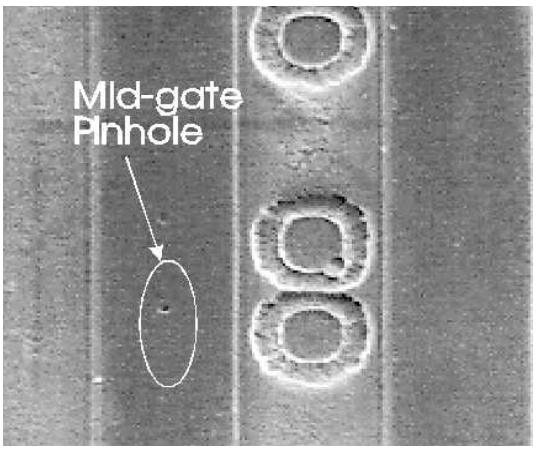


Figure 5.1.1 — Photograph of TDDB failure in a gate oxide — mid-gate

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5.2 FEoL Failure Mechanisms – Hot Carrier Injection (HCI)

Hot carrier injection describes the phenomenon by which carriers gain sufficient energy to be injected into the gate oxide **[5.2.6 to 5.2.15]**. This occurs as carriers move along the channel in MOSFET and experience impact ionization near the drain end of the device. The damage can occur at the interface, within the oxide and/or within the sidewall spacer. Interface-state generation and charge trapping induced by this mechanism result in transistor parameter degradation, typically switching frequency degradation, rather than a "hard' functional failure.

5.2.1 Constraints and limitations

HCI-induced transistor degradation is well modeled by peak substrate current for the n-channels and peak gate current for the p-channels, at least for transistors at >0.25 μm. For sub-0.25 μm p-channel, the drive current tends to decrease like NMOS after hot carrier stress. For sub-0.25 μm p-channel, worst-case lifetime occurs at maximum substrate current stress. The time-to-failure (TTF) model is the same as n-channel. The drive currents for the n-channel transistors tend to decrease after HCI stressing; the p-channel drive current may increase/decrease depending on channel length and stress conditions. The off-state leakage can increase dramatically **[5.2.12]**, especially for initially high drive current p-channels.

There have been reports that the temperature dependence of substrate current has positive activation energy when V_{CC} is lower than 2.5 V **[5.2.1 to 5.2.3]**. The temperature dependent model for lower V_{CC} is still under investigation. A new energy driven paradigm is proposed for NMOSFET hot carrier effects. The driving force is the energy (voltage) instead of the electric field (lucky electron model) **[5.2.4]**. A gate-drain/source overlap asymmetry can result in worse hot carrier reliability **[5.2.5]**.

There is growing evidence that HCI physics may be starting to change at 0.25 μm and smaller, leading to changes in worst-case stress conditions **[5.2.4]**. Precise voltage models (rather than substrate current or gate current) would be very useful.

HCI evaluations are almost always performed on test structures rather than products and done under DC conditions, thus the calculated lifetime should be considered a figure of merit for process comparison. A short "lifetime" observed with DC test structures does NOT imply unacceptable product performance under AC conditions. For a digital circuit, like an inverter, HCI stress only occurs during the device turn-on and turn-off periods. These turn-on and turn-off periods are typically 1-2% of the overall cycle time. Hence, the conversion factor between DC stress and AC stress can be large. Note that this section treats device HCI when the transistor is conducting, but does not treat other effects when the device is not conducting (NBTI, PBTI, Drain-Gate stress, etc., which can have large duty cycle and different failure mechanisms).

Typically, HCI degradation causes reduced circuit speed rather than catastrophic failure; although, a large enough speed reduction can cause device failure. For products where the substrate or gate current is unknown, large voltage acceleration is possible because gate and substrate current are exponentially related to the reciprocal of the gate oxide electric field. HCI-induced transistor degradation modeling seems to be accurate, but the extrapolation from transistor degradation to circuit-level degradation is uncertain and should be the focus of future research efforts.

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5.2 FEoL Failure Mechanisms – Hot Carrier Injection (HCI) (cont'd)

5.2.2 Models

Generally, degradation induced by the HCI can be described by:

$$\Delta p = A * t^n \quad \textbf{(5.2.1)}$$

where

Δp = shift in device parameter of interest (V_T, g_m, I_{Dsat}, etc.)
A = material dependent parameter
t = stress time
n = empirically determined exponent, a function of stress voltage, temperature, and effective transistor channel length

5.2.2.1 N-channel model

N-channel devices use an Eyring model. Eyring makes the practical assumption of mathematically separable, independent variables:

$$TTF = B * (I_{sub})^{-N} * \exp(E_{aa} / kT) \quad \textbf{(5.2.2)}$$

where

B = arbitrary scale factor (strong function of proprietary factors such as doping profiles, sidewall spacing dimensions, etc.)
I_{sub} = peak substrate current during stressing
N = 2 to 4
E_{aa} = apparent activation energy, -0.2 to +0.4 eV
k = Boltzmann's constant
T = temperature in kelvins

NOTE: The apparent activation energy can be negative or positive depending on channel length and voltage **[5.2.1 to 5.2.3]**.

5.2.2.2 P-channel model

5.2.2.2.1 For L >= 0.25 μm

$$TTF = B * (I_g)^{-M} * \exp(E_{aa} / kT) \quad \textbf{(5.2.3)}$$

where

B = arbitrary scale factor (strong function of proprietary factors, such as doping profiles, sidewall spacing dimensions, etc.)
I_G = peak gate current during stressing
M = 2 to 4
E_{aa} = apparent activation energy, -0.1 to -0.2 eV
k = Boltzmann's constant
T = temperature in kelvins

NOTE A rough "rule-of-thumb" for the gate current versus voltage dependence of p-channel devices is peak gate current doubles for each 0.5 V increase in drain-source voltage (V_{DS}).

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5.2.2 Models (cont'd)

5.2.2.2 P-channel model (cont'd)

5.2.2.2.2 For L <0.25 μm

$$TTF = B * (I_{sub})^{-N} * \exp(E_{aa} / kT) \quad \textbf{(5.2.4)}$$

where

B = arbitrary scale factor (strong function of proprietary factors such as doping profiles, sidewall spacing dimensions, etc.)
I_{sub} = substrate current during stressing at $V_G = V_D$
N = 2 to 4
E_{aa} = apparent activation energy, +0.1 to +0.4 eV
k = Boltzmann's constant
T = temperature in kelvins

5.2.3 HCI numerical example

Objective: Calculate the acceleration factor (AF) for Hot Carrier Injection for an office environment vs. a test structure accelerated environment.

Assumptions:
Office conditions are: 50°C chip temperature & substrate current of 1 μA
Accelerated conditions are: -40°C & 10 μA substrate current
Substrate current is accelerated by elevating V_{CC}
N value of 3
Apparent activation energy, E_{aa}: -0.15 eV

AF, the ratio of the time-to-failure (TTF) values will be:

$$AF \text{ (ratio of } TTF_{office} \text{ to } TTF_{accel} \text{ values)} = [(I_{sub,\,office} / I_{sub,\,accel})^{-N}] * \exp[(E_{aa} / k)(1 / T_{office} - 1 / T_{accel})]$$

$$AF = [(1\ \mu A / 10\ \mu A)^{-3}] * \exp[(-0.15\ eV / 8.62 \times 10^{-5}\ eV/K)(1 / (273 + 50)K - 1 / (273 - 40)K)]$$

$$AF = 1 \times 10^{3} * 8 = 8000$$

Conclusion: So, moving from the accelerated test structure environment to the office environment will increase TTF value to 8000 times the accelerated stress value, of which 1000 X is due to substrate current and 8-fold is due to temperature.

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5.3 FEoL Failure Mechanisms – Negative Bias Temperature Instability (NBTI)

Negative Bias Temperature Instability (NBTI) is a wearout mechanism experienced by PMOSFETs with the channel in inversion **[5.3.1 to 5.3.18]**. It is believed that NBTI is controlled by an electrochemical reaction where holes in the PMOSFET inverted channel interact with Si compounds (Si-H, Si-O, etc) at the Si/SiO_2 interface to produce donor type interface states and possibly positive fixed charge. NBTI damage is generated by cold holes (thermalized) in the inverted channel. Attention must be paid not to confuse this mechanism with PMOSFET damage generated by possible impact ionization at high V_G regime which produces hot hole damage. The relative contribution of the NBTI induced interface states generation and positive fixed charge formation is very sensitive to the gate oxide process used in the technology. The electrochemical reaction is strongly dependent on the gate oxide electric field (V_G / t_{ox}) and the channel temperature. The NBTI damage may lead to substantial PMOSFET parameter changes, in particular to an increase of the absolute value of the threshold voltage (transistor is harder to turn on) as well as mobility degradation with consequent reduction in drive current.

5.3.1 Constraints and limitations

NBTI is a limiting factor in scaling CMOS submicron technologies for the following main two reasons:

- NBTI has a strong dependence on the gate oxide process. Nitrided oxides are more sensitive to NBTI than thermal oxides. Nitrided oxides are needed in thinning the gate oxide to reduce Boron penetration.
- The vertical gate oxide electric field is observed to increase with CMOS scaling.

Recent work has shown relaxation effects after stopping the NBTI stress, resulting into a recovery of the NBTI damage which has two important effects:

- Typical testing of device parameters after the NBTI stress is somewhat sensitive to the NBTI recovery. The measured parameter shift strongly depends on the testing sequence and tester used
- Because of the fast recovery effects, it is expected that AC-level NBTI is less than what is measured in DC at the same voltage and temperature stress bias conditions. A general relation between DC and AC NBTI is not established yet. It is expected to be frequency independent, but duty cycle dependent

NBTI stresses are typically performed on test structures rather than products and under DC bias conditions. The estimated DC lifetime should be considered a figure of merit for a process or technology comparison. A short DC NBTI “lifetime” does not imply unacceptable product performance under AC conditions.

GIDL leakage (Gate-Induced-Drain-Leakage) can increase due to NBTI (especially as nitrided oxides are more sensitive to NBTI than pure Si oxides) as consequence of hole damage in the gate-drain overlap region, while the channel off current is reduced. Typically, NBTI degradation causes reduced circuit speed rather than catastrophic failure; although, clearly a large enough speed reduction can cause circuit failure. Circuits allowing large voltage overshoots may be more sensitive to NBTI given the large gate voltage acceleration of this mechanism.

A given PMOSFET in a circuit is exposed to the NBTI damage as long as it operates in inversion. For this reason NBTI is sensitive to stand-by conditions (‘0’ input on an inverter for example), contrary to Channel Hot Carrier, which is typically active during voltage transients.

Larger NBTI induced V_T mismatching is expected in small area PMOSFET transistors – this is particularly true for SRAM. This is the result of the larger broadening of device parameters observed after NBTI with PMOSFET area scaling.

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5.3 FEoL Failure Mechanisms – Negative Bias Temperature Instability (NBTI) (cont'd)

5.3.1 Constraints and limitations (cont'd)

NBTI can be enhanced by BEoL charging. Circuit and device design need to be optimized to minimize this effect.

5.3.2 Models

The current state of the NBTI models is limited by the knowledge of the physics for this mechanism. For a given gate oxide thickness (t_{ox}), either one of the following phenomenological models is generally used to describe the NBTI degradation:

$$\Delta p = A_o * \exp(E_{aa} / kT) * (V_G)^{\alpha} * t^n \quad \textbf{(5.3.1)}$$

or

$$\Delta p = A_o * \exp(E_{aa} / kT) * \exp(\beta V_G) * t^n \quad \textbf{(5.3.2)}$$

where

- Δp = shift in device parameter of interest (V_T, $\%g_m$, $\%I_{Dsat}$, etc.)
- A_o = pre-factor dependent on the gate oxide process and CMOS technology
- E_{aa} = apparent activation energy (experimentally measured values range between -0.01 to +0.15 eV)
- k = Boltzmann's constant
- T = channel temperature in kelvins
- V_G = absolute value of the gate voltage applied to the PMOSFET device in inversion
- α = measured gate voltage exponent (measured values range between 3 to 4)
- β = measured gate voltage sensitivity, units are reciprocal of Voltage
- t = stress time
- n = measured time exponent (measured values range between 0.15 to 0.25)

Assuming **(5.3.1)** is applicable, the following time-to-failure (TTF), for a given accepted Δp failure criterion (Δp_t), is:

$$TTF = [\Delta p_t / A_o * \exp(E_{aa} / kT_{appl}) * (V_{G,\,appl})^{\alpha}]^{1/n} \quad \textbf{(5.3.3)}$$

where

- A_o = pre-factor dependent on the gate oxide process and CMOS technology
- E_{aa} = apparent activation energy, typically expressed in electronvolts (eV)
- k = Boltzmann's constant
- T_{appl} = application channel temperature in kelvins
- $V_{G,\,appl}$ = application gate voltage
- α = measured gate voltage exponent
- n = measured time exponent

In the case where **(5.3.2)** is applicable, TTF becomes:

$$TTF = [\Delta p_t / A_o * \exp(E_{aa} / kT_{appl}) * \exp(\alpha V_{G,\,appl})]^{1/n} \quad \textbf{(5.3.4)}$$

where symbols in equation **(5.3.4)** have the same meanings as in **(5.3.3)**.

The failure criterion Δp_t is defined in terms of an allowed PMOSFET parameter shift such as ΔV_T or $\%I_{Dsat}$. Typically, the selection of a given failure criterion should depend on the circuit sensitivities and requirements of the PMOSFET device under investigation.

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5.3 FEoL Failure Mechanisms – Negative Bias Temperature Instability (NBTI) (cont'd)

5.3.3 NBTI numerical example

Objective: Calculate the acceleration factor (AF) defined as the ratio between TTF for application conditions (TTF_{appl}) over TTF for accelerated conditions (TTF_{accel}), i.e., AF = TTF_{appl} / TTF_{accel}

Assumptions:
The application temperature and bias conditions are: 50°C chip temperature & V_G = -1.0 V
The accelerated temperature and bias conditions are: 140°C & V_G = -1.5 V
α value of 3.5
n value of 0.25
Apparent activation energy, E_{aa}: -0.02 eV

Using **(5.3.3)** we have:

$$AF = [(V_{G,\,accel} / V_{G,\,appl})^{\alpha / n}] * \exp[(E_{aa} / k)(1 / T_{accel} - 1 / T_{appl})(1 / n)]$$

$$AF = [(1.5\ V / 1\ V)^{3.5 / 0.25}] * \exp[(-0.02\ eV / 8.62 \times 10^{-5}\ eV/K)(1 / (273 + 140)K - 1 / (273 + 50)K)(1 / 0.25)]$$

$$AF = 292 * 1.87 = 546$$

Conclusion: So, moving from the accelerated stress conditions to the application conditions will increase TTF value to 546 times the accelerated stress value.

5.4 FEoL Failure Mechanisms – Surface inversion (mobile ions)

Alkaline-metal elements such as Li, Na, and K can sometimes be found in the semiconductor processing materials. In SiO_2, these ions are very mobile under the presence of modest electric fields (~0.5 MV/cm) and temperatures (100 °C). An accumulation of the drifted ions at the Si/SiO_2 interface can cause surface inversion and lead to increased leakage and device failure **[5.4.1 to 5.4.5]**.

Sodium and potassium are the usual mobile ion suspects, simply because of their high mobility and their relative abundance in many materials. Under bias, they can drift from the polysilicon anode to the silicon substrate (cathode). A build-up of positive ions at the Si/SiO_2 interface can invert the surface and severely degrade the oxide isolation. Ionic drift in the SiO_2 gate dielectric can also cause premature TDDB. In the case of EPROMs, mobile ion accumulation around the negatively-charged polysilicon floating-gate can lead to data retention fails.

Devices showing such inversion-induced leakage failures can recover during an unbiased high temperature bake. The bake causes a redistribution of the mobile ions away from the accumulated Si/SiO_2 interface (or polysilicon floating-gate in the case of an EPROM-like device).

5.4.1 Constraints and limitations

The activation energy for mobile ion diffusion depends on several factors:

- Diffusing species
- Medium through which the mobile ions diffuse
- The concentration of the contaminant

Generally, one finds activation energies for mobile ion diffusion in SiO_2 (and along its interfaces) in the 0.75 to 1.8 eV range **[5.4.1 to 5.4.7]**. Citation **[5.4.5]** calculates activation energy values from fundamental physical parameters for 25 different species (charge zero, +1 or +2) and is deemed the most reliable source, especially as its values are largely corroborated by later research.

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5.4 FEoL Failure Mechanisms – Surface inversion (mobile ions) (cont'd)

5.4.2 Models

Mobile ions are influenced by both electric field and temperature. An Eyring model for time-to-failure can be written:

$$TTF = A * (< J_{ion} >)^{-1} * exp(E_{aa} / kT) \quad \textbf{(5.4.1)}$$

where

A	=	material dependent constant
$< J_{ion} >$	=	$< (e E \rho D_o / kT) – (D_o \partial\rho(x,t) / \partial x) >$ is the time-averaged mobile ion flux
E_{aa}	=	apparent activation energy for mobile ion diffusion (0.75 to 1.8 eV)
k	=	Boltzmann's constant
T	=	temperature in kelvins

The time-averaged mobile ion flux $< J_{ion} >$ has two components:

1. $(e E \rho D_o / kT)$ is the drift component which causes surface inversion during device operation, where:
   - e is the electronic charge on the mobile ion
   - E is the electric field across gate dielectric
   - ρ is the mobile ion density
   - D_o is the diffusion coefficient
2. $(D_o \partial\rho(x,t) / \partial x)$ is the back diffusion component (or recovery component).

For drift dominated failure (i.e., recovery component is small), the time-to-failure equation **(5.4.1)** reduces to:

$$TTF = A * (kT / e E \rho D_o) * exp(E_{aa} / kT) \quad \textbf{(5.4.2)}$$

5.4.3 Mobile ion numerical example

Objective: Calculate the acceleration factor (AF) for surface inversion between a use environment and an accelerated stress environment.

Assumptions:
The use temperature and bias conditions are: 50 °C chip temperature & V_G = 3.3 V
The accelerated stress temperature and bias conditions are: 150 °C & V_G = 5.0 V
Apparent activation energy, E_{aa}: 0.75 eV (Na+ drift dominated failure)

Using equation **(5.4.2)**, the acceleration factor (AF) becomes:

$$\text{AF (ratio of } TTF_{use} \text{ to } TTF_{accel} \text{ values)} = (T_{use} / T_{accel})(V_{G,\,accel} / V_{G,\,use}) * \exp[(E_{aa} / k)(1 / T_{use} – 1 / T_{accel})]$$

$$AF = ((273 + 50)K / (273 + 150)K)(5.0\ V / 3.3\ V) * \exp[(0.75\ eV / 8.62 \times 10^{-5}\ eV/K)(1 / (273 + 50)K – 1 / (273 + 150)K)]$$

$$AF = [0.7636 * 1.515\ ]* 583.0 = \sim 675$$

Conclusion: The acceleration factor (from accelerated stress environment to the use environment) is ~675. Of this total acceleration factor, ~1.16 X is due to mobile ion flux while ~583 X is due to temperature.

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5.5 FEoL Failure Mechanisms -- Floating-Gate Nonvolatile Memory Data Retention

Nonvolatile memories are subject to several mechanisms that can cause data to be lost. For floating-gate memories, a cell's data ('0' or '1') depends on whether its threshold voltage (V_T) is above or below a critical threshold level ($V_{T,crit}$). The threshold voltage may shift over time, leading to a change in data. The most common mechanisms for threshold drift are dielectric charge leakage and dielectric charge detrapping.

5.5.1 Constraints and limitations

These models apply to silicon floating-gate memories which are erased via tunneling through a 7 to 12 nm thick oxide or nitrided oxide. It is assumed that cell V_T is linear with stored charge, which is true for most common floating-gate memories. Devices such as split-gate memories with nonlinear responses require corrections to the equation terms which contain V_T. The models apply to the best-studied intrinsic data retention mechanisms but do not necessarily apply to other mechanisms.

5.5.2 Models

5.5.2.1 SILC-related dielectric leakage induced by program/erase cycling

High-field stressing of SiO_2 causes low field current leakage, called Stress-Induced Leakage Current or SILC. SILC is attributed to trap-assisted tunneling, whereby electrons or holes tunnel from one electrode to the other through traps generated by the stress. In memories, program/erase cycling causes the trap generation, and the resulting SILC causes V_T to drift. Programmed Flash cells may lose electrons (charge loss) and erased Flash cells may gain electrons (charge gain). The time-to-failure depends on cycle count, temperature, applied voltage, and the threshold voltage at which failure occurs **[5.5.1]:**

$$TF = A_o * (cycles^{-n}) * \exp[E_{aa}/kT] * \exp[-\gamma*(V_{T,Crit} - V_G)] \quad (\textbf{5.5.1})$$

$$TF = A_o * (cycles^{-n}) * \exp[E_{aa}/kT] * \exp[-\gamma*(V_G - V_{T,Crit})] \quad (\textbf{5.5.2})$$

where equations **(5.5.1)** and **(5.5.2)** refer to charge-loss and charge-gain SILC, respectively, and where:

A_o	=	arbitrary scale factor, dependent upon materials & process details
cycles	=	number of program/erase cycles prior to the retention period
n	=	cycling power-law coefficient (typically 0.4 to 0.7)
E_{aa}	=	apparent activation energy (typically zero to 0.3 eV)
k	=	Boltzmann's constant
γ	=	field-acceleration coefficient, referenced to the V_T differential that creates the field in the oxide. Typically 2 to 6 V^{-1}.
$V_{T,crit}$	=	cell threshold voltage at which the cell will be sensed as having incorrect data
V_G	=	applied voltage on the top or control gate of the cell during the retention stress. Zero for an unbiased stress (retention bake).

Temperature acceleration is usually avoided in SILC characterization, because E_{aa} is low and because high temperatures can cause the oxide to recover. Instead, electric-field acceleration is often used, using either margin testing (whereby devices are tested with a guardbanded value of $V_{T,crit}$) or an applied gate voltage (V_G).

The model formulae have been shown to accurately fit results taken over multiple years of retention time for some technologies. However, for other technologies there have been reports of deviations from a pure power-law dependence on cycle count and a pure exponential dependence on voltage **[5.5.2, 5.5.3].** In addition, it has been observed in some devices that threshold drift can abruptly stop when a certain threshold voltage is reached [**5.5.4**]. These effects are not comprehended by the model described above.

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5.5.2 Models (cont'd)

5.5.2.1 SILC-related dielectric leakage induced by program/erase cycling (cont'd)

NOTE For given $V_{T,Crit}$ and V_G, the fraction of bits that are in error, called the bit error rate (BER), depends on the cycle count and the retention time. For BER<<1,

$$BER = BER_0 + B_o * (cycles^n * t)^m \quad (\textbf{5.5.3})$$

where

BER_0 = BER at the beginning of the retention period, due to effects other than SILC
B_o = arbitrary scale factor, dependent upon materials and process details
t = retention time
m = retention-time power law coefficient, typically 1 to 2
n = power law exponent on number of program/erase cycles

In Flash memories designed to be used with error correction codes (ECC), the SILC-related leakage may cause some memory bits to fail even in an unaccelerated retention stress, though data loss does not occur since the BER does not reach the threshold at which the ECC capability is exceeded. In that case, an alternative method may be used: the BER may be measured as a function of time, fit to equation **(5.5.3)**, extrapolated to times beyond the stress time, and then compared to the ECC capability. The ECC capability can be calculated from the details of the ECC method used and the allowable failure rate, using equations that are well known in the field of ECC [5.5.9] but beyond the scope of this document. The capability calculated in this way is accurate only if the bit errors are randomly distributed, which is not perfectly the case in real devices. Accordingly, care must be taken to maintain a safety margin between the calculated ECC capability and the BER; this margin must be chosen to account for the variation of the BER from device to device and from one location of the device to another [5.5.9].

5.5.2.2 Charge detrapping

Generated traps directly affect the V_T of a cell when the traps are directly over the channel, and the V_T will shift if the traps detrap over time. Detrapping can occur under the influence of bias at room temperature or under the influence of elevated temperature. Acceleration results are available for elevated-temperature detrapping [NOR **5.5.5, 5.5.6**, NAND **5.5.7**].

Characterizing detrapping requires two reliability stresses in series – program/erase cycling followed by a data-retention bake. Detrapping in the bake, which can lead to data loss, depends not only on the time and temperature of the bake, but also on the time and temperature of the cycling period, because significant detrapping occurs during the delays between program/erase cycles. As a result, an accelerated reliability stress corresponds not to a single equivalent time under a chosen use condition, but to two such times, one for cycling and one for retention:

$$t_{cycling,use} = t_{cycling,stress} * \exp[(E_{aa}/k) * (1/T_{use} - 1/T_{cycling,stress})] \quad (\textbf{5.5.4})$$

$$t_{retention,use} = t_{retention,stress} * \exp[(E_{aa}/k) * (1/T_{use} - 1/T_{retention,stress})] \quad (\textbf{5.5.5})$$

where:

$t_{cycling,use}$ = time over which cycling occurs at use condition
$t_{cycling,stress}$ = time over which cycling is performed at accelerated stress condition
E_{aa} = apparent activation energy for detrapping (typically 1.1 to 1.2 eV)
k = Boltzmann's constant
T_{use} = temperature in kelvins at use condition
$T_{cyclin,stress}$ = temperature in kelvins during cycling period at accelerated stress condition
$t_{retention,use}$ = time over which retention period occurs at use condition
$t_{retention,stress}$ = time over which retention period is performed at accelerated stress
$T_{retention,stress}$ = temperature in kelvins during retention period at accelerated stress condition

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5.5.3 Data retention numerical example

Objective: Calculate the Acceleration Factors for data retention failure for an office environment vs an accelerated environment for both the detrapping and SILC mechanisms. For detrapping, also calculate the cycling stress conditions necessary to match the office environment after acceleration is considered. For SILC, use the voltage-acceleration method to calculate the acceleration factor. Separately, for SILC calculate the retention time-to-fail using the extrapolated-BER method.

Assumptions:

Use conditions are: 50 °C chip temperature (~T_{use}), with 100,000 cycles over a 2-year period (~$t_{cycling,use}$) followed by a retention period.

SILC accelerated stress conditions are: 100,000 cycles followed by a 25°C retention period. For the voltage-acceleration method, margin testing will be used to guardband the failure level $V_{T,crit}$ by 2V. For the BER-extrapolation method, it will be assumed that the ECC scheme has a BER capability of 4E-5, that a factor-of-two margin of safety is desired based on an analysis of the BER nonuniformity, and that unaccelerated 1000-hour retention results are available with measurement points at 48, 168, 500, and 1000 hours.

Detrapping accelerated stress conditions are: 100,000 cycles performed at 85°C, followed by a retention period at 125°C.

For SILC, γ = 2.3 V^{-1} and E_{aa} = 0 eV; and for detrapping, E_{aa} = 1.1 eV

For detrapping, the required cycling time in the accelerated stress is:

$$t_{cycling,stress} = t_{cycling,use} * \exp[(-E_{aa}/k)*(1/T_{use} - 1/T_{cycling,stress})]$$
$$t_{cycling,stress} = 2 \text{ years} * \exp[(-1.1 \text{ eV} / 8.62\text{x}10^{-5} \text{ eV/K}) * (1/(273 + 50)\text{K} - 1/(273+85)\text{K})]$$
$$t_{cycling,stress} = 2 \text{ years} * 0.0210 = 15 \text{ days}$$

The AF for detrapping in bake is then:

$$AF = t_{retention,use}/t_{retention,stress}$$
$$AF = \exp[(E_{aa}/k)*(1/T_{use} - 1/T_{retention,stress})]$$
$$AF = \exp[(1.1 \text{ eV} / 8.62\text{x}10^{-5} \text{ eV/K}) * (1/(273+50)\text{K} - 1/(273+125)\text{K}] = 1711$$

For SILC using the voltage-acceleration method, the ratio of the TF values will be:

$$AF \text{ (ratio of TF values, office/accelerated)} = \exp[\gamma*(V_{T,crit,accel} - V_{T,crit,office})]$$
$$AF = \exp[(2.3\ V^{-1})*(2\ V)] = 99$$

For SILC using the BER-extrapolation method, the following BER data points will be assumed:

Retention Time (Hours)	BER
0	0
48	5.63E-08
168	2.23E-07
500	7.41E-07
1000	1.59E-06

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5.5.3 Data retention numerical example (cont'd)

These data points would be extrapolated in time as shown below. In this example, the data fit a pure power-law relationship with zero for the BER_0 term. The ECC capability of $4x10^{-5}$ is divided by two to create the specified safety margin, as shown by the horizontal dashed line. The extrapolated BER line intercepts this horizontal dashed line at 10,000 hours, which would be the estimated retention time.

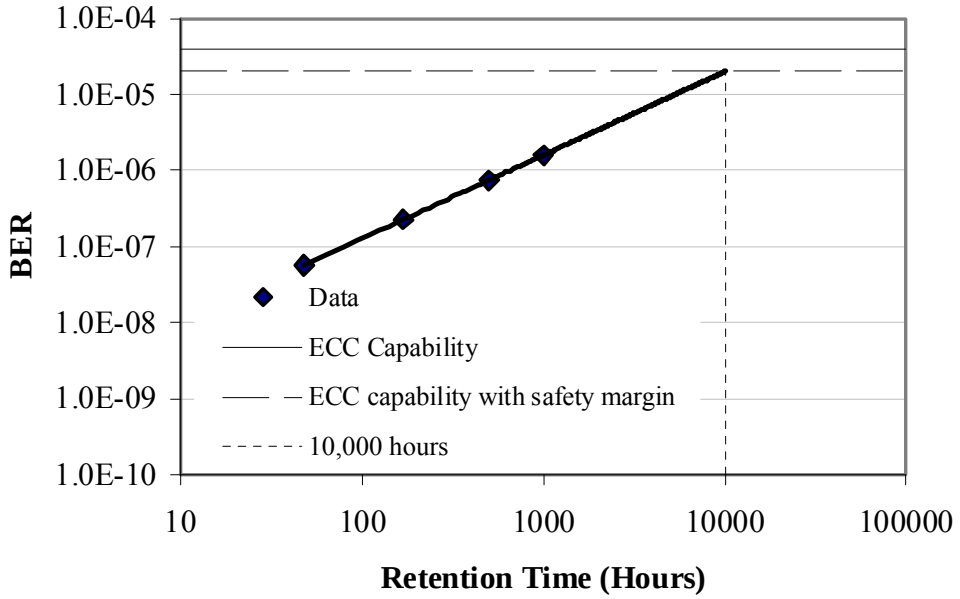


Figure 5.5.1 – Extrapolation of SILC bit error rate

Conclusion: For detrapping, a choice of 15 days at 85 °C for the cycling condition causes the cycling conditions to match the office conditions, and then choosing 125 °C for the retention bake provides an acceleration factor of 1711. For SILC retention, a 2 V margin guardband provides an acceleration factor of 99 compared to the office environment. For SILC retention evaluated with the BER-acceleration method, the example data extrapolate to a TTF of 10,000 hours.

5.6 FEoL Failure Mechanisms – Localized Charge Trapping Nonvolatile Memory Data Retention

In localized charge-trapping NVM devices, such as NROM (Nitride Read Only Memory) devices, the threshold voltage of a cell (V_T) is determined by the quantity and the spatial distribution of the charge trapped locally in an ONO (Oxide-Nitride-Oxide) dielectric layer over the junction edge of an n-channel MOSFET transistor. Charges in NROM cells can be stored locally at both edges of each transistor, thus two physically separated bits can be stored in each cell **[5.6.1]**.

The reliability of data retention of NROM cells depends on the ability of the ONO layer to retain trapped charge. The primary data retention reliability detractor of NROM devices is migration of trapped charges, which may affect the threshold voltage of the cell. Lateral charge migration may occur due to thermally activated charge detrapping. NROM technology with bottom oxide thicker than 4 nm is relatively immune to vertical charge loss. Point defects in the bottom dielectric layer (SILC-type leakage) may cause the loss of only negligible fraction of the stored charge, because only charges trapped directly over the percolation path will be lost **[5.6.2]**.

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5.6 FEoL Failure Mechanisms – Localized Charge Trapping Nonvolatile Memory Data Retention (cont'd)

5.6.1 Constraints and limitations

The model below applies to devices programmed by channel-hot-electron injection and erased by channel-hot-hole assisted tunneling **[5.6.7]**. Charge is injected from the n-channel of the transistor into a nitride layer of an ONO structure through 3 nm to 6 nm thick bottom oxide layer. The charge is stored locally near the junction edges.

The model considers the degradation of an unbiased NVM product as a function of time, temperature and number of endured program/erase cycles **[5.6.3]**. The model applies to cycled cells in which both types of charge carriers had been injected. Injection conditions and microscopic scattering mechanisms are different for holes and electrons, so the spatial distributions of trapped holes and trapped electrons in the dielectric layer are expected to be slightly different, resulting in an internal lateral dipole (multipole) **[5.6.4]**.

The relaxation of a dipole in disordered glasses is controlled by dispersive transport mechanism, resulting in a stretched exponential decay function **[5.6.5]**.

The model describes the decrease of V_T of a programmed cell from its high V_T state. Increase of V_T of the erased state over time (charge-gain) may also degrade the window of operation of NROM cell. The later mechanism and methods to suppress it are discussed elsewhere **[5.6.6]**.

5.6.2 Model

The decrease of V_T of programmed NROM cells is attributed to the migration of holes accumulated during cycling at the junction edges of the device. During long-term storage or under bake conditions at elevated temperatures these holes detrap and migrate laterally toward the electrons trapped further away over the channel, quenching their electric field and reducing the V_T of the cell. Electrons in the nitride are relatively immobile and hardly participate in the charge migration process.

The kinetics of lateral migration of holes in the disordered nitride film follows dispersive transport mechanism **[5.6.2, 5.6.3]**. This mechanism involves multiple trapping and detrapping via a series of events with stochastically increasing release times as the carriers fall from one trap to the next. It leads to a time-dependent diffusion coefficient and a stretched exponential kinetic behavior **[5.6.2]**. The change of V_T with time relative to its initial programmed state, ΔV_T, is described by:

$$\Delta V_T = \Delta V_{Tsat} * \{1 - \exp[-(t / \tau)^{\beta}]\} \quad \textbf{(5.6.1)}$$

$$\tau = \tau_o * \exp(E_\tau / kT) \quad \textbf{(5.6.2)}$$

$$\beta = T / T_o \quad \textbf{(5.6.3)}$$

where ΔV_{Tsat} is the saturation value of the retention degradation, t is storage time, T is storage temperature in kelvins, τ is a time constant, E_τ is a characteristic energy of the dipole relaxation process, k is Boltzmann's constant and τ_o and T_o are empirical coefficients. The parameters ΔV_{Tsat}, τ_o, and E_τ are product, process and cycle-count dependent **[5.6.2, 5.6.3]**. The value of the coefficient T_o was found to be 2550±100K for all NROM products tested to date, irrespective of Fab or technology node.

The Apparent Activation Energy **[5.6.3]** varies with number of cycles according to:

$$E_\tau = 0.75 + 0.07 * \log(\#\ \text{program/erase cycles}); \text{ in units of electronvolts (eV)} \quad \textbf{(5.6.4)}$$

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