

JIS

JAPANESE INDUSTRIAL STANDARD

General rules for transistors

JIS C 7032—1993

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In the event of any doubt arising,
the original Standard in Japanese is to be final authority.

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General rules for transistors

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1. Scope This Japanese Industrial Standard specifies general items of bipolar transistors and field effect transistors, used for electronic appliance (hereafter the both are called as "transistors").

Remarks 1. The following Standards are cited in this Standard:

- JIS C 0301 Graphical symbols for electrical apparatus
 - JIS C 7021 Environmental testing methods and endurance testing methods for discrete semiconductor devices
 - JIS C 7030 Measuring methods for transistors
 - JIS C 7210 General rules for reliability assured discrete semiconductor devices
 - JIS Z 8202 Quantity symbols, unit symbols and chemical symbols
 - JIS Z 8203 SI units and the use of their multiples and of certain other units
2. The International Standards corresponding to this Standard are given below:
- IEC 747-1 (1983) Semiconductor devices, Discrete devices and integrated circuits Part 1 : General
 - IEC 747-7 (1988) Semiconductor discrete devices and integrated circuits Part 7 : Bipolar transistors
 - IEC 747-8 (1984) Semiconductor devices, Discrete devices Part 8 : Field-effect transistors

2. Definitions

2.1 Absolute maximum rating Threshold value of rating which shall not be exceeded even for a moment, and the threshold values which shall not be reached in any two items at the same time, if specified values are determined on 2 or more items.

The voltage and the current related to this parameter mean d.c. or peak values.

2.2 Bipolar transistor The definitions for bipolar transistors are given below.

- (1) storage temperature (T_{stc}) Allowable range of ambient temperature at the time of storage without voltage application.
- (2) junction temperature (T_j) The maximum allowable value of apparent junction temperature in a semiconductor which indicates the correlation of thermal conditions and electric conditions in a bipolar transistor.

- (3) collector-base voltage (V_{CBO}) The maximum allowable value of voltage applicable in the reverse direction of collector junction with the emitter open.
- (4) emitter-base voltage (V_{EBO}) The maximum allowable value of voltage applicable in the reverse direction of emitter junction with the collector open.
- (5) collector-emitter voltage (V_{CEO}) The maximum allowable value of voltage in the reverse direction of collector junction with the base open.
- (6) collector current (I_C) The maximum allowable value of current able to pass continuously in the reverse direction of collector junction when a forward voltage is applied between the emitter and the base.
- (7) emitter current (I_E) The maximum allowable value of current able to pass continuously in the forward direction of emitter junction when the collector and the base are short circuited.
- (8) base current (I_B) The maximum allowable value of current able to pass through base continuously, by applying forward voltage between emitter and base, with the emitter short circuited to the collector.
- (9) total power dissipation (P_{tot}) or collector power dissipation (P_c) The maximum allowable value of total power which can be dissipated, or that of the power which can be dissipated at collector junction, under specified heat radiation conditions.

2.3 Field effect transistor The definitions for field effect transistors are given below.

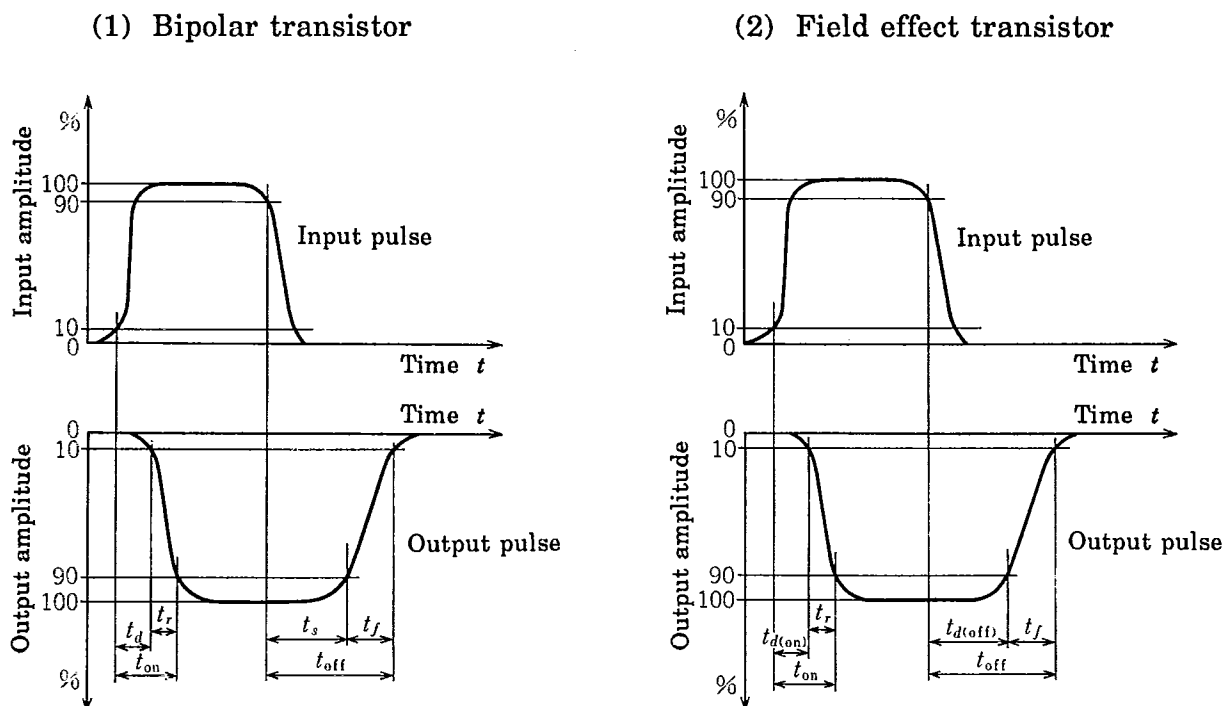
- (1) storage temperature (T_{stg}) Allowable range of ambient temperature at the time of storage without voltage application.
- (2) junction temperature (T_j) The maximum allowable value of apparent junction temperature in a semiconductor which indicates the correlation of thermal conditions and electrical conditions in a field effect transistor.
- (3) channel temperature (T_{ch}) The maximum allowable value of apparent channel temperature in a semiconductor which indicates the correlation of thermal conditions and electrical conditions in a field effect transistor.
- (4) gate-drain voltage (V_{GD}) The maximum allowable value of voltage applicable between the gate and the drain when the source is brought under specified conditions.
- (5) gate-source voltage (V_{GS}) The maximum allowable value of voltage applicable between the gate and the source when the drain is brought under specified conditions.
- (6) drain-source voltage (V_{DS}) The maximum allowable value of voltage applicable between the drain and the source when the gate is brought under specified conditions.
- (7) drain current (I_D) The maximum allowable value of current which can be passed through the drain when the specified voltage is applied between the drain and the source while the specified conditions are maintained between the gate and the source.

- (8) gate current (I_G) The maximum allowable value of current which can be passed through the gate.
- (9) total power dissipation (P_{tot}) or drain-source power dissipation (P_{DS}) The maximum allowable value of total power which can be dissipated, or that of the power which can be dissipated at the drain junction and the channel.

2.4 Pulse response characteristic

2.4.1 Pulse response waveform The pulse response waveform shall be as given in Fig. 1.

Fig. 1. Pulse response waveform



2.4.2 Bipolar transistor The pulse response characteristic of bipolar transistors is defined by the following parameters:

- (1) delay time (t_d) The time interval from the instant when the input pulse reaches to 10 % of its amplitude to the instant when the output pulse reaches to 10 % of its amplitude (see Fig. 1).
- (2) rise time (t_r) The time interval necessary for the output pulse to increase from 10 % to 90 % of its amplitude (see Fig. 1).
- (3) turn-on time (t_{on}) The time interval from the instant when the input pulse reaches to 10 % of its amplitude to the instant when the output pulse reaches to 90 % of its amplitude (see Fig. 1).
- (4) carrier storage time (t_s) The time interval from the instant when the input pulse decreases to 90 % of its amplitude to the instant when the output pulse decreases to 90 % of its amplitude (see Fig. 1).

- (5) fall time (t_f) The time interval necessary for the output pulse to decrease from 90 % to 10 % of its amplitude (see Fig. 1).
- (6) turn-off time (t_{off}) The time interval from the instant when the input pulse decreases to 90 % of its amplitude to the instant when the output pulse reaches to 10 % of its amplitude (see Fig. 1).

2.4.3 Field-effect transistor The pulse response characteristic of field-effect transistors is determined by the following parameters:

- (1) turn-on delay time [$t_{d(on)}$] The time interval from the instant when the input pulse reaches to 10 % of its amplitude to the instant when the output pulse reaches to 10 % of its amplitude (see Fig. 1).
- (2) rise time (t_r) The time interval necessary for the output pulse to increase from 10 % to 90 % of its amplitude (see Fig. 1).
- (3) turn-on time (t_{on}) The time interval from the instant when the input pulse reaches to 10 % of its amplitude to the instant when the output pulse reaches to 90 % of its amplitude (see Fig. 1).
- (4) turn-off delay time [$t_{d(off)}$] The time interval from the instant when the input pulse decreases to 90 % of its amplitude to the instant when the output pulse decreases to 90 % of its amplitude (see Fig. 1).
- (5) fall time (t_f) The time interval necessary for the output pulse to decrease from 90 % to 10 % of its amplitude (see Fig. 1).
- (6) turn-off time (t_{off}) The time interval from the instant when the input pulse decreases to 90 % of its amplitude to the instant when the output pulse reaches to 10 % of its amplitude (see Fig. 1).

3. Detail specification When the rating, performance and external shape of individual transistor are expressed based on this standard, such data shall be specified in the relevant detail specifications.

4. Symbol The graphical symbols used for this standard shall be those given in JIS C 0301.

And the unit symbols shall be those given in JIS Z 8202 and JIS Z 8203.

5. Classification Transistors are classified as given in Table 1.