

JIS

JAPANESE INDUSTRIAL STANDARD

**Graphical Symbols for Binary
Logic Elements**

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In the event of any doubt arising,
the original Standard in Japanese is to be final authority.

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JAPANESE INDUSTRIAL STANDARD

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Graphical Symbols for Binary Logic Elements

X 0122-1986

1. Scope

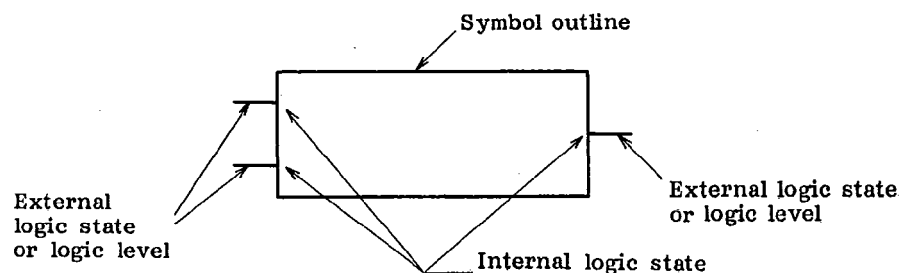
This Japanese Industrial Standard specifies the graphical symbols which denote binary logic functions and their uses.

2. Definitions

For the purposes of this Standard, the following definitions apply.

- (1) binary variable A variable having two different values either of which is adopted.
- (2) binary logic element An element of which input and output represent binary variable and output is specified by the logic function of input (as special cases, time relation, threshold logic function and amplification operation are included). However, the element in this Standard shall represent a unit of logic circuit fulfilling a basic logic function, and shall be denoted normally by a symbol outline (refer to example 1) or connected symbol frames of plural numbers.
- (3) combined logic element A logic element whose output value at an arbitrary time is determined only by the input value at that time.
- (4) sequential logic element A logic element whose input value at an arbitrary time is determined by its input value and the internal state of the element. Its internal state is determined by the input value and the internal state just before that.
- (5) logic state A condition corresponding to the two values of binary variable. The logic state shall be represented by two different symbols, generally the symbols 0 and 1, and called a logic state 0 and logic state 1 or simply state 0 and state 1, respectively.
- (6) internal logic state A logic state of input or output to be obtained within the symbol outline. Unless confusing, it shall be called simply an internal state (refer to example 1).

Example 1:



Applicable Standard:

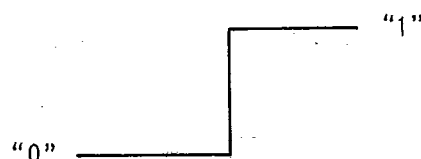
JIS C 0301-Graphic Symbols for Electrical Apparatus

Corresponding International Standard:

IEC Publication 617-12-Graphical symbols for diagrams Part 12:
Binary logic elements

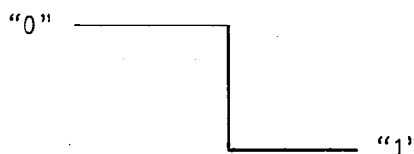
- (7) external logic state A logic state of input or output to be obtained outside the symbol outline. Unless confusing, it shall be called simply an external state (refer to example 1).
- (8) logic level A physical quantity corresponding to two logic states obtained by a binary variable. This is expressed generally with the symbols of H and L. H is used to denote a logic level with a comparatively larger value and L is used to denote a logic level with a comparatively small value.
- (9) positive logic A logic to make the state 1 of binary variable correspond to the logic level of a larger value (H level), and to make the state 0 to that of a smaller value (L level) (refer to Example 2).

Example 2: Positive logic



- (10) negative logic A logic to make the state 1 of binary variable correspond to the logic level of a smaller value (L level), and to make the state 0 to that of a larger value (H level) (refer to Example 3).

Example 3: Negative logic

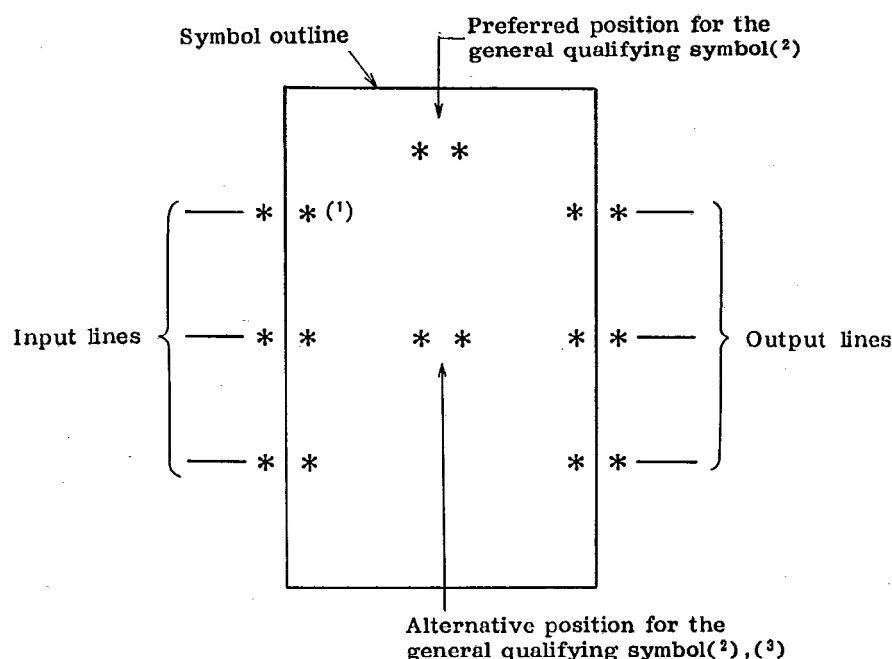


- (11) dependency notation A means of denoting the relationship between inputs and inputs, outputs and outputs, or inputs and outputs, without actually showing any interconnection of circuits composed of plural logic elements in the symbol outline (refer to 5.1.).
- (12) affecting input Input affecting other inputs or outputs following the dependency notations (refer to 5.1.).
- (13) affecting output Output affecting other inputs or outputs following the dependency notations (refer to 5.1.).
- (14) affected input Input affected by the dependency notation (refer to 5.1.).
- (15) affected output Output affected by the dependency notation (refer to 5.1.).

3. Form of Figure Symbols

3.1 Construction of Figure Symbols Figure symbols of binary logic element are constructed as follows (refer to Example 1).

Example 1. Symbol Construction



Notes (1) The single asterisk (*) denotes possible positions for qualifying symbols relating to inputs and outputs.

(2) If and only if the function of an element is completely determined by the qualifying symbols associated with its inputs and/or outputs, no general qualifying symbol is needed.

(3) Preferred position for the general qualifying symbol is at the upper position in the symbol outline, but under certain circumstances its position may be in the center.

(1) **Symbol Outlines** A symbol representing binary logic elements, generally rectangles (refer to 3.3). However, the size of symbols or the ratio of length and breadth may be arbitrary.

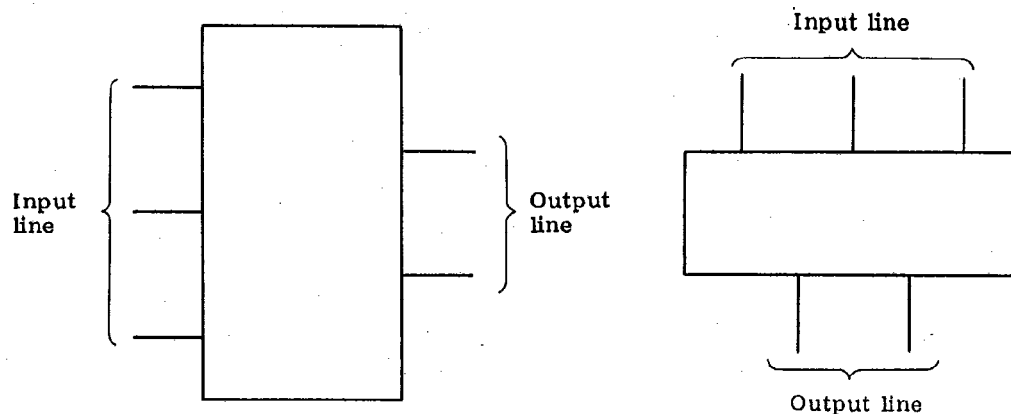
(2) **Qualifying Symbols** A symbol denoting the operating function of binary logic elements and consisting of the following 3 kinds:

- (a) A general qualifying symbol denoting the relation between the logic states of input and output of binary logic elements.
- (b) An input qualifying symbol denoting the relation between the external and internal logic states of input.
- (c) An output qualifying symbol denoting the relation between the internal and external logic states of output.

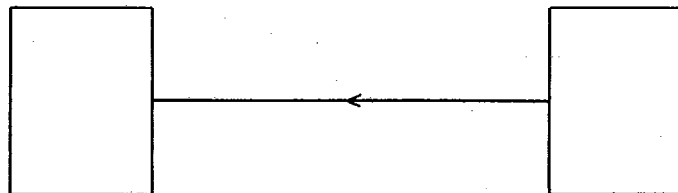
Unless confusing, (b) and (c) are generically called input and output qualifying symbols.

- (3) Input and Output Lines Symbols denoting the input and output of signals, and indicated at both sides of left and right or upper and lower sides of the symbol outlines (refer to example 2). The directions of signal flow on the input and output lines are from left to right or from up to down as a rule. In case the direction of signal flow is uncertain, it shall be shown by arrowheads written on the information transmission lines. However, those arrow marks must not be positioned next to the symbol outlines (refer to Example 3).

Example 2. Input and Output Lines



Example 3. Direction of Signal Flow



- (4) Additional Information Where it is necessary to add additional information, such as types or locations of logic elements, the following rules shall apply.
- To add information not specified by this Standard in relation to specific inputs (outputs), they shall be put in brackets, and the positions are adjacent to the related inputs (outputs) and in back (front) of their input (output) qualifying symbols (refer to symbol number 6-12-7).
 - Additional information related to general logic functions of elements may be indicated in brackets in the symbol outline.

Remark: Although for the sole purpose of distinguishing the input and the output, small letters of alphabet or numerals are conventionally prefixed to the outside of symbol outline, they are not part of the symbols specified in this Standard.

3.2 Logic Agreement In using binary logic, the logic agreements which specify the correspondence between logic states and logic levels shall conform to either of the following.

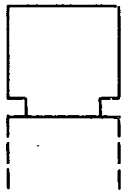
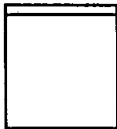
- (1) **Single Logic Agreement** The logic agreement for all inputs and outputs in the logic figure shall be either of positive logic or negative logic. Unless particularly specified, it shall be positive logic.

In the single logic agreement, as occasion demands, the logic negation (refer to symbol numbers 4-1-1 and 4-1-2) may be used, but the logic polarity indicator (refer to symbol numbers 4-1-3 to 4-1-6) shall not used.

- (2) **Logic Polarity Agreement** The input or output which makes the logic level L correspond to state 1 is indicated accompanied by the logic polarity indicator. In case either the input or the output is not marked with the logic polarity indicator, it shall be assumed that the the state 1 is made to correspond to the logic level H. In the logic polarity agreement, the logic negator shall not be used. However, the case of internal connection is omitted (refer to 4.1).

3.3 Basic Notation of Symbol Outlines Basic notation of symbol outlines shall be as given in Table 1.

Table 1. Basic Notation of Symbol Outlines

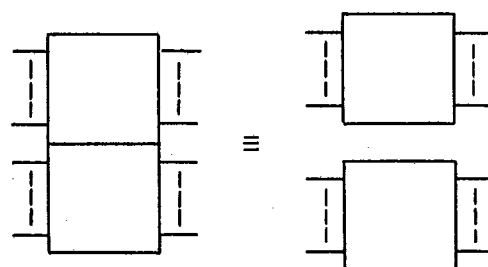
Symbol No.	Symbol	Description · Meaning
3-3-1 (12-05-01)		Element outline (square shown) [refer to 3.1 (1)]
3-3-2 (12-05-02)		Common control block outline [refer to 3.4 (5) to (8)]
3-3-3 (12-05-03)		Common output element outline [refer to 3.4 (9) to (11)]

Remark: Numerals in () in the symbol number column denote the symbol numbers given in IEC 617-12.

3.4 Combination of Symbol Outlines The outlines of the associated element groups may be joined in one sum or embedded inside other symbol outlines. However, in this case, the following rules shall be observed.

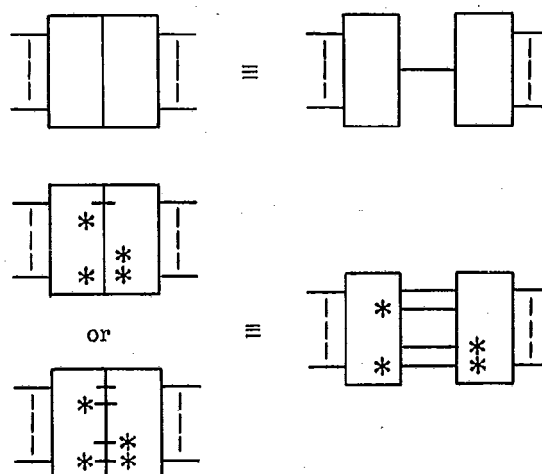
- (1) There is no logic connection between elements when the line common to their outlines is in the direction of signal flow (refer to Example 1). However, this rule does not necessarily apply to those arrays in which there exist two or more directions of signal flow, e.g. symbols, indicated by a common control block or a common output element, and a dependency notation.

Example 1:



- (2) There is at least one logic connection if the line common to two outlines is perpendicular to the direction of signal flow (refer to Example 2).

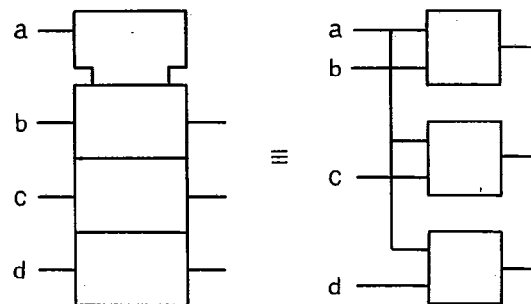
Example 2:



Remark: Each asterisk denotes a position for input and output qualifying symbol.

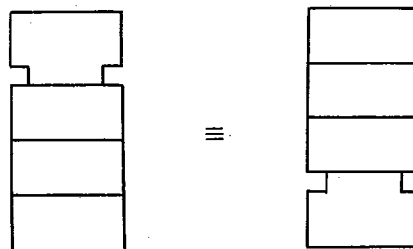
- (3) Each connection can be shown by the presence of qualify symbols at one or both sides of the common line. If confusion can arise about the number of logic connections, use can be made of the internal connection symbol (refer to symbol No. 4-2-1) (refer to Example 2).
- (4) If no indications are shown on either side of the common line, it is assumed that there exists only one logic connection (refer to Example 2).

- (5) In the array of symbol outlines, if the input (output) is common to some or all elements of the array, it is called a common input (output). The common input and output may be indicated in conjunction with the common control block, and as occasion needs, shall be labeled appropriately [refer to 3.4 (11)].
- (6) If an input shown at a common control block is an affecting input in the sense of dependency notation (refer to 5.1), it is connected as an input only to those elements of the array in which its identifying number appears.
- (7) If an input shown at a common control block is not an affecting input in the sense of dependency notation, it is an input common to, or affecting, all elements of the array (refer to Example 3).

Example 3:

- (8) The common control block is placed on one end of an array of related elements (refer to Example 4).

Unless indicated otherwise, the element next to the common control block is assumed to be the lowest order element.

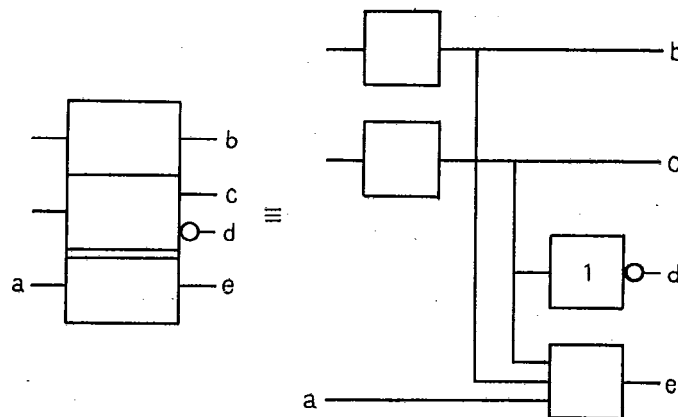
Example 4:

- (9) A common output, depending on all elements of the array, can be shown as the output of a common output element.
- (10) In the case where any array element has more than one output, the common output element may be used only if those outputs always have identical internal logic states. There is one internal connection from each of the elements to the common output element and these shall not be shown. In addition, the common output element may have other inputs and they must be explicitly shown. The function of the common output element shall be indicated (refer to Example 5).

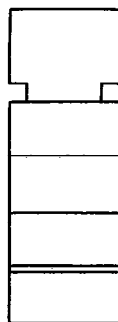
(11) The position of a common output element shall be as follows:

- (a) At the end of the array, or if the common control block exists, in its diametrically opposite position or inside the common control block (refer to Examples 5, 6 and 8).

Example 5:



Example 6:



- (b) Where it is appropriate to show an array of common output elements, the double line need be shown only once. (refer to Example 7).

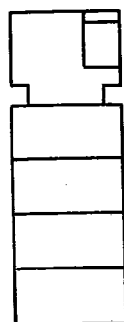
Example 7:



Array with two common output elements

(c) Inside the common control block (refer to Example 8)

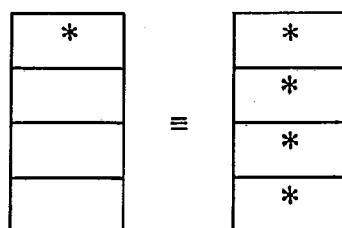
Example 8:



Array with common output element
inside the common control block

- (1) For an array of elements consisting of successive identical elements, it may be sufficient to show the internal qualifying symbol in only the first of the successive elements, provided that no confusion can arise (refer to Examples 9 to 11).

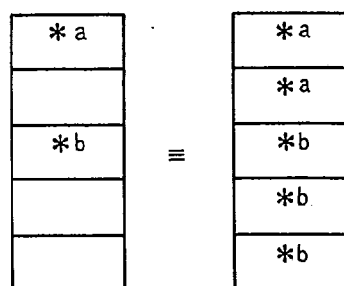
Example 9:



Array with successive identical
elements

Remark: * The mark denotes the internal function.

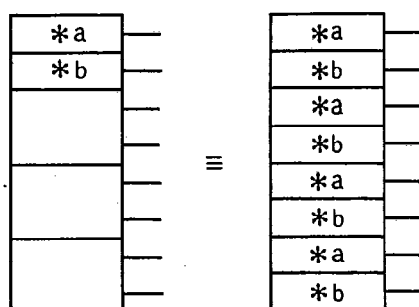
Example 10:



Array of two successive groups of
elements

Remark: *a and *b denote the internal functions.

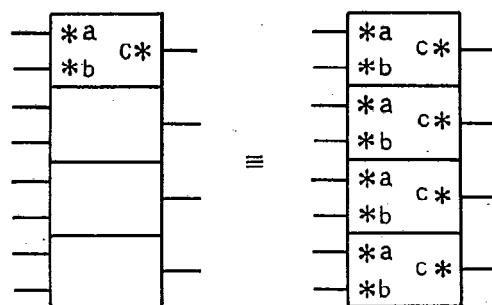
Example 11:



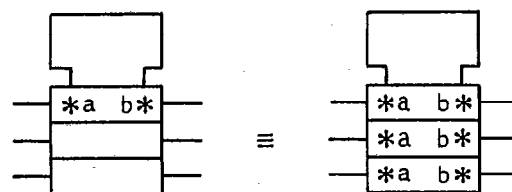
Array of two interlaced groups of
elements

Remark: *a and *b denote the internal
functions.

- (13) In the case that the input and output qualifying symbols appear inside the symbol outlines of array elements, it may be sufficient to show the input and output qualifying symbols in only the first of the element symbol outlines or the element symbol outline next to the common control block, provided that no confusion can arise (refer to Examples 12 and 13). In this case, it is assumed that the identifying numbers of affecting inputs (outputs) and affected inputs (outputs) are different for each array element, respectively. (refer to 5.1).

Example 12:

Remark: *a, *b, and *c indicate the input and output functions.

Example 13:

Remark: *a and *b indicate the input and output functions.

4. Qualifying Symbols Related to Inputs, Outputs and Other Connections

4.1 Negation, Logic Polarity and Dynamic Input Negation, logic polarity and dynamic input are the qualifying symbols representing the relations between internal and external logic states or between internal logic state and external logic level as shown in Table 2.

If none of the symbols specified in this section are shown, the internal logic 1-state corresponds with either of the following.

- (1) The external logic 1-state in a diagram of single logic rule.
- (2) The logic H-level in a diagram using the symbol for logic polarity.
In the latter diagram, external logic states do not exist.

The symbols for logic negation and logic polarity shall not be used together on the same diagram, except when internal connections with logic negation are to be shown on diagrams using the symbol for logic polarity (refer to symbols 4-2-2 and 4-2-4).

Table 2. Logic Negation, Logic Polarity Indicator and Dynamic Input

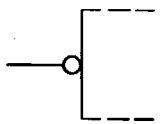
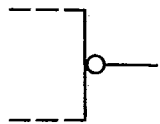
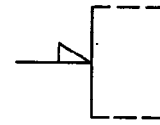
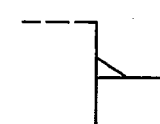
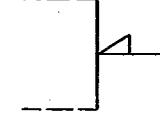
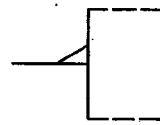
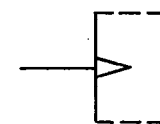
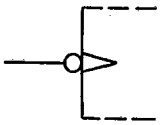
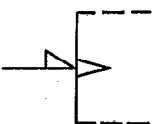
Symbol No.	Symbol	Description · Meaning
4-1-1 (12-07-01)		Logic negation, shown at an input
4-1-2 (12-07-02)		Logic negation, shown at an output The internal 1-state corresponds with the external 0-state. Note: The connecting line may extend through the circle.
4-1-3 (12-07-03)		Logic polarity, shown at an input Polarity indicator, shown at an input
4-1-4 (12-07-04)		Logic polarity, shown at an output Polarity indicator, shown at an output
4-1-5 (12-07-05)		Logic polarity } shown at an input in the Polarity indicator } case of signal flow from right to left
4-1-6 (12-07-05)		Logic polarity } shown at an output in Polarity indicator } the case of signal flow from right to left
4-1-7 (12-07-07)		Dynamic input The (transitory) internal 1-state corresponds with the transition from the external 0-state to the external 1-state. At all other times, the internal logic state is 0. On diagrams using the symbol for logic polarity the (transitory) internal 1-state corresponds with the transition from the L-level to the H-level on the connecting line. At all other times, the internal logic state is 0.

Table 2 (Continued)

Symbol No.	Symbol	Description • Meaning
4-1-8 (12-07-08)		Dynamic input with logic negation The (transitory) internal 1-state corresponds with the transition from the external 1-state to the external 0-state. At all other times the internal logic state is 0.
4-1-9 (12-07-08)		Dynamic input with polarity indicator The (transitory) internal 1-state corresponds with the transition from the H-level to the L-level on the connecting line. At all other times, the internal logic state is 0.

4.2 Internal Connection The symbols in this section define the relationships between internal logic states at internal connections as shown in Table 3.

Remark: An internal connection is a connection within a logic element. It is useful to be able to symbolize such a connection in order to show the logic relationships between elements whose outlines are combined. In many applications, it is also convenient to use the symbols in this section to show the function of complex elements. In such cases, dependency notation should be used to define the effects of any internal inputs or outputs.

Table 3. Internal Connection

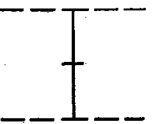
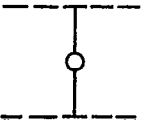
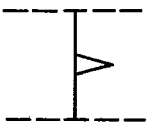
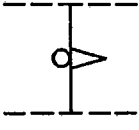
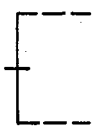
Symbol No.	Symbol	Description • Meaning
4-2-1 (12-08-01)		Internal connection The internal 1-state [0-state] of the input of the element on the right corresponds with the internal 1-state [0-state] of the output of the element on the left. Remark: This symbol may be omitted if no confusion can arise [refer to also 3.4 (3)].
4-2-2 (12-08-02)		Internal connection with negation The internal 1-state [0-state] of the element on the right corresponds with the internal 0-state [1-state] of the output of the element on the left. Remark: The vertical line may extend through the circle.

Table 3 (Continued)

Symbol No.	Symbol	Description · Meaning
4-2-3 (12-08-03)		Internal connection with dynamic character The (transitory) internal 1-state of the input of the element on the right corresponds with the transition from the internal 0-state to the internal 1-state of the output of the element on the left. At all other times, the internal logic state of the input of the element on the right is 0.
4-2-4 (12-08-04)		Internal connection with negation and dynamic character The (transitory) internal 1-state of the input of the element on the right corresponds with the transition from the internal 1-state to the internal 0-state of the output of the element on the left. At all other times, the internal logic state of the input of the element on the right is 0.
4-2-5 (12-08-05)		Internal input (virtual input) This input always stands at its internal 1-state unless it is affected by a dependency relationship that has an overriding or modifying effect (refer to symbols 6-8-12 and 6-11-5). Remarks 1. Internal inputs and outputs have internal logic states only. 2. Symbols of Section 4.1 shall not be applied to internal inputs and outputs, except symbol 4-1-7.
4-2-6 (12-08-06)		Internal output (virtual output) The effect of this output on an internal input to which it is connected must be indicated by dependency notation. Remark: The remarks 1 and 2 with symbol 4-2-5 apply.

4.3 Symbols inside the Outline Symbols inside the outline is qualifying symbols to be used inside the outline to specify the input-output characteristic or the function as shown in Table 4. If two or more inputs have the same qualifying symbols for the function, they are assumed to stand in an OR-relation, except in the case of bi-threshold and extension inputs (refer to symbols 4-3-2 and 4-3-10) where the relationship should be appropriately indicated.

- Remarks 1. The symbols in 4-3-14 to 4-3-23 do not indicate dynamic characteristics. If the inputs have the input dynamic characteristics, the symbols in 4-1-7 should be used in addition (Example: refer to symbol 6-10-6).

The internal logic states of these elements are determined by external logic states or external logic levels, and may be affected by other inputs (for example, C_m input).

2. Symbols 4-3-34 to 4-3-45 may be accompanied by numerals representing weight. When the weight is power of 2, only the exponent may be indicated.

Table 4. Symbols Inside Outlines

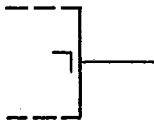
Symbol No.	Symbol	Description . Meaning
4-3-1 (12-09-01)		<u>Postponed Output</u> This symbol indicates that, in a sequential logic element and the like, the change of the internal state of this output is postponed until the input signal which initiates the change returns to its initial external logic state or logic level (in case the input is inter-connected, until the output of the first internal logic element returns to the first internal state again). (For example, the pulse trigger bistable element). So long as the internal stage of this input remains 1, the internal states of all affecting and affected inputs related to that input shall not be changed. When these inputs change, correct outputs cannot be assured. Remarks 1. Where only one specific output is to be postponed, the identifying symbols or numbers (both, if necessary) shall be prefixed to these symbols (refer to symbol 6-11-16). And if none are prefixed, the output related to each input of $\rightarrow$, $\leftarrow$, $+$, $-$ and T and the output related to C_m input and C_m output (refer to symbols 5-7-1 and 5.7.2) are postponed. 2. To avoid confusion with other symbols (for example, the figure 7), the symbol shall be two lines of equal length at right angles with each other. 3. For the applicaiton of this symbol and additional explanation, see 6.8.

Table 4 (Continued)

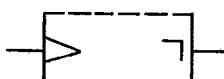
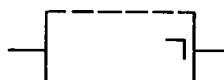
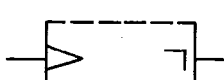
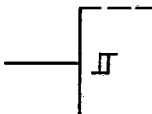
Symbol No.	Symbol	Description • Meaning
4-3-1 (12-09-01)		Example 1: In a diagram of the single logic rules  The internal state changes when the input changes from its external 1-state to its external 0-state.  The internal state changes when the input changes from its external 0-state to its external 1-state. Example 2: In a diagram of the polarity logic rules  The internal state changes when the input changes from its H-level to its L-level.  The internal state changes when the input changes from its L-level to its H-level.
4-3-2 (12-09-02)		Bi-threshold Input or Input with Hysteresis This symbol indicates that the internal state of input maintains 1, from that the external signal level of input exceeds the first threshold value V1, and returns to the second threshold value V2. Remarks 1. V1 shall be more positive (negative) than V2 when used in a diagram of the positive (negative) single logic rule or polarity logic rule. 2. When the logic negator or logic polarity indicator is indicated, the relationship between V1 and V2 is reversed.

Table 4 (Continued)

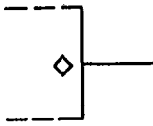
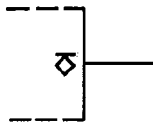
Symbol No.	Symbol	Description • Meaning
4-3-2 (12-09-02)		Remarks 3. When this symbol is used with other symbols, this symbol shall be indicated at the nearest position of the input line. 4. Refer to symbol 6-2-1 for the detail and application of this symbol.
4-3-3 (12-09-03)		<u>Open-circuit Output</u> This symbol indicates that either one of the internal logic states (1 and 0) of output corresponds with an external high-impedance condition, and also the possibility of distributed connection (refer to symbol 6-1-13). In the output circuit of this symbol, an externally connected load (or internal resistance of other elements) shall be required. Remarks 1. This symbol shall be drawn adjacent to the output line, except when using the bit-grouping symbol (symbol 12-09-25) in the manner defined in Section 25, where an alternative position is permitted. 2. Although this symbol is shown inside the outline, it refers to external states and levels only. 3. If it is necessary to indicate which logic level is the one with the low impedance, use can be made of symbol 4-3-4 or 4-3-5. Example: Open collector, open emitter, open drain, open source.
4-3-4 (12-09-04)		<u>Open-circuit Output (H-Type)</u> This symbol indicates that the output produces either the external high impedance state or relatively low impedance H-level (Example: refer to symbol 6-1-18). Remarks 1. Remarks 1 and 2 in symbol 4-3-3 apply. 2. The meaning of this symbol is not altered by the presence of a logic negation or logic polarity indicator. Example: PNP open collector, NPN open emitter, P channel open drain, N channel open source.

Table 4 (Continued)

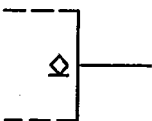
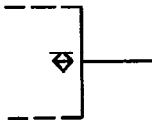
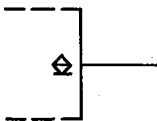
Symbol No.	Symbol	Description • Meaning
4-3-5 (12-09-05)		<u>Open-circuit Output (L-type)</u> This symbol indicates that the output produces either the external high impedance state or relatively low impedance L level (Example: symbol 6-1-17) Remark: Remarks 1 and 2 in symbol 4-3-3, and Remark 2 in symbol in symbol 4-3-4 apply. Example: NPN open collector, PNP open emitter, N channel open drain, P channel open source.
4-3-6 (12-09-06)		<u>Passive-pull-down Output</u> Similar to symbol 4-3-4, this symbol indicates that the output produces either the external high impedance state or relatively low impedance H level and the possibility of distributed connection. However, the output circuit of this symbol requires no external load. Remarks 1. This symbol shall be indicated approaching the output lines. However, if the bit grouping symbol (refer to symbol 4-3-26) is used with the method specified in 5.12.2, this symbol may be indicated at other positions. 2. The meaning of this symbol does not change even if there exists a logic negator or polarity indicator.
4-3-7 (12-09-07)		<u>Passive-pull-up Output</u> Similar to symbol 4-3-4, this symbol indicates that the output produces either the external high impedance state or relatively low impedance L level, and the possibility of distributed connection. However, the output circuit of this symbol does not require external lead. Remark: Remarks 1 and 2 in 4.3.6 apply.

Table 4 (Continued)

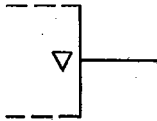
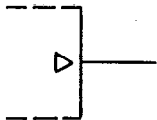
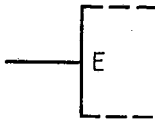
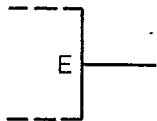
Symbol No.	Symbol	Description · Meaning
4-3-8 (12-09-08)		<u>3-state Output</u> This symbol indicates to have a third external high impedance state, having no logic significance, except 2 logic states. (Example: refer to symbol 6-1-32). Remark: This symbol shall be indicated approaching the output lines. However, if the bit grouping symbol (symbol 4-3-26) is used with the method specified in 5.12.2, this symbol may be indicated at other positions.
4-3-9		<u>Output with Special Amplification</u> This symbol emphasizes amplification function and indicates the direction of signal flow. In 6.1.3 a using example for an element as a general qualifying symbol is given. Remarks 1. This symbol shall be indicated approaching the output lines. However, if the bit grouping signal (symbol 4-33-6) is used with the method specified in 5.12.2, the symbol may be indicated at other positions. 2. When this symbol is used with symbols 4-3-3 to 4-3-8, those symbols shall be indicated more approaching the output line than the amplification symbol.
4-3-10 (12-09-09)		<u>Extension Input</u> This symbol indicates an input connected with the output of extension element (refer to symbol 4-3-11). Remark: A description representing the relation between external logic state and external logic level is not applies to the extended input and output.
4-3-11 (12-09-10)		<u>Extender Output</u> This symbol indicates the output connected to the extension input of other elements. Remark: The remark in symbol 4-3-10 applies.

Table 4 (Continued)

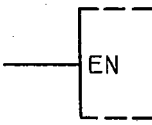
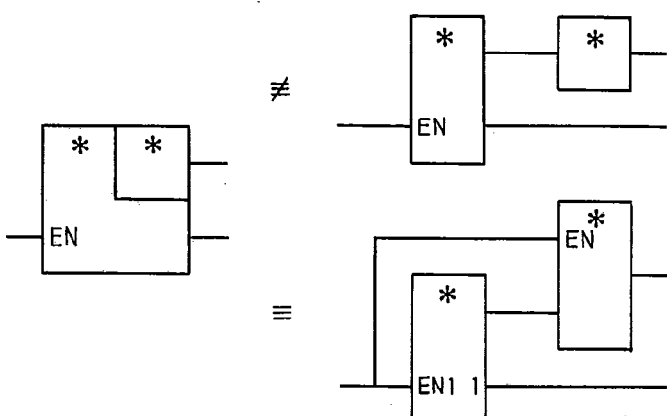
Symbol No.	Symbol	Discription · Meaning
4-3-12 (12-09-11)		<u>Enable Input</u> This symbol indicates that if this input stands at its internal 1-state all outputs stand at their internal logic states defined by other symbols and have effects defined by other symbols on elements or distributed elements that may be connected to the outputs (refer to examples 1 to 3). When the internal state of input is 0, each output state is as follows: (1) <u>Open-circuit Output</u> (Symbols 4-3-3 to 4-3-5) External high impedance states. (2) <u>Pull-down Output</u> L-levels of high impedance. (3) <u>Pull-up Output</u> H-levels of high impedance. (4) <u>3-state Output</u> Internal logic states and external high impedance states defined by other symbols. (5) <u>Other Outputs</u> Internal states 0. Remark: This input only affects outputs shown as external outputs. If it is an input of an element having an internal connection indicated by one of the symbols 4-2-1 to 4-2-4, it is also an input of internally connected element (including the case that the remark in symbol 4-2-1 can be applied). If confusion can arise, the enable dependency as defined in 5.9 may be used (refer to examples 1 to 3). Example 1. 

Table 4 (Continued)

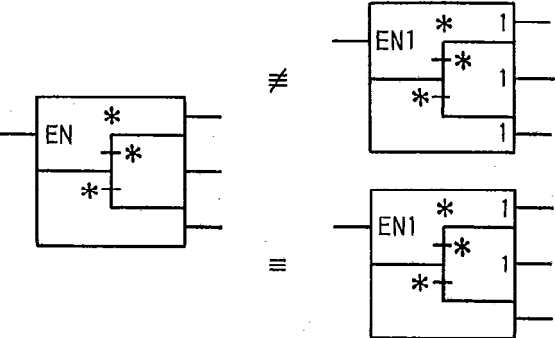
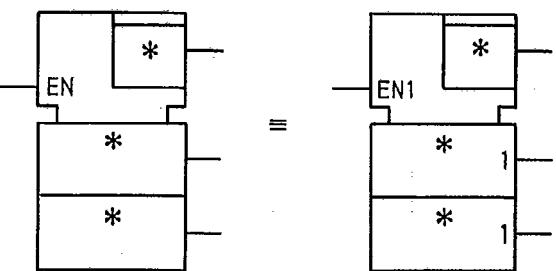
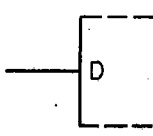
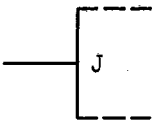
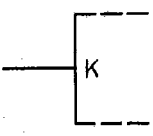
Symbol No.	Symbol	Discription • Meaning
4-3-12 (12-09-11)		<u>Example 2:</u>  <u>Example 3:</u> 
4-3-13 (12-09-12)		<u>D-input</u> This symbol indicates that the internal logic state of the D-input is stored by the element (refer to symbol 6-8-2). Remark: The internal logic state of this input is always subject to an affecting input or output.
4-3-14 (12-09-13)		<u>J-input</u> This symbol indicates that when this input takes on its internal 1-state, a 1 is stored by the bistable element. When the input stands at its internal 0-state, it has no effect on the element.
4-3-15 (12-09-14)		<u>K-input</u> This symbol indicates that when this input takes on its internal 1-state, a 0 is stored by the bistable element. When the input stands at its internal 0-state, it has not effect on the element.

Table 4 (Continued)

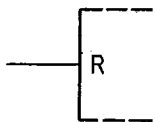
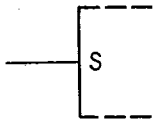
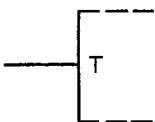
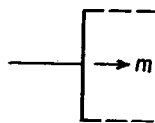
Symbol No.	Symbol	Description . Meaning
4-3-15 (12-09-14)		Each occurrence of the combination $J = K = 1$ causes a single change of the internal state of the output to its complement. Remark: This symbol does not indicate dynamic inputs (refer to Remark 1 of 4.3).
4-3-16 (12-09-15)		<u>R-input</u> This symbol indicates that when this input takes on its internal 1-state, a 0 is stored by the bistable element. When the input stands at its internal 0-state, it has no effect on the element.
4-3-17 (12-09-16)		<u>S-input</u> This symbol indicates that when this input takes on its internal 1-state, a 1 is stored by the bistable element. When the input stands at its internal 0-state, it has no effect on the element. The effect of the combination $R = S = 1$ is not specified by the symbol; this effect may be indicated by means of SET-/RESET-dependency (refer to 5.8). Remark: This symbol does not indicate dynamic inputs (refer to Remark 1 of 4.3).
4-3-18 (12-09-17)		<u>T-input</u> This symbol indicates that each time this input takes on its internal 1-state, a single change of the internal state of the output to its complement takes place. When the input stands at its internal 0-state, it has no effect on the element. Remark: This symbol does not indicate dynamic inputs (refer to Remark 1 of 4.3).
4-3-19 (12-09-18)		<u>Shifting Input, Left to Right or Top to Bottom</u> This symbol indicates that each time this input takes on its internal 1-state, the information contained in the register element will be shifted once m positions from left to right or from top to bottom, depending on the orientation of the symbol for the element. When the input stands at its internal 0-state, it has no effect on the element.

Table 4 (Continued)

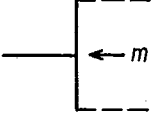
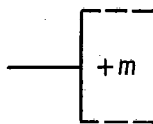
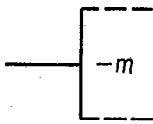
Symbol No.	Symbol	Discription • Meaning
4-3-19 (12-09-18)		Remarks 1. This symbol does not indicate dynamic inputs. 2. "m" shall be replaced by the relevant value. If $m = 1$, the 1 may be omitted.
4-3-20 (12-09-19)		<u>Shifting Input, Right to Left or Bottom to Top</u> This symbol indicates that each time this input takes on its internal 1-state, the information contained in the element will be shifted once "m" positions from right to left or from bottom to top, depending on the orientation of the symbol for the element. When the input stands at its internal 0-state, it has no effect on the element. Remarks 1. This symbol does not indicate dynamic inputs (refer to Remark 1 in 4.3). 2. "m" shall be replaced by the relevant value. If $m = 1$, the 1 may be omitted.
4-3-21 (12-09-20)		<u>Counting-up Input</u> This symbol indicates that each time this input takes on its internal 1-state, the count of the element is increased once by m units. When the input stands at its internal 0-state, it has not effect on the element. Remarks 1. This symbol does not indicate dynamic inputs (refer to Remark 1 in 4.3). 2. "m" shall be replaced by the relevant value. If $m = 1$, the 1 may be omitted.
4-3-22 (12-09-21)		<u>Counting-down Input</u> This symbol indicates that each time this input takes on its internal 1-state, the count of the element is decreased once by m units. When the input stands at its internal 0-state, it has no effect on the element. Remarks 1. This symbol does not indicate dynamic inputs (refer to Remark 1 in 4.3).

Table 4 (Continued)

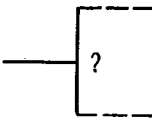
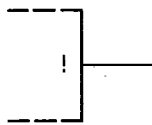
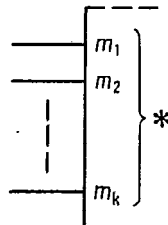
Symbol No.	Symbol	Description · Meaning
4-3-22 (12-09-21)		Remark 2. "m" shall be replaced by the relevant value. If $m = 1$, the 1 may be omitted.
4-3-23 (12-09-22)		<u>Query Input of an Associative Memory/Interrogative Input of an Associative Memory</u> This symbol indicates that if this input takes on its internal 1-state, an interrogation of the content of the element takes place. If the input stands at its internal 0-state, it has no effect on the element. Remark: This symbol does not indicate dynamic inputs (refer to Remark 1 in 4.3).
4-3-24 (12-09-23)		<u>Compare Output of an Associative/Match Output of an Associative Memory</u> This symbol indicates that the internal 1-state at this output indicates a match between the contents of associative memory and query input.
4-3-25 (12-09-24)		<u>Bit Grouping for Multibit Input</u> This symbol indicates that inputs grouped by this symbol produce a number that is the sum of the inputs standing at their internal 1-states. The individual inputs shall be shown in ascending or descending order by weight. The sum represents any of the following: (1) Operand of arithmetic operation (2) Identifying number in the sense of dependency notation (5.12.2). (3) A value to become the content of the element. "$m_1, \dots, m_k$" shall be replaced by the decimal equivalents of the actual weights. If all weights are powers of 2, "$m_1, \dots, m_k$" may be replaced by the exponents of the powers of 2 (refer to Examples). Labels between "m_1" and "m_k" may be omitted to the extent that no confusion can arise.

Table 4 (Continued)

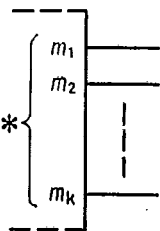
Symbol No.	Symbol	Description . Meaning
4-3-25 (12-09-24)		"*" must be replaced by any of the following: (1) An appropriate indication of the operand of arithmetic operation (e.g. P or Q) (2) An appropriate indication in the sense of dependency notation. (3) CT (Content value of elements) (refer to symbol 4-3-46). <u>Example 1:</u> $\left. \begin{array}{c} \text{---} 0 \\ \text{---} \\ \text{---} \\ \text{---} \\ \text{---} 4 \end{array} \right\} * \equiv \left. \begin{array}{c} \text{---} 1 \\ \text{---} \\ \text{---} \\ \text{---} \\ \text{---} 16 \end{array} \right\} *$ <u>Example 2:</u> $\left. \begin{array}{c} \text{---} 4 \\ \text{---} \\ \text{---} \\ \text{---} 7 \end{array} \right\} * \equiv \left. \begin{array}{c} \text{---} 16 \\ \text{---} \\ \text{---} \\ \text{---} 128 \end{array} \right\} *$
4-3-26 (12-09-25)		<u>Bit Grouping for Multibit Output</u> This symbol indicates that the outputs grouped by this symbol represent a number that is the sum of the individual weights of the outputs standing at their internal 1-states. The individual outputs shall be shown in ascending or descending order by weight. The sum represents any of the following: (1) The value of results of arithmetic operation (2) The value of contents of the element.

Table 4 (Continued)

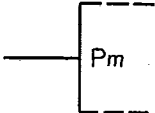
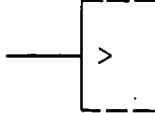
Symbol No.	Symbol	Description · Meaning
4-3-26 (12-09-25)		"$m_1, \dots, m_k$" shall be replaced by the decimal equivalents of the actual weights. If all weights are powers of 2, "$m_1, \dots, m_k$" may be replaced by the exponents of the powers of 2. Labels between m_1 and m_k may be omitted to the extent that no confusion can arise (refer to example). "*" must be replaced by any of the following: (1) An appropriate indication of the operand of arithmetic operation (2) CT (Content value of elements) (refer to symbol 4-3-47). Example: $* \begin{Bmatrix} 0 \\ 2 \\ 4 \\ 6 \end{Bmatrix} \equiv * \begin{Bmatrix} 1 \\ 4 \\ 16 \\ 64 \end{Bmatrix}$
4-3-27 (12-09-26)		<u>Operand Input (P_m-Input Shown)</u> This symbol indicates the input which represents one bit of an operand in the arithmetic operation. Remarks 1. "m" shall be replaced by appropriate numerals. If the weights of all inputs are powers of 2, at each input "m" may be replaced by the exponent. 2. If an operand consists of two or more bits, the bit grouping symbol (symbol 4-3-25) may be used. 3. Preferred letters for operands are P and Q. If these letters are not suitable or if more than two operands are involved, other characters may be used providing no confusion can arise.
4-3-28 (12-09-27)		<u>Greater-than Input of a Magnitude Comparator</u> This symbol indicates a direction to put in the >(greater than) output of former stage as the input of comparators (Example: refer to symbol 6-6-16).

Table 4 (Continued)

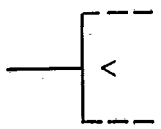
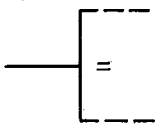
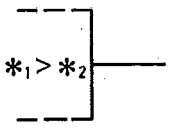
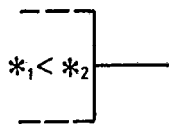
Symbol No.	Symbol	Description · Meaning
4-3-28 (12-09-27)		Remarks 1. Symbols 4-3-28 to 4-3-30 may be combined such as $\geq$ (or $\leq$), $\leq$ (or $\geq$), $\geq$. 2. This symbol shall not be represented adjacent to symbol outlines for fear of confusion.
4-3-29 (12-09-28)		<u>Less-than Input of a Magnitude Comparator</u> This symbol indicates putting in the < (less than) output of former stage in the comparator (example: refer to symbol 6-6-16). Remark: Remark 1 of 4-3-28 applies.
4-3-30 (12-09-29)		<u>Equal Input of a Magnitude Comparator</u> This symbol indicates putting in the = (equal) output of former stage in the comparator (example: refer to 6-6-16). Remark: Remark 1 in symbol 4-3-28 applies.
4-3-31 (12-09-30)		<u>Greater-than Output of a Magnitude Comparator</u> This symbol indicates the > (greater than) output of the comparator. When the value of operand "$*_1$" is greater than that of "$*_2$", the internal state of output becomes 1. Remarks 1: "$*_1$" and "$*_2$" shall be replaced by the appropriate designations of operands, for example, P and Q, respectively. 2: Symbols 4-3-31 to 4-3-33 may be combined to such as $*_1 \geq *_2$ (or $*_1 \leq *_2$), $*_1 \leq *_2$ (or $*_1 \geq *_2$), $*_1 \geq *_2$. 3. If this symbol is used in one element of a series of cascade comparators, the output marked with this symbol is affected not only by the operands, but also by the inputs marked with symbols 4-3-28 to 4-3-30.
4-3-32 (12-09-31)		<u>Less than Output of a Magnitude Comparator</u> This symbol indicates < (less than) output of the comparator. When the value of operand "$*_1$" is less than that of "$*_2$", the internal state of output becomes 1. Remark: Remarks 1 to 3 in symbol 4-3-31 applies.

Table 4 (Continued)

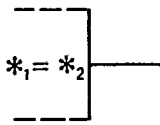
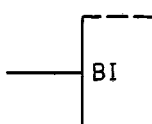
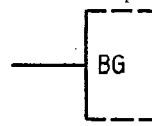
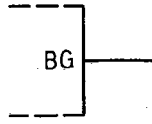
Symbol No.	Symbol	Description · Meaning
4-3-33 (12-09-32)		<u>Equal Output of a Magnitude Comparator</u> This symbol indicates = (equal) output of the comparator. When the value of operand "$*_1$", is equal to that of "$*_2$", the internal state of output becomes 1. Remarks 1. Remarks 1 to 3 in symbol 4-3-31 apply. 2. If this symbol is used solely, the operands may be omitted providing no confusion can arise.
4-3-34 (12-09-33)		<u>Borrow-in Input of an Arithmetic Element</u> This symbol indicates that in an arithmetic element operating subtraction, the borrow-in output from the lower figure is set as the input. Remark: Remark 2 in 4.3 applies.
4-3-35 (12-09-34)		<u>Borrow-generate Input of an Arithmetic Element</u> This symbol indicates that in an arithmetic element operating look ahead borrow generation, the BG output of the lower figure is set as the input (refer to symbol 4-3-36). The borrow generation due to the foresight borrow generation shall be determined using BG, BP and BI input signal to reduce the propagation delay. Remark: Remark 2 in 4.3 applies.
4-3-36 (12-09-35)		<u>Borrow-generate Output of an Arithmetic Element</u> This symbol indicates that in an arithmetic element operating subtraction, when the borrow generates from the figure independent of the lower figure, the internal state becomes 1. Remark: Remark 2 in 4.3 applies.

Table 4 (Continued)

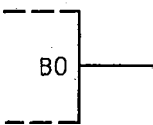
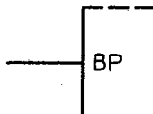
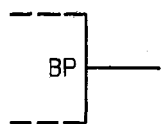
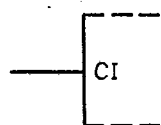
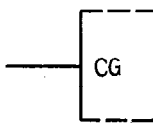
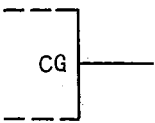
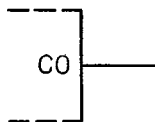
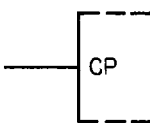
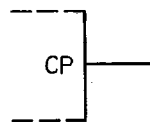
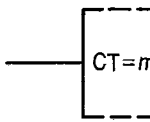
Symbol No.	Symbol	Description • Meaning
4-3-37 (12-09-36)		<u>Borrow-out Output of an Arithmetic Element/Ripple-borrow Output of an Arithmetic Element</u> This symbol indicates that in an arithmetic element operating subtraction, when the borrow generates from that figure, the inter state becomes 1. Remark: Remark 2 in 4.3 applies.
4-3-38 (12-09-37)		<u>Borrow-propagation Input of an Arithmetic Element</u> This symbol indicates that in an arithmetic element operating the look ahead borrow generation, the BP output of lower figure is set to the input (refer to symbol 4-3-39). Remark: Remark 2 in 4.3 applies.
4-3-39 (12-09-38)		<u>Borrow-propagate Output of an Arithmetic Element</u> This symbol indicates that in an arithmetic element of operating subtraction, when the subtracting and subtracted numbers are equal, and the borrow is generated if the borrow of lower figures exists, the internal state becomes 1. Remark: Remark 2 in 4.3 applies.
4-3-40 (12-09-39)		<u>Carry-in Input of an Arithmetic Element</u> This symbol indicates that in an arithmetic element operating addition, the carry output from the lower figure is set to the input. Remark: Remark 2 in 4.3 applies.
4-3-41 (12-09-40)		<u>Carry-generate Input of an Arithmetic Element</u> This symbol indicates that in an arithmetic element generating look ahead carry, the CG output of lower figure is set to the input (refer to symbol 4-3-42). The carry by the look ahead carry-generate is determined using CG, CP and CI input to reduce the propagation delay. Remark: Remark 2 in 4.3 applies.

Table 4 (Continued)

Symbol No.	Symbol	Description · Meaning
4-3-42 (12-09-41)		<u>Carry-generate Output of an Arithmetic Element</u> This symbol indicates that in an arithmetic element of operating addition, when the carry from the figure is generated independent of the carry from the lower figure, the internal state becomes 1. Remark: Remark 2 in 4.3 applies.
4-3-43 (12-09-42)		<u>Carry-out Output of an Arithmetic Element</u> <u>Ripple-carry Output of an Arithmetic Element</u> This symbol indicates that in an arithmetic element, when the carry is generated in that figure, the internal state becomes 1. Remark: Remark 2 in 4.3 shall be applied.
4-3-44 (12-09-43)		<u>Carry-Propagate Input of an Arithmetic Element</u> This symbol indicates that in an arithmetic element operating the look ahead carry generation, the CP output of lower figures is set to the input. (refer to symbol 4-3-45). Remark: Remark 2 in 4.3 applies.
4-3-45 (12-09-44)		<u>Carry-propagate Output of an Arithmetic Element</u> This symbol indicates that in an arithmetic element operating addition, when the result of addition is 1 less than the carry-condition and generates carry if the carry from the lower figure exists, the internal state becomes 1. Remark: Remark 2 in 4.3 applies.
4-3-46 (12-09-45)		<u>Content (CT) Input</u> This symbol indicates that when the internal state of the input is 1, the content value of element (e.g. a counter) becomes "m". "m" shall be replaced by an appropriate numeral (example: refer to symbol 6-11-17). If the internal state of the input of this symbol is "0", it has no effect on the element.