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9.1 Functional Description of Module

In order to improve the effective communication range of Solid State Interlocking (SSI) data transmission systems, the Long Distance Terminal was developed. The Functions of the LDT can be summarised as follows:

- The SSI works at a nominal data rate of 20kbts/s. The LDT converts this SSI data rate to 64kbts/s using First-In-First-Out registers (FIFOs) and suitably converts signal levels from the SSI standards to G703 levels suitable for transmission using telecommunications bearer systems channels.
- It adds and subtracts the hardwired Control Centre Identity to protect against data being incorrectly routed through the telecommunications bearer system.
- It adds additional coding protection to the transmitted telegrams by sending each one in normal and inverted senses, this is to provide protection against bit errors in the telecommunications bearer systems.
- It manages message handling to and from the SSI and manages the protocol where reply messages are returned to the interlocking in the minor cycle subsequent to that in which the corresponding interlocking telegram was sent.
- It manages itself in that it carries out many internal safety checks to ensure that it is not holding on to out-of-date data and to prove its internal hardware is functioning correctly.

Interlocking and one or more trackside LDTs are provided for each of the two Data Links provided for an SSI Central Interlocking (CI). The interlocking LDTs are located inside the CI cubicle in place of the trackside Data Link Modules (DLM). Trackside LDTs can drive modules directly or be connected to a Data Link Module to transmit data via a baseband Data Link. Both Interlocking and Trackside LDTs are connected to a contra-directional G703 telecommunications bearer system channel. All connections to/from the LDT are made through a single 75-way Trident connector.

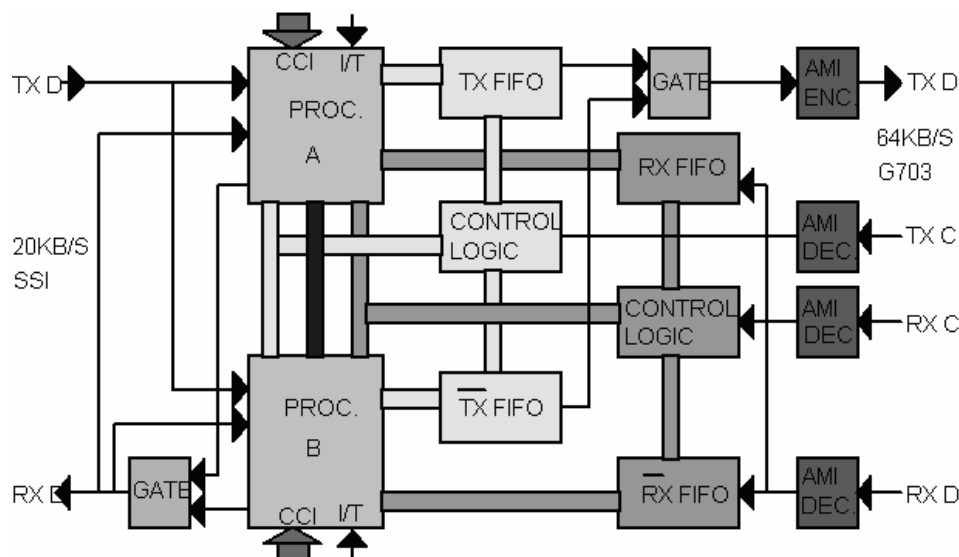
Only ALSTOM have manufactured SSI LDTs.

9.2 Module Details and Operation

The LDT is contained in a half-size SSI trackside module case (100 x 365 mm), the same size as a DLM. The front panel of the case carries the manufacturer's plate, 75-way Trident connector, indicators and carrying handles / securing bolts. Unlike the majority of SSI modules, the LDT is equipped with a large number of indicators. The names of these indicators, how they are derived and what they mean when on/off is shown in Section 9.3 of this document. The rear of the case has no controls or indications but is the site of two case-retaining

bolts. The top of the case is fitted with two bolts that carry the module's seal. The power supply to the module is a nominal 110 Va.c. or 12 Vd.c.

The LDT is a dual processor module and each processor runs a non-site specific functional program held in EPROM. At present there is only a Mk1 LDT and they have only ever been produced by ALSTOM Signalling Limited (or predecessor companies).



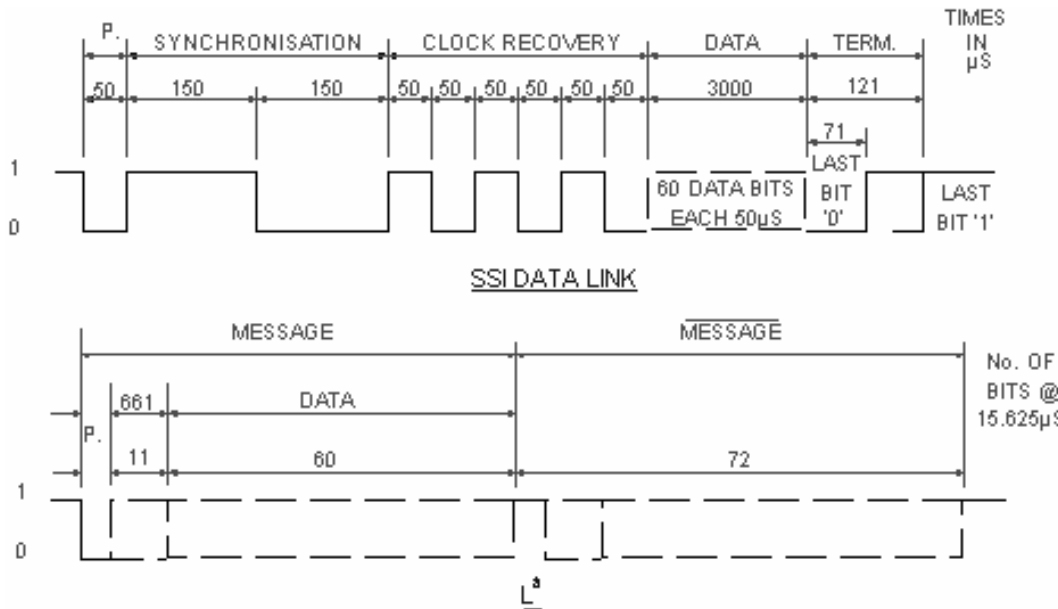
Schematic diagram of internal circuitry of an LDT

The schematic diagram of the circuitry of an LDT is shown above. The unit has dual processors, each with their own CCI and Interlocking/Trackside input circuitry, transmit and receive FIFOs and control logic. The unit is fitted with Alternate Mark Inversion (AMI) circuitry to allow direct connection to telecommunications bearer systems. As can be seen from the telecommunications interface on the right-hand side of the diagram, all clocking is done by the telecommunications equipment.

In order to send a message from the 20kbit/s SSI interface to the 64kbit/s G703 interface the events described in the following paragraphs take place:-

- Processors A & B detect the start of a baseband message coming in on the 20kbits/s current loop interface by detection of the first bit, called the precursor. The precursor is marked with a 'P' on the SSI data link telegram diagram shown below.
- Whilst reading and checking the 12 bit synchronisation and clock recovery pattern (each of the synchronisation pulses counts as three bits) of that message both processors clock the value of the hardwired Control Centre Identity (CCI) into their respective transmit First-In-First-Out (FIFO) registers. The Manchester coded telegram data is then clocked into the transmit FIFOs as it is read from the SSI. Both

processors run the same program but due to additional hardware on the B processor side of the LDT the B message is sent to the G703 interface inverted. The makeup of the telecommunications bearer system, or Long Line Link (L3), message is also shown below.



SSI baseband and Long Line Link telegram formats

- Transmission of data to the G703 interface can commence as soon as enough data has been clocked into the transmit FIFOs. The point at which G703 transmission starts is controlled by the LDT such that the last 20kbits/s data will have been clocked into the FIFOs before it is clocked out by the 64kbits/s clock from the telecommunications bearer system.

To receive a message from the 64kbits/s G703 interface of the PCM the following happens:

- The data stream from the remote LDT is clocked into the two receive FIFOs. Control logic detects the start of the message and steers the normal and complementary messages into the A & B FIFOs respectively. As soon as the first bit of the complementary message is received in the 'not receive' FIFO both the A & B processors begin to unload their respective FIFOs at 20kbits/s.
- As the message is clocked from the receive FIFOs the precursor, synchronisation and clock recovery patterns are reinstated and the Control Centre Identity received from the remote end is compared with the locally hardwired version. If the local and remote CCIs are different the output process is aborted. When the end of the telegram is reached the message terminator is reinstated.

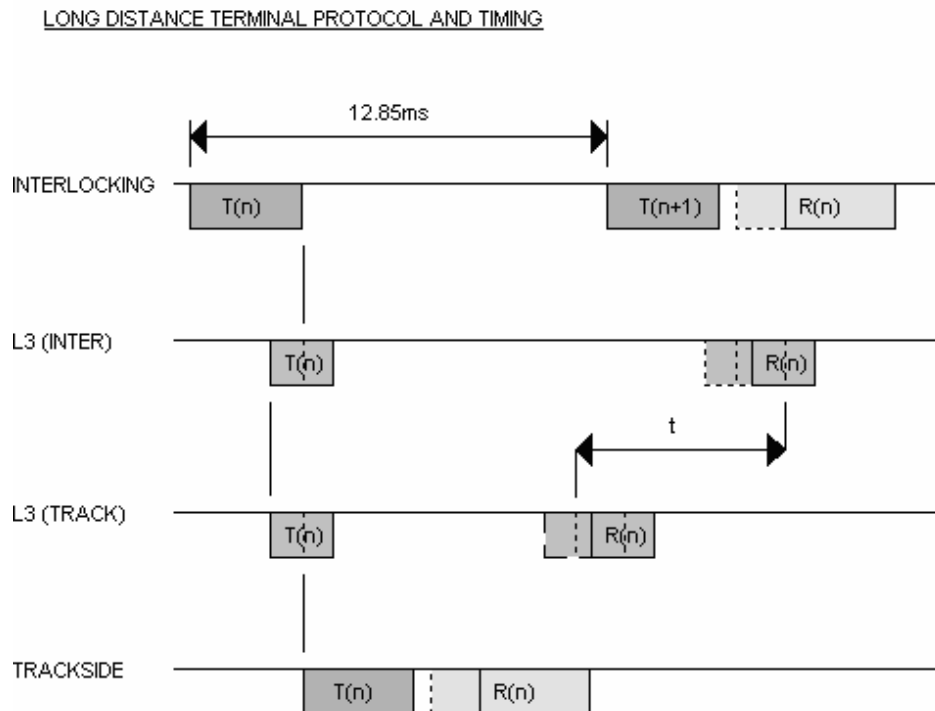
- The processors take it in turns to transmit telegrams to the SSI interface and both check the content of each telegram as it is sent. Should either processor consider the data being sent to the SSI interface to be incorrect it will force the data to an invalid state.
- It should be clear that the LDT is talking to both the 20kbits/s SSI interface and to the 64kbits/s PCM interface. Depending where the LDT is located it must be synchronised to data coming from the SSI CI or telecommunications bearer system, this selection is made by virtue of hardwired strapping within the free-connector to the LDT. Two straps are required at each LDT and they should be connected to the relevant (A/B) logic '1' for the interlocking LDT or logic '0' for the Trackside LDT; details of these connections will be shown in a site's schematic diagrams.

It should be clear from the description above that the FIFO memories are crucial to the operation of the LDT in that they are the device in which the bit rate conversion is carried out. FIFOs could be thought of as a type of shift register, with one major difference, whatever is clocked in first ripples through to the output and is able to be clocked out on demand. Data will come out in the same order that it went in, but need not be clocked out at the same rate. In the LDT the data is clocked into the transmit FIFOs at 20kbits/s and out at 64kbits/s. The receive FIFOs have data clocked in at 64kbits/s and out at 20kbits/s.

SSI telegrams received by the LDT are encoded in the FIFO registers as has been described. Before this data is sent to the Telecommunications bearer systems it is subject to one further alteration to make it suitable for transmission through a transformer based G703 interface; that final process is Alternate Mark Inversion (AMI) coding. This is required to convert the logic levels used inside the LDT to bipolar levels suitable for transmission to the telecommunications transmission system.

The links to the PCM consist of four pairs of wires, all of which are balanced lines similar to a baseband data link, the characteristic impedance of these lines should be 120 ohms. To keep the d.c. sum of signals on these lines at zero and to allow strings of logic 1s to be sent through the transformers, every subsequent logic 1 or 'mark' is inverted by the AMI encoder.

On an LDT system interlocking, telegrams are spaced at a minimum of 12.85 ms though this can also increase to 30 ms or 120 ms in the same way as in a baseband system. As soon as enough data has been clocked into the transmit FIFOs to stop the telecommunications system out-clocking the LDT, transmission begins. The message is sent normal and inverted and takes 2.25 ms. The diagram below shows LDT system timing; this diagram lumps the telecommunications transmission delays in order to show the time available for Long Line Link transmission 't'.



SSI Long Line Link timing diagram

As soon as just over half of the message is received at the trackside it can start to be clocked out to the SSI trackside Baseband link. The trackside modules reply in the normal way between 4.0 ms and 5.3 ms after the start of the interlocking telegram, these replies are received by the LDT and sent on to the telecommunications bearer system in a similar way as those from the interlocking.

When this message is received from the telecommunications bearer system it is held in the interlocking LDT until it can be inserted at the desired point following the transmission of the next outgoing telegram. It should be apparent what differences exist between baseband and LDT transmission i.e. the replies are returned to the interlocking in the reply period of the minor cycle subsequent to that in which the initiating outgoing telegram was sent (n+1 protocol).

An interlocking must be programmed to expect replies arriving in this fashion in its data programs if it is using LDT transmission. An interlocking must use either all baseband or all LDT (with or without subsequent baseband) transmission - the two cannot be mixed.