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Level 2

Signalling Design: Module B11 -

Interlockings – Electronic Interlocking Guidelines

Endorsement and Authorisation

For endorsement and authorisation, please refer to NR/L2/SIG/11201

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Issue record

Issue	Date	Comments
4	June 2011	Modularisation of handbook and guidance notes, contains content of former NR/GN/SIG/11600, Appendix F4.

Compliance

This Module is mandatory and shall be complied with by Network Rail and its contractors if applicable from 03/09/2011.

When this standard is implemented, it is permissible for all projects that have formally completed GRIP Stage 3 (Option Selection) to continue to comply with the issue of any relevant Network Rail standards current when GRIP Stage 3 was completed and not to comply with requirements contained herein, unless stipulated otherwise in the scope of this standard.

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1 INTRODUCTION

This module describes the factors for consideration in the design and selection of electronic interlocking systems.

[NR/L2/SIG/11201, Module B7](#), Section 3 laid down the requirements for interlocking controls and specified their tabulation in control tables. The application of the principles and requirements to route setting systems are summarised in [NR/L2/SIG/11201, Module B7](#), Section 7. This module demonstrates how those controls may be provided by the use of electronic data.

2 ELECTRONIC SYSTEMS

All new systems shall be approved in accordance with [NR/L2/EBM/029](#) and comply with the following requirements:

- a) Her Majesty's Railway Inspectorate safety principles;
- b) demonstration of an acceptable level of safety, with assurance of system safety under all failure conditions, including power failure;
- c) an acceptable level of dependability;
- d) compatible interfaces between hardware, software and other systems, including electro-magnetic compatibility;
- e) testability, including the ability to validate individual sub-systems separately, e.g. by disconnecting output comparators; and
- f) the occupational safety of personnel working on the system.

These requirements may be achieved by the use of commercially available programmable logic controllers of an appropriate safety integrity level.

A balance of diversity and redundancy should be used in developing the system architecture, so as to achieve the required safety and availability. If necessary, graceful degradation should be used to maintain availability with reduced functionality in the event of system failure. Some examples of system architecture are given in Figure :1.

Whole life-cycle management, including verification and validation, should be provided for each phase of design, in accordance with [BS EN 50129](#). Software requirements are given in [BS EN 50128](#) and dependability requirements in [BS EN 50126](#).

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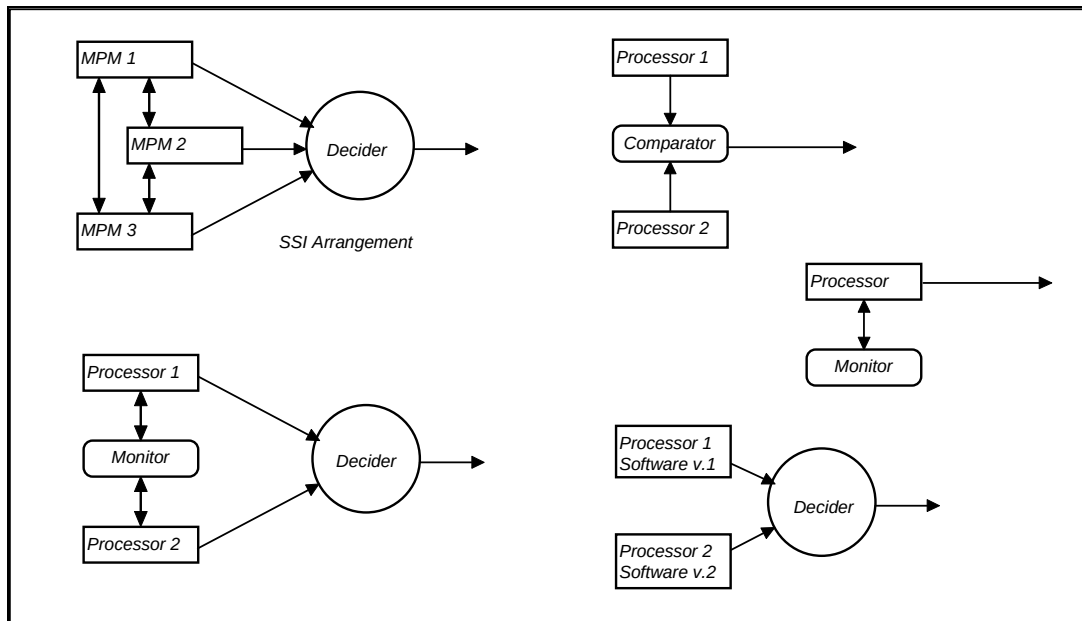


Figure 1 – Examples of Electronic Interlocking Architecture

The requirements for configuration control of data driven systems are laid down in [NR/L2/SIG/11201](#).

For the protection of programmable electronic systems against interference see [NR/L2/SIG/11201, Module B3](#).

2.1 LADDER LOGIC FOR PROGRAMMABLE LOGIC CONTROLLERS

The data is usually written in the form of ladder logic, which is a series of logic equations generally evaluated in sequence during each cycle of the processor. The logic enables an output to be determined for a given range of inputs. This can be illustrated by means of a truth table, as shown in Figure :2.

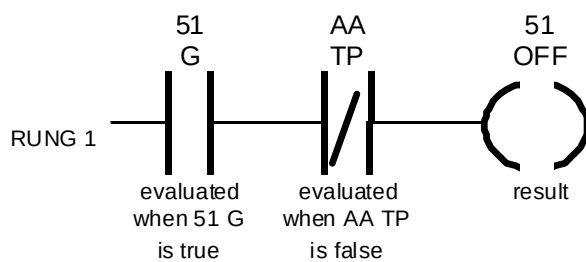
The logic equations with series and parallel logic elements can be almost directly related to relay logic, including the use of latches for stick relays.

Rules should be developed for the preparation of data for use in programmable logic controllers to confirm safe, consistent and stable outputs. These should confirm that:

- equations are kept as simple as practicable to confirm that no unintended paths are present;
- stability is achieved, e.g. by logic equations only containing elements that have already been evaluated on a previous “rung of the ladder”;
- cycle times are minimised, e.g. by arranging equations with the main switching elements at the beginning, so that elements beyond the first “false” element do not have to be evaluated; and
- consistent names (or mnemonics) are used for the internal elements, as described in [NR/L2/SIG/11201, Module A15](#).

A typical logic equation (or “ladder rung”) is depicted in Figure :2.

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51 G	AA TP	51 OFF
0	0	0
0	1	0
1	0	1
1	1	0

Figure 2 – Ladder Logic and Truth Table

Various logic features, such as timers and latches can be incorporated. An internal timer should comprise both a start condition logic element and an end condition logic element, such that the end condition becomes true a predetermined time after the start condition becomes true. The timer can be reset at any time by making the start condition false.

Data preparation tools should have a safety integrity level commensurate with their application. Guidance is given in [NR/L2/SIG/11201, Module A21](#).

3 SOLID STATE INTERLOCKING (SSI)

The Solid State Interlocking developed by GEC-GS, WBS and BRB is one example of an electronic interlocking system.

This section describes some of the concepts upon which SSI is based to allow comparison with other interlocking systems and demonstrate compliance with the design requirements in [NR/L2/SIG/11201, Module B7](#), Section 3. It does not lay down design requirements which are given in [SSI 8500](#) in the SSI applications manual, [NR/L2/SIG/17002](#).

Figures :3 and :4 identify how the standard controls are applied to SSI and provide a comparison with the other interlocking systems.

3.1 GENERAL DESCRIPTION

The standard SSI interlocking cubicle contains the following modules in a single rack, the dimensions complying with [BS EN 60297-3-101:2004](#):

- three interlocking multi-processor modules (MPMs) to specification [BR 1905A](#);
- deduplicated panel processor modules (PPMs) to BR 1908 that communicate with a signalling display system (SDS) or panel multiplexer (as described in [BR 1921](#)), transmitting safety-related controls and indications over a link that is not safety critical;
- a diagnostic multi-processor module to [BR 1905A](#);
- two data link modules (DLMs) to [BR 1904](#), or long distance terminals (LDTs) to [BR 1906](#) that transmit operating commands and receive proving information from trackside functional modules (TFMs) to BR 1901 (points modules) or