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Methodology for the demonstration of compatibility with HVI Track Circuits (formerly RT/E/C/50007)

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The Ref above will be formally allocated to this standard when it is next changed in the meantime the contents, date and issue number of this Network Rail Standard are UNCHANGED and with immediate effect it should be referred to as “(new ref) formerly (old ref)”.

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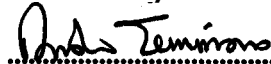
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METHODOLOGY FOR THE DEMONSTRATION OF COMPATABILITY WITH HVI TRACK CIRCUITS

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ISSUE RECORD

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I	February 2003	New Code of Practice

IMPLEMENTATION

The provisions of this code of practice may be used from the date of issue.

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I INTRODUCTION

I.1 Purpose

The purpose of this document is to provide a methodology to demonstrate compatibility of trains with HVI track circuits on the a.c. and d.c. railways on Railtrack controlled infrastructure. This is achieved by:

- Providing a model of the infrastructure for the a.c. and d.c. railways
- Providing a methodology for taking the line current recordings and using the infrastructure model producing a corresponding rail to rail voltage at the receiver
- Defining a methodology to play the rail to rail voltage into a HVI receiver
- Defining the criteria for the demonstration of compatibility

These elements form the basis of a test for checking the compatibility of trains with HVI track circuits.

I.2 Scope

This document describes a method by which a train's compatibility with HVI track circuits used on Railtrack's a.c. and d.c. electrified infrastructure can be assessed.

I.3 Installation Types Covered By This Document

This document covers HVI track circuits installed in single rail mode on the a.c. and d.c. railway only.

I.4 Equipment types included in this document

The receiver equipment type covered by this document is NCO.RTV.600 which is used by Railtrack, this variant does not include the 4 terminal capacitor included in some HVI variants. Some HVI track circuits have been fitted with an external capacitor (ref.5). These will be replaced in due course by a variant specific to Railtrack in which the capacitor will be an integral part. The effect of the capacitor is to reduce the track circuits susceptibility to high frequency interference (>4kHz ref.3). By ignoring the capacitor, this methodology is pessimistic.

2. SOURCE DOCUMENTS

2.1 Group Standards

1. GK/RC0752 General information on track circuits, Issue 2, December 1998
2. GK/RT0252 Minimum requirements for the bonding of track circuits, Issue 2, February 1996.
3. GK/RC0756 HVI Track Circuits, Issue 2, December 1998.
4. Signalling Installation Handbook, GS/IH0001, Issue 2, Railtrack S&SD, January 1994.
5. RT/SIN/067 Railtrack Line Special Instruction Notice 'HVI track circuits on a.c. electrified lines', Issue 2, December 1999.

2.2 Previous Safety Case Documentation

6. PRJ-SCSE(JUN)-RP-15 GEC Juniper Project Assessment of HVI Track Circuits Response to Transient Interference (AC and DC Routes), Issue 3, October 1999
7. SAO_REF-HVI-RP-02 Juniper Project Class 334 – HVI Track Circuit Response to Transient Waveforms, Issue 2, March 2000
8. “Class 92 Locomotive EMC Safety Assessment – Volume 9, HVI Track Circuits, Fleet Operation on the Route between Crewe and Doncaster”, AEA Technology ref. 120-dr0460, version b0, dated April 2000.

2.3 Other Documentation

9. High Voltage Impulse Track Circuit Receiver Sensitivity Tests, MTR 175, P. D. Booth, D. Poole, Alstom Signalling, June 1994.
10. Immunity of High Voltage Impulse Track circuits to Class 373 TMTS, MER181, D. Poole, J. Waller, Alstom Signalling, November 1993.
11. Fax from AEA Technology Rail to P. Hopkins, Railtrack, reference fx2276 dated 27th February 1997 (in support of the Class 92 locomotive EMC safety case)

2.4 Railtrack IDI Documentation

12. RT/E/C/50019 Guidance on Traction & Auxiliary Monitoring, To be issued.

3. INFRASTRUCTURE ASSUMPTIONS

The infrastructure assumed during the analysis is as described below, further assumptions are listed in Appendix B:

- The infrastructure is electrified using standard a.c., d.c. or dual electrification configurations.
- Track circuits are installed in single rail mode without the use of impedance bonds.
- Maximum length of HVI track circuit on d.c. and dual electrified infrastructure is 200m (ref. 3).
- Maximum length of HVI track circuit on a.c. electrified infrastructure is 300m (ref. 3).
- The external capacitor is ignored in this assessment.
- The rail impedance is modelled using a multifrequency track model validated in ref. 6.
- The HVI receiver is represented by a network component model to determine the rail to rail voltage at the receiver. This model is representative of the NCO.RVT.600 type. Type numbers for the equipment forming the HVI track circuit are listed in ref. 3.
- It is assumed that the HVI receiver is fitted with two BR933 slow to pick TPRs (Track Repeat Relays) or "extra delay" SSI data (ref. 3).

4. SUSCEPTIBILITY ANALYSIS

4.1 HVI Track Circuit Description

The Alstom HVI track circuit can be used for a.c. or d.c. electrified or non electrified lines, as a jointed track circuit. The track circuits are short in electrified areas, being up to 200 m in d.c. areas, up to 300 m in a.c. areas (ref. 3). They are therefore suitable in electrified areas where space to accommodate the tuned zone, required for jointless track circuits, is limited, such as points and crossings. They are also suitable for areas where there is poor electrical wheel/rail contact.

4.2 Operation of the HVI Track Circuit

The track circuit consists of a power supply, transmitter, receiver and track relay. The transmitter and receiver are coupled to the rail through transformers. Figure 1 shows the setup of HVI track circuit. This figure is reproduced from reference 3.

The wire from terminal C+ is a flying lead that is connected to one of the terminals numbered 1 to 6.

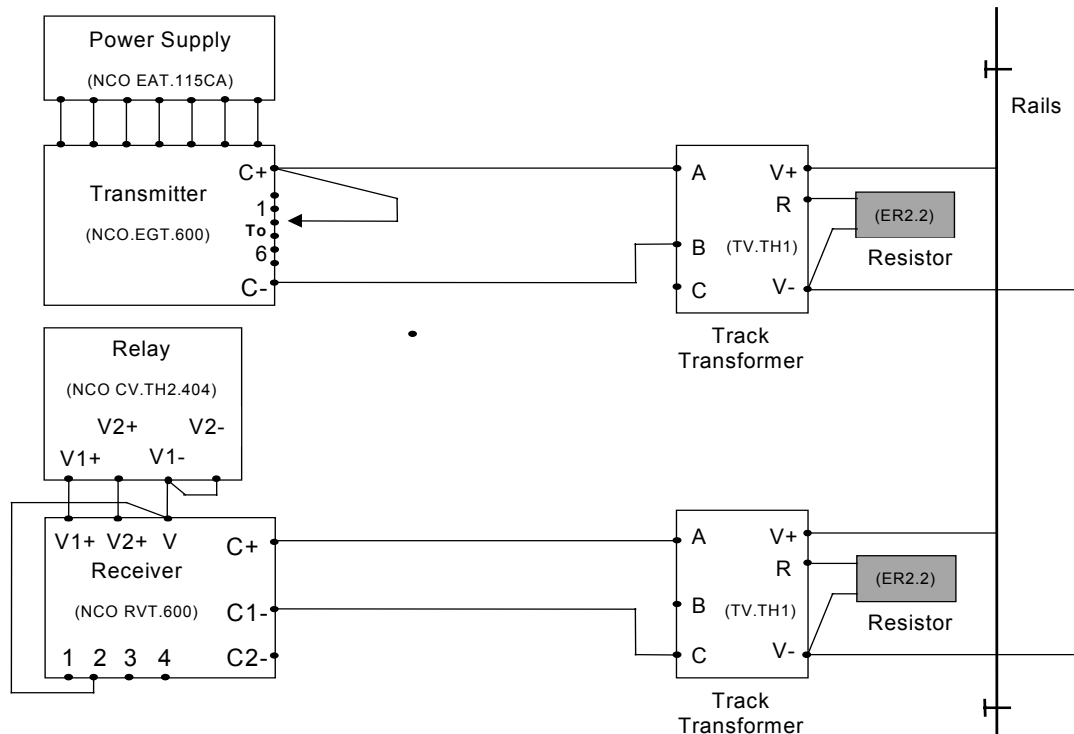


Figure 1: Setup of HVI track circuit on electrified lines

The track circuit operates by applying a short high voltage impulse to the rails, typically 100 V, three times per second. The operating pulse waveform is asymmetric with the ratio of the positive to negative voltage being 7:1. This waveform is generated by charging a capacitor to a high voltage and then discharging it through a thyristor and a track transformer. The inductance of the feed and relay end track transformers, together with that of the rails, causes the positive pulses to be followed by a negative undershoot. Figure 2 shows a typical feed end rail voltage waveform.

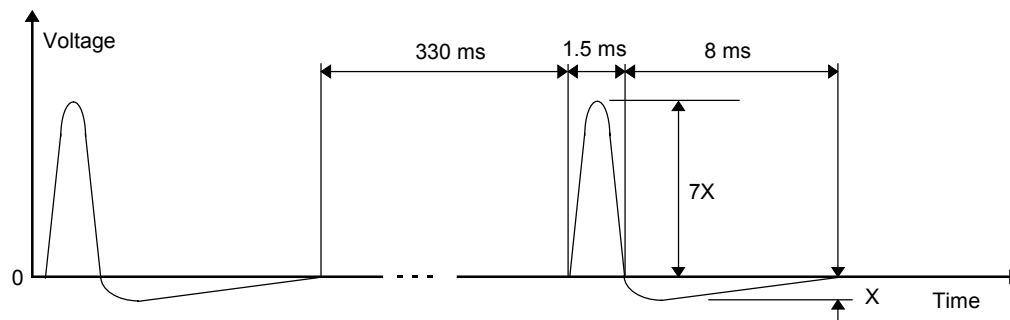


Figure 2: Typical transmitted HVI waveform

The nominal frequency of 3 pulses per second can vary and the track circuit will still work. However when the frequency is reduced to below 1 pulse per second the relay will pick momentarily and then drop (ref. 9).

At the receiver the energy from the track transformer is rectified and directly drives the track relay (see Figure 3). Therefore a power supply is not required at the relay end. The positive and negative parts of the waveform are rectified separately and applied to different windings on the relay. The flux in the centre limb of the detector cancels out when the positive and negative voltages are in the correct proportions. The flux then flows in the outer yoke picking the relay.

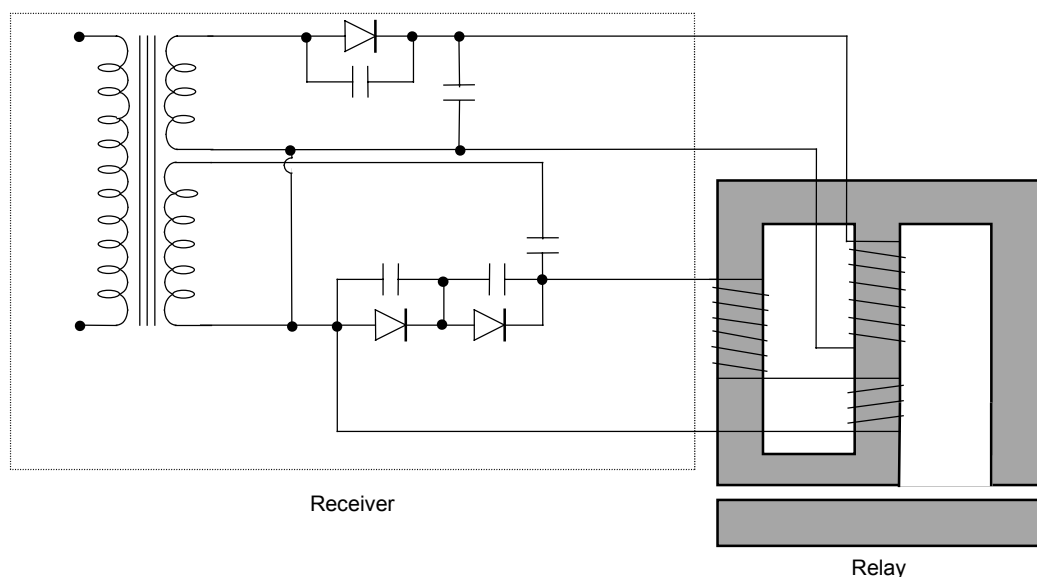


Figure 3: HVI receiver and relay