IECC Technical Handbook

IECC 6005

Issue 9

Date 16 February 2004

Board Configuration

For approval and authorisation of this document, please refer to the IECC Applications Manual Contents, RT/E/S/10040.

This document is the property of Network Rail. It shall not be reproduced in whole or in part, nor disclosed to a third party, without the written permission of the document owner.

Published and issued by
Network Rail
40 Melton Street
LONDON
NW1 2EE

ã **2004 Network Rail**

Documents
Document Sharing Hub

Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT

This page is intentionally blank

Documents
Document Sharing Hub

Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS

Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT

Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

Amendment Record

Issue	Date	Description
7	29/10/1999	Converted to Word format by AEA Technology Rail. Same as Issue 6.2.
7.1	01/11/1999	Sections 1, 2.1, 2.3, 4.1, 4.3, 4.3.1, 4.3.2 and 4.4 modified for MVME172 board. New section 2.3 added for MVME172 board configuration. New section 4.3.6 added for MVME172 board IndustryPack batteries. New sections 4.4.1 and 4.4.2 added for J1 and J2 backplanes. New section 4.5 added for fitting/removing IndustryPacks to/from MVME172 boards.
7.2	28/03/2000	Section 4.3 amended for battery replacement strategy and shelf life of RAM and Clock Device battery.
8	22/05/2001	Sections 1 and 5.1 amended and new section 4.6 added to cover the procedures for use of the CD-ROM facility.
8.1	10/09/2001	Section 2.2.2 real-time clock SET command amended. Section 2.3.1 amended to include setting of real-time clock. Section 2.3.4 amended to include environment settings for MVME172-213 and MVME172-Petra boards used in CD-ROM based subsystems. Section 4.6.1 amended to state that EPROMs containing the download program are the same for all MVME172 boards used in CD-ROM based subsystems, whereas EPROMs containing VME-bug differ.
9	16/02/2004	Amended to be applicable to all IECC-approved variants of the MVME172 board and with additional updates for rationalised drawing set as follows: Section 2.1 amended to refer to board configuration drawings in new Appendix A. References to IGS and RDF removed. Section 2.2.2 use of power save mode for board storage added. Section 2.3.2 created for MVME172 clock initialisation, subsequent sections renumbered. Use of power save mode for board storage added. Section 2.3.3 (new numbering) amended for setting up MVME172 board information block variables after RAM/Clock chip battery replacement. Section 2.3.5 (new numbering) amended for setting up MVME172-652SE board and stating that Debugger/BRX PROM is the same for all MVME172 variants. Section 3.2 amended to cover PSM, IPL and PIT. Section 4.1 renamed ‘Antistatic Precautions’ and amended to include dissipative desk mat.

Documents
Document Sharing Hub
Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

Section 4.3.1 amended to include CR2032 battery on MVME172-642LSE and MVME172-652SE boards, amended for SRAM battery connection in accordance with SAO-IEC-D22 and amended to include removal of J14 jumpers on stored boards.
Section 4.3.2 amended to include ‘Caphat’ and M4T28 ‘Snaphat’ devices.
Section 4.3.4 relating to MVME216 board removed.
Section 4.6.1 amended to include EPROM version 4.1 on MVME172-652SE boards.
Section 5.1 amended to refer to NDS board customisation drawing in new Appendix B.
Appendices A and B added with configuration drawings for MVME172 boards and customisation drawings for NDS board.
Overall- references to ‘Petra’ boards removed, ‘Industry Pack’ amended to ‘IndustryPack’, “NDS Connector Card” amended to “NDS Board” and ‘Railtrack’ amended to ‘Network Rail’.

Author	Approved	Date	Authorised	Date

Documents
Document Sharing Hub

Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

Contents

1 Introduction 1

2 VME Board Configuration Information 2

2.1 HARDWARE CONFIGURATION 2
2.2 MVME162 NON VOLATILE RAM CONFIGURATION 4
2.3 MVME172 NON VOLATILE RAM CONFIGURATION 10

3 PC Board Configuration Information 20

3.1 DIS 20
3.2 PSM, IPL AND PIT 20

4 Configuration And Handling Of Boards 21

4.1 ANTISTATIC PRECAUTIONS 21
4.2 INSERTION AND EXTRACTION OF RAM/EPROM/PROM DEVICES 21
4.3 BATTERY REPLACEMENT 22
4.4 VME BACKPLANES 24
4.5 FITTING AND REMOVAL OF MVME172 INDUSTRYPACKS 25
4.6 PROGRAM & DATA DOWNLOAD USING CD-ROM FACILITY 26

5 Computer Unit Identification 28

5.1 NDS BOARD 28
5.2 DIS PC 30

Appendices

APPENDIX A MVME172 BOARD CONFIGURATION DRAWINGS
APPENDIX B NDS BOARD CUSTOMISATION DRAWING

Documents
Document Sharing Hub
Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

Documents
Document Sharing Hub

Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT

1 Introduction

This document provides information on:

- the configuring of VME boards;
- the configuring of PC boards;
- the antistatic precautions to be taken when handling boards and components;
- the insertion and extraction of RAM/EPROM/PROM devices;
- the downloading of programs and data using the CD-ROM facility;
- the fitting and removal of IndustryPacks;
- the replacement of batteries; and
- computer unit identification.

All the boards used in the VME sub-racks and most of the boards used in the PCs can be configured. This allows certain parameters including bus addressing, interrupt priority, memory type and size, and interface connections to be defined. The non self-healing VME backplane can be configured to allow different board positioning and spacing.

In the drawing codes in the following sections:

XXXX is the IECC scheme reference;

YYY represents a standard subsystem abbreviation where the drawing is applicable to more than one subsystem; and

3NN is a number in the 300 series.

Documents
Document Sharing Hub
Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

2 VME Board Configuration Information

2.1 HARDWARE CONFIGURATION

For exact details of the configuration refer to the site specific hardware drawings.

MVME025 This board controls the bus arbitration. There is one MVME025 board per computer unit. All are configured the same. The configuration is detailed in:

- "MVME 025 Card (Arbiter) Customisation Drawing" IECC 5000-XXXX-YYY-300.

MVME101 There are six basic configurations for this board. Variations exist within these configurations depending on the number of RAM and EPROM chips used. The configurations are detailed in:

- "MVME 101 Card (NDS) Customisation Drawing" IECC 5000-XXXX-YYY-301;
- "MVME 101 Card (NCS/LTM) Customisation Drawing" IECC 5000-XXXX-YYY-302;
- "MVME 101 Card (I/O) Customisation Drawing" IECC 5000-XXXX-YYY-303;
- "MVME 101 Card (ISM) Customisation Drawing" IECC 5000-XXXX-ISM-304;
- "MVME 101 Card (NDS) Customisation Drawing" IECC 5000-XXXX-TTP-301;
- "MVME 101 Card (I/O) Customisation Drawing" IECC 5000-XXXX-DIS-306.

NB. Drawing number 301 for TTP (IECC 5000-XXXX-TTP-301) is not the same as drawing number 301 for the other subsystems (IECC 5000-XXXX-YYY-301).

MVME123 This board is the main application processor. The configuration is detailed in:

- "MVME 123 Card (Application CPU) Customisation Drawing" IECC 5000-XXXX-YYY-310.

MVME162 This board is the main application processor. There is one configuration for the variants of the board available (MVME162-001 and MVME162-010). The configuration is detailed in:

Documents
Document Sharing Hub
Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

- "MVME 162 Card (Application CPU) Customisation Drawing" IECC 5000-XXXX-YYY-368.

MVME172 This board is an embedded controller board. There are fifteen configurations for the MVME172 board; one 'M' board configuration and four 'C' board configurations for each of the IECC-approved MVME172 variants (MVME172-213, MVME172-642LSE and MVME172-652SE).

The 'M' board configurations are detailed in:

- AH/372/1, AH/372/2 and AH/372/3 (See Figures A1, A2 and A3 in Appendix A).

The 'C' board configurations (Dual PIT IndustryPack fitted) are detailed in:

- AH/373/1, AH/373/2 and AH/373/3 (See Figures A4, A5 and A6 in Appendix A).

The 'C' board configurations (No IndustryPack fitted) are detailed in:

- AH/374/1, AH/374/2 and AH/374/3 (See Figures A7, A8 and A9 in Appendix A).

The 'C' board configurations (NV-RAM IndustryPack fitted) are detailed in:

- AH/375/1, AH/375/2 and AH/375/3 (See Figures A10, A11 and A12 in Appendix A).

The 'C' board configurations (Two Quad-Serial IndustryPacks fitted) are detailed in:

- AH/376/1, AH/376/2 and AH/376/3 (See Figures A13, A14 and A15 in Appendix A).

MVME211 This memory board may be configured with RAM and EPROM chips. Each board is divided into two blocks with each block having an independent bus address and memory chip specification. There is a basic configuration for RAM and EPROM on the same board. Where a subsystem requires additional EPROM further MVME211 boards are configured with EPROM only. The RAM/EPROM board configuration is detailed in:

- "MVME 211 Card (RAM-EPROM) Customisation Drawing" IECC 5000-XXXX-YYY-311.

The EPROM-only configured boards are detailed in:

- "MVME 211 Card (EPROM-EPROM-A) Customisation Drawing" IECC 5000-XXXX-YYY-312;
- "MVME 211 Card (EPROM-EPROM-B) Customisation Drawing" IECC 5000-XXXX-YYY-313.

MVME215-3 This is the battery backed RAM memory board used by ARS, SIM and RII. The configuration is detailed in:

- "MVME 215-3 Card Customisation Drawing" IECC 5000-XXXX-YYY-320.

Documents
Document Sharing Hub
Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

MVME333-2 This is the intelligent communication controller board used by the ECS. The configuration is detailed in:

- "MVME 333 Card Customisation Drawing"
  IECC 5000-XXXX-ECS-330.

MVME705A This is the serial transceiver module board. There is one MVME705A board per MVME333-2 board in the ECS. The configuration is detailed in:

- "MVME 705A Card Customisation Drawing"
  IECC 5000-XXXX-ECS-340.

CMC130 This is the Ethernet controller board used by the Flexible Display Subsystem (DIS). It can be configured for "thicknet" or "thinnet". The configuration is detailed in:

- "CMC 130 Ethernet Card Configuration"
  IECC 5000-XXXX-DIS-307.

The Engineering Drawings IECC 5000 detail the position of EPROMs and IndustryPacks and give the positions of jumpers. The EPROM positions are marked by numbers preceded by 'U' or 'XU', the IndustryPacks are denoted by 'IP', and the jumper pin numbers are marked by numbers preceded by 'J' or 'K'.

2.2 MVME162 NON VOLATILE RAM CONFIGURATION

2.2.1 Set Up

Together with the hardware configuration as defined in section 2.1, the MVME162 requires the Non Volatile RAM configured to allow correct operation in an IECC environment. In order to configure the Non Volatile RAM, a standard terminal such as the ARS J102 terminal needs to be connected to the console port (the bottom 25-way D-type connector).

The MVME162 board to be configured should be placed in its usual place in the computer unit rack **with its jumpers set to the default settings**, *i.e.* as the board is delivered from the supplier. All other boards should be removed from the computer unit before power is applied. When power is applied, after approximately 5 seconds, the following appears on the terminal:

Copyright Motorola Inc. 1988-1993, All Rights Reserved

MVME162 Debugger/Diagnostics Release Version 2.1 - 10/19/93
COLD Start

Local Memory Found =00100000 (&1048576)

MPU Clock Speed =25MHz

162-Bug>

Note: The version must be 2.1 or later. Copies of the MVME162 debugger can be obtained from the supplier, Crellon Microsystems.

Documents
Document Sharing Hub
Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

Two versions of the MVME162 board are in use, the -001, which contains 1M byte RAM, and the -010 which contains 4M bytes of RAM. The 'Local Memory Found' (as described above) will change accordingly.

In the following sub-sections, commands entered by the user are shown in **bold**. Each command is terminated by pressing the ENTER or RETURN key.

2.2.2 Clock Initialisation and Power Save Mode

The on-board clock should be initialised first. The general format of the command to set the clock is **SET mmddyyhhmm**, where **mm**=month, **dd**=day, **yy**=year, **hh**=hour and **mm**=minutes. For example, to set the clock to 29th January 1993 at 1200 the following would be typed:

162-Bug>**SET 0129931200**

If the MVME162 board is subsequently removed for storage it is recommended that the real-time clock is put into power save mode to reduce the device battery drain. This is done by entering the following command when the board is in 162-Bug mode:

162-Bug>**PS**

2.2.3 Board Information Block

The board information block parameters for the MVME162 board must be set up in Non Volatile RAM using 162-Bug. At the prompt type:

162-Bug>**CNFG;M**

The board will respond with the following parameters for which appropriate entries should be input by the user (NB other characters may be output instead of the series of question marks):

Board (PWA) Serial Number = "????????????"? **<serial no>**
Board Identifier = "????????????????"? **MVME162-001** or **MVME162-010**
Artwork (PWA) Identifier = "????????????????"? **<artwork no>**
MPU Clock Speed = "????"? **2500**
Ethernet Address = "????????????"? **<ethernet addr>**
Local SCSI Identifier = "??"? **07**
Parity Memory Mezzanine Artwork (PWA) Identifier = "????????"? **.** (*i.e.* enter a full stop)

where: <serial no> is the serial number of the board which can be found on a label underneath a barcode on the reverse side of the board between the two edge connectors;

<artwork no> is the artwork number and revision which can be found under the serial number. The artwork number is printed on the board and the revision is printed on the paper tag;

<ethernet addr> is the Ethernet address and can be found on a label on the J2 (right hand) connector looking from the front of the board with the edge connectors uppermost.

After completion of the above, the board will respond with:

Documents
Document Sharing Hub
Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

Update Non Volatile RAM Y/N?

Answer:

Y

and the board will respond with:

162-Diag>

2.2.4 Self Test Configuration

Various self tests which are not appropriate to the MVME162 board when in an IECC environment must be removed from the Non Volatile RAM. At the prompt type:

162-Bug>**SD**

The board will respond with:

162-Diag>

At the prompt, type the following:

162-Diag>**MASK RTC RAM**

The board will respond with the question:

Update Non Volatile RAM Y/N?

Answer:

Y

The board will respond with:

162-Diag>

Repeat the sequence (from MASK ...) with the following, always remembering to respond to the question with Y between each occurrence:

MASK RTC ADR
MASK MCC TMR1C
MASK MCC TMR2C
MASK MCC TMR1D
MASK MCC TMR2D
MASK MCC TMR3D
MASK MCC TMR4D
MASK MCC ADJ
MASK MCC WDTMRA
MASK MCC WDTMRB
MASK DCAC DCAC_WT
MASK DCAC DCAC_CB
MASK VME2 REGB
MASK VME2 TMRA
MASK VME2 TMRB
MASK VME2 TMRC
MASK VME2 TRMD
MASK VME2 TMRE

Documents
Document Sharing Hub
Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

MASK VME2 TMRF
MASK VME2 TMRG
MASK VME2 TMRH
MASK VME2 TMRI
MASK VME2 TRMJ
MASK VME2 TMRK
MASK MMU INVPAGE
MASK MMU MAPROM
MASK MMU MODPAGE
MASK MMU RP
MASK MMU TC
MASK MMU USEDPAGE
MASK MMU WALK
MASK MMU WPPAGE

2.2.5 Setting Environment Variables

The correct environment must be set up for the MVME162 board to function correctly within an IECC subsystem. At the prompt type:

162-Diag>**SD**

The board will respond with:

162-Bug>

At the prompt type:

162-Bug>**ENV**

The board will respond with a series of questions that require to be answered as follows:

Bug or System environment = **B**
Field Service Menu Enable = **N**
Remote Start Method Switch = **B**
Probe System for Supported I/O Controllers = **N**
Negate VMEbus SYSFAIL* Always = **N**
Local SCSI Bus Reset on Debugger Startup = **N**
Local SCSI Bus Negotiations Type = **A**
IndustryPack Reset on Debugger Restart = **Y**
Ignore CFGA Block on Hard Disk Boot = **Y**
Auto Boot Enable = **N**
Auto Boot at Power-Up Only = **Y**
Auto Boot Controller LUN = **00**
Auto Boot Device LUN = **00**
Auto Boot Abort Delay = **00**
Auto Boot Default String = (‘Return’ or ‘Enter’ only)
ROM Boot Enable = **Y**
ROM Boot at Power-Up Only = **N**
ROM Boot Enable Search of VMEbus = **N**
ROM Boot Abort Delay = **00**
ROM Boot Direct Starting Address = **FF870000**

Documents
Document Sharing Hub
Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

ROM Boot Direct Ending Address = **FF87FFFC**
Network Auto Boot Enable = **N**
Network Auto Boot at Power-Up Only = **Y**
Network Auto Boot Controller LUN = **00**
Network Auto Boot Device LUN = **00**
Network Auto Boot Abort Delay = **00**
Network Auto Boot Configuration Parameters Pointer = **00000000**
Memory Search Starting Address = **FFE00000**
Memory Search Ending Address = **FFE00000**
Memory Search Increment Size = **00010000**
Memory Search Delay Enable = **N**
Memory Search Delay Address = **FFFFD20F**
Memory Size Enable = **Y**
Memory Size Starting Address = **10000000**
Memory Size Ending Address = **10080000**
Base Address for Dynamic RAM = **10000000**
Size of Parity Memory = **00100000** (for -001 board) or **00400000** (for -010 board)
Size of ECC Memory Board #0 = **00000000**
Size of ECC Memory Board #1 = **00000000**
Base address for Static Memory = **FFE00000**
Size of Static Memory = **00020000**
Slave Enable #1 = **N**
Slave Starting Address #1 = **00000000**
Slave Ending Address #1 = **00000000**
Slave Address Translation Address #1 = **00000000**
Slave Address Translation Select #1 = **00000000**
Slave Control #1 = **0000**
Slave Enable #2 = **N**
Slave Starting Address #2 = **00000000**
Slave Ending Address #2 = **00000000**
Slave Address Translation Address #2 = **00000000**
Slave Address Translation Select #2 = **00000000**
Slave Control #2 = **0000**
Master Enable #1 = **N**
Master Starting Address #1 = **00000000**
Master Ending Address #1 = **00000000**
Master Control #1 = **00**
Master Enable #2 = **N**
Master Starting Address #2 = **00000000**
Master Ending Address #2 = **00000000**
Master Control #2 = **00**
Master Enable #3 = **N**
Master Starting Address #3 = **00000000**
Master Ending Address #3 = **00000000**
Master Control #3 = **00**
Master Enable #4 = **N**

Documents
Document Sharing Hub
Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

Master Starting Address #4 = **00000000**
Master Ending Address #4 = **00000000**
Master Address Translation Address #4 = **00000000**
Master Address Translation Select #4 = **00000000**
Master Control #4 = **00**
Short I/O (VMEbus A16) Enable = **N**
Short I/O (VMEbus A16) Control = **00**
F-Page (VMEbus A24) Enable = **N**
F-Page (VMEbus A24) Control = **00**
ROM Access Time = **03**
FLASH Access Time = **02**
MCC Vector Base = **05**
VMEC2 Vector Base #1 = **06**
VMEC2 Vector Base #2 = **07**
VMEC2 GCSR Group Base Address = **D2**
VMEC2 GCSR Board Base Address = **00**
VMEbus Global Time Out Code = **01**
Local Bus Time Out Code = **02**
VMEbus Access Time Out Code = **02**
IP A Base Address = **01000000**
IP B Base Address = **01800000**
IP C Base Address = **02000000**
IP D Base Address = **02800000**
IP D/C/B/A Memory Size = **7F7F7F7F**
IP D/C/B/A General Control = **34343434**
IP D/C/B/A Interrupt 0 Control = **12121212**
IP D/C/B/A Interrupt 1 Control = **12121212**

After completion of the above, the board will respond with:

Update Non Volatile RAM Y/N?

Answer:

Y

The board will respond with:

Reset Local System (CPU) Y/N?

Answer:

Y

The board will then re-boot and when complete the normal prompt will be shown. This will take approximately 10 seconds. The power should then be switched off, the board removed and the jumpers configured as defined in the Customisation Drawing identified in section 2.1 above. Remember also to insert the MVME162 Debugger/BRX PROM in socket U47 before use.

Documents
Document Sharing Hub
Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

2.3 MVME172 NON VOLATILE RAM CONFIGURATION

2.3.1 Set Up

Together with the hardware configuration as defined in section 2.1, the MVME172 requires the Non Volatile RAM configured to allow correct operation in an IECC environment. In order to configure the Non Volatile RAM, a standard terminal such as the ARS J102 terminal needs to be connected to the console port (Port 1, *i.e.* the top RJ45 connector on the front panel).

The MVME172 board to be configured should be placed in its usual place in the computer unit rack with its jumpers set as shown in the drawings. All other boards should be removed from the computer unit before power is applied. Power should be applied, and the 'ABORT' button on the MVME172 board should be pressed. The following prompt will be shown:

172-Bug>

In the following sub-sections, commands entered by the user are shown in **bold**. Each command is terminated by pressing the ENTER or RETURN key.

2.3.2 Clock Initialisation and Power Save Mode

If the MVME172 board is to be used in a subsystem with CD-ROM Facility (see section 4.6), then the real-time clock should be enabled by entering the current date and time.

The general format of the command to set the clock is **SET mmddyyhhmm**, where **mm**=month, **dd**=day, **yy**=year, **hh**=hour and **mm**=minutes. For example, to set the clock to 29th January 1993 at 1200 the following would be typed:

172-Bug>**SET 0129931200**

If the MVME172 board is subsequently removed for storage it is recommended that the real-time clock is put into power save mode to reduce the device battery drain. This is done by entering the following command when the board is in 172-Bug mode:

172-Bug>**PS**

2.3.3 Board Information Block

The board information block parameters for the MVME172 board must be set up in Non-Volatile RAM using 172-Bug if the RAM and Clock chip battery is replaced. At the prompt type:

172-Bug>**CNFG;M**

The board will respond with the following parameters for which appropriate entries should be input by the user (NB other characters may be output instead of the series of question marks):

WARNING: Board Information Block Checksum Error
Board (PWA) Serial Number = “????????????”? **<serial no>**
Board Identifier = “????????????????”? **<board type>**
Artwork (PWA) Identifier = “????????????????”? <**artwork no**>
MPU Clock Speed = “????”? **<mpu clock>**
Ethernet Address = 000000000000? **<ethernet addr>**
Local SCSI Identifier = “??”? **07**

Documents
Document Sharing Hub
Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

Parity Memory Mezzanine Artwork (PWA) Identifier = "????????"? **.** (*i.e.* enter a full stop)

where: <serial no> is the board serial number which can be found below the barcode on a label on the reverse side of the board between the two edge connectors, for example 6013875;

<board type> is the board type, for example MVME172PA-642LSE;

<mpu clock> is 6000 for the MVME172PA-652SE board or 6400 for all other MVME172 boards;

<artwork no> is the artwork number and revision which can be found below the serial number. The artwork number is printed on the board and the revision is printed on the paper tag, for example 01-W3627F12B where 01-W3627F is the artwork number and 12B is the revision;

<ethernet addr> is the Ethernet address which can be found below the barcode on a label on the reverse side of the board, for example 0001AF097642.

After completion of the above, the board will respond with:

Update Non Volatile RAM Y/N?

Answer:

Y

and the board will respond with:

172-Bug>

2.3.4 Self Test Configuration

There is no requirement to set up the self test configuration of MVME172 boards via the 172-Bug environment, as this is set up by a configuration program.

2.3.5 Setting Environment Variables

The environment variables must be set up for the MVME172 board to function correctly within an IECC subsystem. At the prompt type:

172-Bug>**ENV**

The board will respond with a series of parameters which should be set up as shown below. These parameters differ according to whether the board is to be used in an EPROM-based subsystem or in a subsystem with CD-ROM Facility (see section 4.6). The latter also has two settings, one for MVME172-213 boards and the other for MVME172-642LSE and MVME172-652SE boards.

The environment settings for the three applications are as follows:

(a) MVME172 Board (All Variants) for use in EPROM-Based Subsystems

Bug or System environment = **B**
Field Service Menu Enable = **N**
Remote Start Method Switch = **B**

Documents
Document Sharing Hub
Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

Probe System for Supported I/O Controllers = **Y**
Negate VMEbus SYSFAIL* Always = **N**
Local SCSI Bus Reset on Debugger Startup = **N**
Local SCSI Bus Negotiations Type = **A**
IndustryPack Reset on Debugger Restart = **Y**
Ignore CFGA Block on Hard Disk Boot = **Y**
Auto Boot Enable = **N**
Auto Boot at Power-Up Only = Don't Care
Auto Boot Controller LUN = Don't Care
Auto Boot Device LUN = Don't Care
Auto Boot Abort Delay = Don't Care
Auto Boot Default String = Don't Care
ROM Boot Enable = **Y**
ROM Boot at Power-Up Only = **N**
ROM Boot Enable Search of VMEbus = **N**
ROM Boot Abort Delay = **00**
ROM Boot Direct Starting Address = **FF880000**
ROM Boot Direct Ending Address = **FF88FFFC**
Network Auto Boot Enable = **N**
Network Auto Boot at Power-Up Only = Don't Care
Network Auto Boot Controller LUN = Don't Care
Network Auto Boot Device LUN = Don't Care
Network Auto Boot Abort Delay = Don't Care
Network Auto Boot Configuration Parameters Pointer = Don't Care
Memory Search Starting Address = **FFE00000**
Memory Search Ending Address = **FFE00000**
Memory Search Increment Size = **00100000**
Memory Search Delay Enable = **N**
Memory Search Delay Address = **FFFFD20F**
Memory Size Enable = **Y**
Memory Size Starting Address = **10000000**
Memory Size Ending Address = **100C0000**
Base Address for Dynamic RAM = **10000000**
Size of Parity Memory = **00400000**
Size of ECC Memory Board #0 = **00000000**
Size of ECC Memory Board #1 = **00000000**
Base address for Static Memory = **FFE00000**
Size of Static Memory = **00020000**
Slave Enable #1 = **N**
Slave Starting Address #1 = **00000000**
Slave Ending Address #1 = **00000000**
Slave Address Translation Address #1 = **00000000**
Slave Address Translation Select #1 = **00000000**
Slave Control #1 = **0000**
Slave Enable #2 = **N**
Slave Starting Address #2 = **00000000**
Slave Ending Address #2 = **00000000**

Documents
Document Sharing Hub
Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004

Slave Address Translation Address #2 = **00000000**
Slave Address Translation Select #2 = **00000000**
Slave Control #2 = **0000**
Master Enable #1 = **N**
Master Starting Address #1 = **00000000**
Master Ending Address #1 = **00000000**
Master Control #1 = **00**
Master Enable #2 = **N**
Master Starting Address #2 = **00000000**
Master Ending Address #2 = **00000000**
Master Control #2 = **00**
Master Enable #3 = **N**
Master Starting Address #3 = **00000000**
Master Ending Address #3 = **00000000**
Master Control #3 = **00**
Master Enable #4 = **N**
Master Starting Address #4 = **00000000**
Master Ending Address #4 = **00000000**
Master Address Translation Address #4 = **00000000**
Master Address Translation Select #4 = **00000000**
Master Control #4 = **00**
Short I/O (VMEbus A16) Enable = **N**
Short I/O (VMEbus A16) Control = **00**
F-Page (VMEbus A24) Enable = **N**
F-Page (VMEbus A24) Control = **00**
ROM Access Time = **03**
FLASH Access Time = **02**
MCC Vector Base = **05**
VMEC2 Vector Base #1 = **06**
VMEC2 Vector Base #2 = **07**
VMEC2 GCSR Group Base Address = **D2**
VMEC2 GCSR Board Base Address = **00**
VMEbus Global Time Out Code = **01**
Local Bus Time Out Code = **02**
VMEbus Access Time Out Code = **02**

Documents
Document Sharing Hub
Copyright Network Rail
Provided by IHS under license with Network Rail
No reproduction or networking permitted without license from IHS
Licensee=Weston Williamson/5989497001, User=sam, albett
Not for Resale, 03/28/2016 01:18:14 MDT
Full document details: NR SAO-IEC-HT-20 ISSUE 9 2004