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Module

Chapter B: Introductory Information

For endorsement, authorisation and issue record of this document, please refer to the SSI Applications Manual Contents, NR/L2/SIG/17002.

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User information

This Network Rail standard may contain requirements that are colour-coded according to the following Red–Amber–Green classification.

Red – Mandatory requirements

- **Requirements** that **will** be complied with, and achieved under all circumstances.
- Accountability for the efficacy of these requirements lies with the Professional Head/Standard Owner.
- These requirements are monitored for compliance.
- Local non-compliances, discovered through engineering verification visits, will be reported and monitored through the quarterly Engineering Verification Report.
- Corrective actions will be enforced where local non-compliances remain open beyond the agreed mitigation plan dates.
- These are presented in a red box **and with the word “shall” or a direct instruction.**

Amber – Conditional requirements

- **Requirements** that **will** be complied with unless deviation has been approved.
- Accountability for the efficacy of these requirements lies with the Professional Head/ Standard Owner, or their nominated Delegated Authority.
- These requirements are monitored for compliance.
- Derogations **may** be permitted; which are to be approved by Standard Owner in advance.
- Derogations and Temporary Non-Compliances **may** be granted through the existing Delegated Authority arrangements.
- These are presented with an amber sidebar **and with the word “shall” or a direct instruction.**

Green – Guidance

- Guidance based on good practice; representing supporting information, based on good practice, to help achieve **RED** and **AMBER** requirements.
- This guidance is **not mandatory** and is not monitored for compliance.
- Alternative solutions may be used, which do not need to be formally approved.
- Decisions made by a competent person to use alternative solutions should be backed up by appropriate evidence/documentation.
- This is presented with a dotted green sidebar **and with the word “should” (usually in notes).**

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Issue record

Issue	Date	Comments
2	Feb 2002	2nd Issue
3	04/12/2010	3 rd Issue
4	03/03/2012	4 th Issue

Compliance

This Network Rail standard is mandatory and shall be complied with by Network Rail and its contractors if applicable from 03/03/2012.

When this standard is implemented, it is permissible for all projects that have formally completed GRIP Stage 3 (Option Selection) to continue to comply with the issue of any relevant Network Rail standards current when GRIP Stage 3 was completed and not to comply with requirements contained herein, unless stipulated otherwise in the scope of this standard.

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1 Introduction

One of the basic design objectives of the Solid State Interlocking Project was to create a system which would not require the signal engineer to use computer programming techniques in order to define the Interlocking logic. This has been achieved by the provision of an Interlocking program which remains the same for any application. The logic required for any particular signalling area is provided to the program in the form of tables of data which are held in the Interlocking Processor's memory.

The objectives of this document are to show how the data and program work together to carry out the Interlocking function and how data may be prepared in order to achieve particular requirements. It is assumed that a scheme plan has been obtained and that the allocation of Trackside Functional Modules has been made. The data examples in the main body of this document have been limited for ease of understanding. Details of data preparation for some of the more complex and unusual situations are included in a series of Supplements which will be updated and added to as experience in the application of SSI develops.

2 The Structure of an SSI Central Interlocking

Refer to Figure B1.

An SSI Central Interlocking consists of a number of Processors. The Communications Processors in the Multiprocessor Modules (MPMs) are solely concerned with the operation of the Trackside Data Links (which connect the Central Interlocking to the Trackside Functional Modules (TFMs)) and the Internal Data Links (which connect together a number of Central Interlocking Systems within a Control Centre).

The information transmitted from the Central Interlocking over the Trackside Data Links is a series of command telegrams addressed to each of the potential 62 TFMs (i.e. Signal Modules and Points Modules) in sequence (Address 0 is used for diagnostic purposes, and address 63 shall not be used because of a known program problem). When a TFM receives a telegram addressed to itself, it responds with a reply telegram back to the Central Interlocking. Trackside Data Link command and reply telegrams each contain eight data bits and five status bits which are used to convey information (see Figure B2).

The process of transmitting one command telegram and receiving the corresponding reply telegram takes place at a minimum interval of 9.5 ms, which is referred to as an "Interlocking minor cycle". Over a series of 64 minor cycles the Central Interlocking will have communicated with all 62 (potential) TFMs (the use of address 63 is not permitted) and its Diagnostic Processor (the Main Processor in the Diagnostics MPM), which is addressed as if it were a 64th Trackside Functional Module; this "major cycle" of 608 ms minimum defines the frequency at which the trackside equipment receives fresh commands from the Central Interlocking, and the Central Interlocking receives updates of inputs from the trackside. Minimum minor and major cycle times are increased to 12.85 and 822ms respectively if a Long Line Link is employed.

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The Internal Data Link which links together a number of Central Interlockings within a Control Centre works on a different basis. Each Central Interlocking takes it in turn to transmit a message containing 120 data bits, and the other Central Interlockings pick out of each transmission required data. The message is composed of 15 eight bit telegrams, and to ease the data preparation task, these are referred to as output telegrams 64-78 in the same number series as the Trackside Data Link output telegrams.

The Internal Data Link input telegrams are also numbered in the 64-78 series, but unlike the Trackside Data Link there is no relationship with the output telegram of the same number. Instead it is necessary to specify which Central Interlocking's message, and from which output telegram in the message, the data for the input telegram is to be extracted.

The frequency at which each Central Interlocking transmits over the Internal Data Links is determined by the number of Central Interlockings in the Control Centre (up to a maximum of 30), but will be at least once per major cycle. Each Internal Data Link telegram can be used either as 8 individual bits conveying separate functions, or as an 8 bit code which is treated as a binary number in the range 0-255. The second method is used to pass route requests between Central Interlockings (see [SSI8003-51](#): Communication with Other Interlocking Areas).

The two Panel Processors (one located within each of the two Panel Processor Modules) exchange data between the Interlocking Processors and the panel and other equipment such as Train Describers or an Integrated Electronic Control Centre (IECC).

The Diagnostic Processor monitors system operation and feeds information on faults to the Technician's Terminal. The Technician's Terminal can also communicate with the Interlocking Processors (the Main Processors in the three Interlocking MPMs) via the Panel Processors; this gives the Technician access to certain areas of the Interlocking memory which allows him to bar routes, prevent signals clearing and points moving, falsely occupy track circuits, and enforce temporary approach control conditions.

It is not necessary to consider these Processors further in the context of preparation of Interlocking data (as far as data is concerned, the three Interlocking Processors are henceforth collectively referred to as the "Interlocking"). The Panel Processor and Diagnostic Processor each contain their own geographic data, but these are dealt with in separate documents. [SSI8003-20](#) and [SSI8003-30](#) respectively.

The program within each Interlocking Processor can be divided into four parts. The first part, known as the initialisation program, controls the start up actions of the Processor at power up (see Section 3.7). The second part, known as the redundancy management program, looks after the safety of the system. The third part, known as the interface program, is responsible for interfacing the Interlocking Processor with the Communications Processors and the Panel Processors. The fourth part is the functional program, and it is this part which operates on the data to produce the required Interlocking function.

Because the hardware safety of the system is dealt with by the redundancy management program, and because one of the tasks of the interface program is to check that the functional program in each Interlocking Processor receives the same

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data from its external interfaces, it is possible to consider the functional program in isolation.

3 The Interlocking Processor

It is not necessary to understand the working of the Processor in any detail in order to be able to prepare data. Nevertheless, some knowledge of the way in which information is stored in each Interlocking Processor does help to give an insight into the way in which the program and data structure combine to produce the Interlocking function.

The Interlocking Processor is based upon the Motorola 6802 CPU. This has an 8-bit data bus and a 16-bit address bus. This means that it can address 65,536 locations, each of which contains 8 bits. These are generally referred to as bytes, and the number 65,536 is usually called "64K", where 1K = 1024. These 64K locations are divided up as follows.

60K is taken up by EPROM chips (EPROM stands for Erasable Programmable Read Only Memory, and it is these devices which hold the program and data). All the programs (initialisation, redundancy management, interface and functional) fit into about 20K, leaving the remaining 40K for data. An "extended" version of memory (achieved through paging techniques) is available; where this is used the 20K program area is increased to 32K, and the data area is increased to 60K and split into four overlapping "pages", of which only page 0 and one of pages 1, 2 or 3 (=28K) are addressed at any one time. Further information on this and on data volume limitations is given in [SSI8003-52](#).

Of the 4K not used by EPROMs, 2K is taken up by RAM while the remainder is largely used for input and output devices.

RAM stands for Random Access Memory and this is a read/write memory chip which is used to store information during the operation of the program. One of its most important functions is to store the current state of the railway. Each bit in the RAM has two states known as "one" and "zero"; a bit is said to be "set" to one and "cleared" to zero (the use of the word "clear" should not be confused with, say, the clearance of a signal as a bit in the clear state is generally associated with a restrictive condition).

The RAM is capacitor backed, thus the bit-state is retained for at least six hours in the event of a power supply failure (see Section 3.7).

Figure B3 shows the arrangement of RAM memory (note that the addresses are given in hexadecimal).

3.1 Signal Memory

The first part of RAM is taken up with signal memories, and a maximum of 128 signals can be accommodated. Each signal memory consists of three bytes, each byte containing eight bits.

The function of the bits in the first byte is as follows: