

# Chapter B: Introductory Information

## 1 Introduction

Each SSI Central Interlocking is equipped with two Panel Processors Modules. These modules each have a single processor, the "Panel Processor". The function of the Panel Processors in an SSI Central Interlocking is to provide an interface with the Panel Multiplex system which drives the indications on the Signaller's Panel and detects operation of push buttons and switches, and with Train Descriptor equipment. The Panel Processors are not part of the safety system and duplication is provided to achieve high availability. As with the Interlocking Processors themselves, the program in the Panel Processors is identical for all Panel applications, and the logic required to control the Panel indications and interpret push button and switch operations is stored in the processors' memory as tables of geographic data which are interpreted by the program.

See SSI8003-53 for the Panel Processor data requirements for Central Interlockings controlled by Integrated Electronic Control Centre (IECC) systems.

The purpose of this document is to describe the function of the geographic data and how to prepare it. A fundamental object of the SSI project has been that the task of data preparation should not require staff with experience of computer programming or of the actual software in the SSI Processors. Many of the features of the data are identical to those in the Interlocking Processor, which have been described in SSI8003-10, and these will not be repeated in this document, except to explain how they are applied in the Panel Processor.

## 2 The Panel Processor Structure

The Panel Processor is a Motorola MC6802 CPU with up to 32K byte of Read Only Memory (ROM) and 2K byte of Random Access Memory (RAM). It has serial input/output interfaces to the three Interlocking Processors, the Panel Multiplex, the Technician's Terminal and the Train Descriptor.

### 2.1 ROM Memory

The Panel Processor is equipped with up to 32K bytes of EPROM (Erasable Programmable Read Only Memory) chips. Of this, 12K bytes are used for the fixed program, leaving up to 20K bytes available for geographic data.

### 2.2 RAM Memory

The RAM memory is a read/write memory which is used to store information during the operation of the program. The arrangement of RAM memory is listed in Figure B1. The general purpose areas in the RAM are used by the

program for temporary storage as it carries out its calculations, and like the program ROM need not be considered in this document, but the remaining areas are used to describe the current state of the railway and of the Signaller's Panel, and it is these that are tested and modified by the program according to the rules defined in the geographic data.

### 2.2.1 State of the Railway

The Panel Processor gets its information about the current state of the railway by copying across areas of the Interlocking Memory. Each location in these parts of the Panel Processor is updated once in every Interlocking major cycle of approximately 0.6 to 1.0s. To reduce the amount of data to be transferred, only parts of the Interlocking Memory are copied, so the Panel Processor contains a sub-set of the information in the Interlocking. The information in the Interlocking RAM is described fully in SSI8003-10. The parts of the RAM contents which are copied into the Panel Processor are as follows:

**Signal Memory:** One byte of memory for each of the 128 signals which can be accommodated. This is a copy of the second of the three bytes allocated to each signal in the Interlocking Memory. The byte contains bits indicating lamp proved, auto mode set, free of approach locking, aspect control, button pulled, and a three bit code indicating the aspect. The allocation of these bits is listed in Figure B1.

**Points Memory:** One byte of memory for each of 64 points. This is a complete copy of the Interlocking Points Memory.

**Route Memory:** Two bits of memory for each of 256 routes, 64 bytes in all. This is a complete copy of the Interlocking Route Memory.

**Track Circuit Memory:** Two bits of memory for each of 256 track circuits, 64 bytes in all. The two bits indicate track circuit clear and Technician's control, and are a copy of the two most significant bits in the first of the two bytes allocated to each track circuit in the Interlocking Track Circuit Memory. Both bits must be set for the Panel Processor to interpret the track circuit as clear. Note that the "track circuit occupied" bit in the Interlocking is not copied across. This means that the Panel Processor treats a track circuit in the "undefined" state as if it were occupied (see SSI8003-10 for an explanation of the meaning of the "undefined" state).

**Flag Memory:** One bit of memory for each of 1024 flags, 128 bytes in all. Flags are used to represent sub-routes, sub-overlaps or general purpose latches. This is a complete copy of the Interlocking Flag Memory.

For each type of identity memory, the updating of the Panel Processor RAM by the Interlocking commences at identity zero at the beginning of

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minor cycle zero before any data is processed. Either two bytes (signal and flag identities) or one byte (other identities) of memory updated at the beginning of each of the 64 minor cycles. Thus, for example, the track circuits with identity numbers 0 to 3 are updated at the beginning of minor cycle 0, 4 to 7 at the beginning of minor cycle 1, etc.

It should be noted that the Panel Processor does not receive any information relating to any of the Interlocking Timer Memories, either the general purpose elapsed timers or the special timers associated with each track circuit and signal.

The data is transferred from the interlocking over a dedicated serial link at 250 kbaud, least significant bit first. These serial links are not accessible for on site diagnostic purposes, and specialised equipment is required to analyse the data being carried by them.

When monitoring items of panel processor memory on the Technician's Terminal, it is necessary to refer to an identity listing for the interlocking, produced by a SSI Design Workstation, to find the number of the identity required. A single identity from panel processor memory may be monitored at a time. For signal and points memory the appropriate byte (8 bits) is displayed, for routes and track circuits two bits are displayed, and for flags the single bit is shown. Details of the meanings of bits displayed are given in Figure B1. It should be noted that the TT screen displays the most significant (highest numbered) bit on the left and the least significant (lowest numbered, usually 0) on the right of the bits shown. Further information on operation of the TT is available in Technical manuals M1303/7 Technician's Terminal Technical Manual, or SSI8002: Technician's Terminal User Guide.

### 2.2.2 Input Image

The Input Image contains a copy of the information received in the last valid message from the Panel Multiplex, describing the state of the switch contacts in the Panel. One bit is allocated for each of up to 256 contacts, each bit being set to '1' when the corresponding contact is in the closed position and cleared to '0' when the contact is in the open position.

The Input Image is used in two distinct ways. Firstly, any bit can be tested to determine its current state; this is mainly used to check points key detection (see Chapter C, Section 4.3.1) but can also be used for other purposes. Secondly, whenever a new message is received from the Panel Multiplex, each bit in the message is compared with the corresponding bit in the Input Image before this is over-written with the new information, and if the bit has changed state in the "active" direction (normally '0' to '1', but see Section 4.2 below), the corresponding bit is set in a separate memory area known as the "Active Input Image". A bit

set in the Active Input Image indicates that the Signaller has operated a button or switch which may indicate a requirement to send a panel request code to the Interlocking (see Chapter C, Section 5).

### 2.2.3 Output Image

The Output Image contains the information which is sent to the Panel Multiplex to control the indications on the Panel. These indications are either flashable or non-flashable. Non-flashable indications are grouped at the start of the Output Image and are allocated one bit each; if the bit is set the indication is illuminated. Flashable indications are allocated two bits each and follow on in memory after the last non-flashable indication; the two bits are interpreted as a code to mean "extinguished", "illuminated-flashing", or "illuminated-steady". The allocation of the flashable and non-flashable areas of memory are carried out by the data compiler (see Section 4.3 below). The total Output Image contains 192 bytes, giving space for 1536 non-flashable or 768 flashable outputs, or appropriate combinations of the two.

### 2.2.4 Start-up Conditions

At power up of the Panel Processor Module all bits in the State of the Railway memory are initially set to zero and are then updated within the first major cycle by the Interlocking (see Section 2.2.1). All bits in the Input Image are also set to zero initially and are then updated by the first valid message received from the Panel Multiplex. Similarly, all bits in the Output Image are set to zero initially, these being updated accordingly as the Panel Processor data is processed.

## 2.3 Input/Output Interfaces

The Panel Processor has serial interfaces for data transfer to and from the three Interlocking Processors in the same Central Interlocking, the Technician's Terminal and the Panel Multiplex, and to the Train Describer. Communication within the Central Interlocking is independent of the geographic data and need not be considered in this document. The data required to set up the other communication links is discussed below.

### 2.3.1 Technician's Terminal

The purpose of the Technician's Terminal link is to allow commands from the terminal to be passed on by the Panel Processor to the Interlocking Processors, and the only data required in the Panel Processor is the Interlocking Identity number which is used to distinguish between a number of Central Interlockings connected to one Technician's Terminal in a Control Centre.

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This number is defined as part of the geographic data (see Section 4.1); the rules for allocation of identity numbers are described in SSI8003-10C, Section 2.

### 2.3.2 Panel Multiplex

A Panel Multiplex System is required to convert the serial data stream transmitted from the Panel Processor into the drives to individual lamps or LEDS on a conventional Signaller's Panel, and to sample the state of all the Panel switch contacts on a regular basis and make-up a serial stream for transmission back to the Panel Processor. In each case the message corresponds to the contents of the corresponding memory area in the Panel Processor, with each byte converted into serial form and transmitted in address order. The messages also contain control characters which define the start and end of the message and a status byte which is used to monitor the correct operation of the Panel Multiplex, but these can be ignored from the point of view of data preparation. A further control character is used to identify the delineation between information for non-flashable and flashable indications. The detailed requirements for a Panel Multiplex System used in conjunction with an SSI signalling scheme are contained in BR Specification 1921A.

### 2.3.3 Train Descriptor

A separate serial data output is provided to feed information from the Panel Processor to a Train Descriptor. The messages transmitted have a similar pattern to those sent to the Panel Multiplex, but instead of being a direct copy of one memory area in the Panel Processor, the contents of the message are assembled from various parts of the "state of the railway" memory according to a standard set of rules. Each byte in the message contains information regarding a group of eight signals, routes, track circuits and flags; a bit in the '1' state indicating "signal off", "route set", "track circuit not clear" and "flag bit set" respectively. Note that, so long as the fitted PPM program is issue SSI4302-E4 or later, then "track circuit not clear" includes a test for the application of the Technician's control to the track circuit, thus permitting this control to be used in the testing of the Train Descriptor.

The message commences with the information relating to signals followed in order by the routes, track circuits and finally flags. The bytes within each group are transmitted in order of memory address, e.g. the first byte in the message relates to the first eight signal memories, and so to the first eight signals defined in the SIG identity file (see Section 4.1 below). Within each byte however, the bits are allocated in reverse order, e.g. the first signal identity relates to bit 7 of the first message byte. This is the opposite of the relationship between the Panel Multiplex message bytes and the Input and Output Images described above.

The message is limited to the minimum number of bytes needed to cover the numbers of signals, routes and track circuits which have been defined in the identity files. If the numbers of each are not exactly divisible by eight, the appropriate number of bits in the last byte of each group are set to zero. At the end of the message four bytes of flag information are transmitted irrespective of the number of flag identities defined. For this reason it is essential to ensure that any flags which contain information required by the Train Descriptor are among the first 32 defined in the FLG identity file. Other than the ordering of the identities there is no need to consider the requirements of the Train Descriptor any further when preparing Panel Processor geographic data, though it is of course important to ensure that the Train Descriptor itself is correctly programmed to decode the message.

Train Descriptor systems thus depend on the order of identities in identity files SIG, ROU and TCS, and the order of the first thirty-two identities in the FLG file. Any changes to the order of identities, or the deletion or addition of identities, in these files may affect the Train Descriptor's interpretation of which bit in the message to it represents which function.

Precautions similar to those in SSI8003-53 Section 5 should be taken to avoid upsetting this interpretation.

Where a function required by a Train Descriptor is copied into other Central Interlockings, then the Train Descriptor should normally use the original.

See SSI8003-53 for details of Panel Processor when the Interlocking is connected to an IECC system.

### **3 Data Types in the Panel Processor**

There are three main functions of the Panel Processor which are controlled by the geographic data.

- (i) Setting up the bits in the Output Image to Control Panel indications in response to the information received from the Interlocking.
- (ii) Checking the Steady State Input Image and informing the Interlocking as to whether certain key switches and buttons are still detected in the correct position.
- (iii) Checking the Active Input Image for valid push-button sequences and key switch operations, and sending the appropriate Panel Request to the Interlocking.

As in the Interlocking, these functions are specified by means of the data types which are specified formally in ELS-DOC-2903 "Design of Data Types for the Solid