

Chapter B: Introduction and Simpler Boundaries

1 Introduction

In any signalling scheme there may be a requirement to split the railway into a number of areas, each controlled by a separate Interlocking. In a relay scheme, these areas are determined by the boundaries of the areas allocated to each Control Centre and to each relay room. In an SSI scheme, there also needs to be a subdivision into areas which are within the capacity of a single SSI Central Interlocking; this is determined primarily by the limit on the number of Trackside Functional Modules (TFMs) which can be addressed (63), but there are other factors, see SSI8003-52.

1.1 Methods of Communication

In order to control its operations in the fringe area, each SSI Central Interlocking needs to be able to exchange information with the adjacent Interlocking areas. Two mechanisms are provided for this:

- (i) Communication between SSI Central Interlockings in a single Control Centre takes place over a dedicated pair of data links known as the Internal Data Link (IDL). This is entirely independent of the Trackside Data Links. Up to 30 Central Interlockings can be connected to the IDL in a Control Centre. Each Central Interlocking transmits a message containing 15 eight bit data telegrams, and can decode up to 15 of the telegrams transmitted by the other Central Interlockings.
- (ii) Communication with other types of Interlocking, or with remote SSI Central Interlockings, is achieved by using the inputs and outputs of standard SSI TFMs. Each Signal Module can provide 8 outputs to drive relays and 6 inputs to detect relay contacts.

The data to process these inputs and outputs is written in the appropriate telegrams in the Input Telegram Data and Output Telegram Data. The Input Telegram Data sets up the Interlocking memory with the information received from the fringe Interlocking, and the Output Telegram Data generates the outputs to the fringe area based on the current state of the Interlocking memory.

As part of writing this data, the appropriate forms listing the information transferred by these telegrams has to be updated accordingly. Guidance on completing the forms for the IDL is given in GS/SI8300 Part 3 and in SSI8003-40B Section 3.

When sending and receiving information to and from other Interlockings, single bits in IDL telegrams or TFM/relay interfaces should only be used to convey information across interlocking boundaries where the consequence of transmission failure is tolerable i.e. fail-safe. Intermittent transmission failures are possible and the 'nature' of the data being transmitted by a single bit should be considered - could failure of the transmission result in a wrong-side failure?

1.2 Types of Boundary

The task of data preparation is greatly simplified if the division of the railway into Interlocking areas is designed so as to minimise the information to be transferred - a boundary on plain track is much easier to deal with than one which runs through a complex station area. Boundaries between Control Centre areas, and between separate Signaller's Console areas within a large Control Centre are usually chosen on this basis in any case, but the limited capacity of each SSI Central Interlocking means that each Signaller's area will usually have to be split between three or four SSIs. In a complex area this means that some awkward boundaries are inevitable. In these circumstances it is also important to ensure that the group of Central Interlockings operate together so that the Signaller does not need to be aware of the sub-division of his area. For the purposes of this document, we have categorised 3 types of boundary of increasing complexity:

- (i) Where there is no route locking across the boundary, and the information to be transferred relates to signal controls and approach locking only. This occurs when the boundary can be drawn "through the signal post" on unidirectional running lines with no points in the overlap beyond the signal (see Section 2).
- (ii) Where the boundary is on a bidirectional line, and route locking is provided by means of "slots" on the signals controlling the entrances to the single line section. This will usually occur on a boundary between Control Centre areas (see Section 3).
- (iii) Where the area controlled by a single Signaller has to be split so that routes cross the boundary between Interlocking areas, and the Central Interlockings have to operate together so that the Signaller is unaware of the split (see Chapter C, and Chapter D Section 1).

Items peculiar to boundaries between SSI Central Interlockings and relay controlled areas are covered by Chapter D Section 2.

Certain special or more complex features are covered by Chapter E. These include routes that involve three Central Interlockings or require flank points which are in another Central Interlocking.

2 Boundary Without Route Locking

Figure B1 illustrates the typical boundary which can be drawn on plain double track. In the example Interlocking "LN" controls the down routes up to and including the route from LN45 up to SY101, and receives the inputs from the down line track circuits up to and including HJ. As there are no points in the overlap beyond SY101 and no opposing routes, Interlocking "LN" can set its route from LN45 without reference to "SY", but requires information on the lamp proving and aspect of SY101 and the state of the overlap track circuit HK for use in calculating the aspect to be displayed. The route from SY101 onwards is entirely under the control of Interlocking "SY". This Interlocking has all the aspect control information it requires, but it will also need information about the state of the track circuits and signals from HJ back to HE for its signal stick, temporary approach control and approach locking map search calculations. Similar information needs to be transferred in the opposite direction between the Interlockings to control signals SY100 & LN44 on the up track.

The tables in Figure B1 summarise the information that has to be output from and input to Interlocking "LN". The following sections summarise the data required in "LN" to achieve these functions. If Interlocking "SY" were an SSI, the data would follow the same pattern. The example covers the case where four-aspect controlled signals are provided, with comprehensive approach locking release and temporary approach control facilities. In an area of auto signals, or fewer signal aspects, much of the data below can be omitted.

The use of inputs 7 & 6 in Figure B1, which for Signal Modules may only be used for lamp proving, implies that LN & SY are Interlockings in the same Control Centre communicating via the internal communications systems. The data examples in the following section apply equally to communications between any Interlockings via Signal Modules except that input numbers will have to be changed accordingly, the eight inputs being spread over more than one Module.

2.1 Identity Naming

It is a requirement that identities, that are created just to hold information passed from another Interlocking area, should be named differently such that they can be distinguished from the identities in the originating Interlocking, can be identified as holding copied information, and can meet any restrictions on name duplication required by other associated systems such as Train Describers or IECCs. Additional naming restrictions are imposed by IECC control (see SSI8003-53 Section 4.1).

Where the copied information originates from an Interlocking not in the same SSI (or IECC) scheme then an identifier should be added after the first letter of an identity holding copied information e.g. as in "S(SY)101" below. Where both Interlockings concerned are in the same scheme then the lower case letter 'd' (for duplicate) should be added after the first letter of the identity name. Where an identity is duplicated more than once then 'd', 'dd' etc. should be used. Thus identity TGF in Interlocking "LN" in the examples below will be either T(SY)GF or TdGF, and similarly for THK in "LN". TGF/GK-Z and TGF/GH-Z are

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adequately named as shown. The restrictions on identity order in SSI8003-10C Section 3.3 must be complied with when adding such identities to identity files.

Where information is copied across boundaries with route locking within the same SSI scheme then in some cases a line designation is used instead for identity names. This is covered in Chapter C Section 1.9.

2.2 Signal Inputs

The signal inputs required by "LN" relate to the state of SY101. Conventionally, three inputs would be provided which indicate lamp proving, yellow or less restrictive, and double yellow or green aspects. These inputs are used in "LN" to set up a dummy signal memory S(SY)101:

```
"S(SY)101 7
if G s 6 then S(SY)101 set y else S(SY)101 set r \
if G s 65 then S(SY)101 set yy \
```

The last line of data, in proving both inputs 6 & 5, also caters for the unusual situation where the "YY or G" input 5 can be made without the "Y" input 6 being made. (This occurs when the HR relay is not proved energised in the HHR or DR circuits.)

2.3 Signal Outputs

The signal outputs sent from "LN" to "SY" relate to the corresponding information about the state of LN44:

```
if S44 set lp then G s 7 \
if S44 set <s then G s 6 \
if S44 set <y then G s 5 \
```

2.4 Track Section Inputs

There are five track section inputs required by "LN". These can be split into three categories:

- (i) HK clear is required as it is the overlap track section for the route from LN45 up to SY101.
- (ii) GF occupied is required for temporary approach control and signal stick unsetting of LN44.
- (iii) GF and combinations of GF to GH and GF to GK conditioned by the approach locking and aspect of signals SY100 and SY102 are required for the approach locking release and TORR map searches for LN44 and the next two signals in advance. For the purpose of the map search two special composite track circuit memories are defined. TGF/GH-Z is equivalent to GF & GG clear, and either GH clear or SY100 on and free of approach locking. TGF/GK-Z is equivalent to TGF/GH-Z plus either GJ clear or SY100 on and free of approach

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locking, and either GK clear or SY100 or SY102 on and free of approach locking.

Note that for (ii) a positive indication of GF occupied is required. This is necessary to ensure that any breakdown in communication between the Interlockings cannot cause the track circuit to appear occupied in "LN" while it appears clear in "SY". This requires the allocation of an extra telegram bit to indicate track circuit occupied.

Where there are trailing connections within the map search area in the adjacent Interlocking this will usually result in multiple end points and thus the composite track circuit memory nomenclature above is no longer practical. Suffices S1, S2, S3 should then be used as required and these are explained in Chapter C Section 1.9. Thus TGF/GH-Z and TGF/TGK-Z could be named TGF-S2 and TGF-S3 respectively.

Where the two Interlockings are in different Control Centres, track section information will be passed between these centres to indicate approaching trains. Conditioning by signals on and free of approach locking may not be required and additional track sections may be wanted, thus track section information over and above the typical map search track sections may be required.

Where track section information is received from an adjacent SSI over the IDL the standard "Input Telegram for Track Circuit" and "Input Telegram for Track Circuit (Delayed)" data types must not be used as they are not designed for use with the IDL.

These data types are also not to be used where the track section information is received from a SSI or RRI via a TFM/relay interface. This is because these data types will set the "occupied" bit if a valid message is received from the TFM with the bit indicating the track circuit section set to zero. Another reason to avoid the use of these data types is that they provide bobbing protection by checking three or four successive telegrams respectively before a track circuit memory is regarded as clear. This is undesirable if a similar time delay has already been provided within the sending Interlocking.

A conditional statement is used to test the state of the bit in the IDL telegram and set the track circuit memory to clear or undefined. For the example in Figure B1, the IPT file data for the track sections will be:

```
if G s 4 then TdHK c else TdHK x \
if G s 1 then TGF/GH-Z c else TGF/GH-Z x \
if G s 0 then TGF/GK-Z c else TGF/GK-Z x \
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The two combined track sections will be referred to at the end of the map search data for the up routes from LN44 and the signals in advance.

Guidance on indicating copied track sections is given in Section 2.4.2.