

Ref:	SSI8003-52
Issue:	8
Date:	05/09/2015
Compliance date:	06/12/2015

Module

Timing Constraints on Interlocking Data Complexity

Endorsement and Authorisation

For endorsement, authorisation and issue record of this document, please refer to the SSI Applications Manual Contents, NR/L2/SIG/17002.

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Published and Issued by Network Rail, 2nd Floor, One Eversholt Street, London. NW1 2DN.



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User information

This Network Rail standard contains colour-coding according to the following Red–Amber–Green classification.

Red requirements – *No variations, could stop the railway*

- **Red requirements shall** always be complied with and achieved.
- Red requirements shall be presented in a red box **with the word “shall” or expressed as a direct instruction**.
- Accountability for the efficacy of red requirements lies with the Professional Head/Standard Owner.
- Red requirements are monitored for compliance.
- Corrective actions shall be enforced if deviations are discovered through functional checks (e.g. engineering verification visits, audit or Operations Self-Assurance).

Amber requirements – *Controlled variations, approved risk analysis and mitigation*

- **Amber requirements shall** be complied with unless variation has been approved in advance.
- Amber requirements shall be presented with an amber sidebar **and with the word “shall” or expressed as a direct instruction**.
- Accountability for the efficacy of these requirements lies with the Professional Head/Standard Owner, or their nominated Delegated Authority.
- Amber requirements are monitored for compliance.
- Variations **may** be permitted. Variations are approved by the Standard Owner or through existing Delegated Authority arrangements.
- Corrective actions shall be enforced if **non-approved** variations are discovered through functional checks (e.g. engineering verification visits, audit or Operations Self-Assurance).

Green – *Guidance*

Guidance is based on good practice. Guidance represents supporting information to help achieve **Red** and **Amber** requirements.

Guidance shall be presented with a dotted green sidebar **and with the word “should” (usually in notes) or as a direct instruction**.

Guidance is **not mandatory** and is not monitored for compliance.

Alternative solutions may be used. Alternative solutions do not need to be formally approved.

Decisions made by a competent person to use alternative solutions should be backed up by appropriate evidence or documentation.

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Issue record

Issue	Date	Comments
7	April 2008	5 th Issue
8	Sept 2015	Cross reference in clause 5.1 corrected

Compliance

This Network Rail standard is mandatory and shall be complied with by Network Rail and its contractors if applicable from 06/12/2015.

When this standard is implemented, it is permissible for all projects that have formally completed GRIP Stage 3 (Option Selection) to continue to comply with the issue of any relevant Network Rail standards current when GRIP Stage 3 was completed and not to comply with requirements contained herein, unless stipulated otherwise in the scope of this standard.

Reference documentation

[GS/SI8300](#) SSI Design Workstation Users' Guide

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1 Introduction

Unlike a Route Relay Interlocking which can be expanded to include however many relays are required to carry out a particular task, each Solid State Interlocking has a finite capacity which cannot be exceeded. When the capacity of a single SSI Central Interlocking is exceeded, the controlled area shall be subdivided between a number of Interlockings. There are three major limitations on the capacity of a Central Interlocking:

- The number of TFMs which can be connected.
- The memory capacity of the MPMs & PPMs.
- The processing speed of the MPMs & PPMs.

1.1 Number of Trackside Functional Modules

The maximum number of Trackside Functional Modules which can be controlled from a single Central Interlocking is 63. This is an absolute limit which cannot be exceeded. In the vast majority of situations, any Central Interlocking designed within this limit will also be within the limits imposed by memory capacity and processing speed.

1.2 Memory Capacity

There are limitations on the RAM memory used to store "state of the railway" information, and the EPROM memory used to store geographic data. These apply to both the Interlocking & Diagnostic MPMs and the Panel Processors. The RAM limit determines the maximum number of identities which can be defined for signals, points, track circuits, etc.:

Signals	128
Points	64
Routes	256
Track circuits	256
Flags	1024
Elapsed timers	64
Panel requests	1023
Panel buttons	256
Panel indications	768-1536 (depends on flashable proportion)

Any attempt to exceed the permitted limits on RAM will be detected by the Design Workstation when the identity files are processed. Similarly, if the total volume of data exceeds the EPROM capacity, this will be detected by the data compiler. In either case it should be possible to redesign the data to fit within the limitations. The most likely limiting factors are number of route identities and total data volume.

In the former case, it may be possible to use a common route identity for more than one route (e.g. main/warning/call-on and alternative routes), with a latch being used to identify the route class. In the latter case, there will be scope for reducing the volume of data by use of "carry out tests/commands at.." data constructs for sets of data which are used repeatedly, and by the use of route compounding in the output

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telegram data (OPT file) as described in [SSI8003-63](#). Similar techniques can be used if any of the other memory limitations are exceeded.

The amount of EPROM capacity used is reported when the data compilers are run. This capacity is restricted by the 64K address locations available to the processor and by what other memory devices have to be accessed (see [SSI8003-10B](#) Section 3).

In the "Standard" form of memory, address line range 1000H to AFFFH is used to access the Interlocking MPM data EPROM, BOOOH to FFFFH being used for the program EPROM. The first part of the data EPROM is used for pointers which advise the processor where the various sections of data start. (See [SSI8003-91](#), Table 14).

Above this part is the geographic data, in object code form (see example in [SSI8003-10B](#) Section 5). It is in the same order as the source data, in MAP, PFM, IPT, PRR, FOP, OPT file order.

Due to problems with data volume an "Extended" (or "paged") version of memory has been introduced together with a paged variant of the program. Address line range 8000H to FFFFH is used to access the program EPROM, an increase in memory allocation from 20k to 32k. Address line range 1000H to 2FFFH is used to access section 1000H to 2FFFH in the data EPROM. Address line range 3000H to 7FFFH is used to access sections 3000H to 7FFFH or 7000H to BFFFH or B000H to FFFFH in the data EPROM depending on the states of the two paging lines. This is the equivalent of selecting page one, two or three in memory, hence the term paging. The processor calculates the required paging line settings at the start of processing each block of data, there being a 4k byte overlap between each page which is way beyond the longest conceivable block of data (a 4k block of data would have a point count of around 2000! - see Section 3). Another constraint is that MAP file data shall reside in address range 1000H to 2FFFH, and the data compiler checks on this, again very unlikely to be exceeded.

A paged variant of the Diagnostic MPM program has also been produced for use with "Extended" memory which allows increased data volumes. The paging is done in the same way as above.

The Panel Processor uses only the "Standard" form of memory, address line ranges 8000H to CFFFH allocated to data EPROM and D000H to FFFFH to program EPROM. The pointers are shown in [SSI8003-91](#), Table 15. Data volume limits for this, the Simulator MPM (which can use Extended or Standard form of memory without changing its program) and the Interface Processor (see [GS/SI 8300](#), "SSI Design Workstation User's Guide") are unlikely to be exceeded.

1.3 Processing Speed

To confirm that the signalling system responds rapidly to changes of state at the trackside, the Central Interlocking shall transmit messages to every Trackside Functional Module at regular intervals, and certain parts of the geographic data shall be processed on a regular cyclic basis. The messages to the trackside are transmitted at a minimum interval of 9.5 ms (the minimum Interlocking "minor cycle"), so that each Trackside Functional Module is addressed at a nominal interval of 608 ms (the minimum "major cycle"). These minimum times are increased to 12.85 ms and 822 ms respectively where a Long Line Link is employed, but this does not

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affect data processing capacity. To confirm that all the geographic data is processed once per minor cycle (except the map, points-free-to-move and panel request data which is only processed when required), the following data shall be processed in every minor cycle:

- 1 trackside input telegram
- 1 trackside output telegram
- 1 Internal Data Link telegram (in 30 out of 64 minor cycles)
- 1/64 of the flag operations

When there is a large amount of data to be processed, the time taken may exceed the minimum minor cycle period, and this in turn will extend the overall major cycle time. To allow for this, the Central Interlocking and Trackside Functional Modules have been designed to allow the extension of individual minor cycles up to a **maximum of 30 ms**, and the overall major cycle up to a **maximum of 1000 ms**.

Outside these limits, diagnostic messages are output on the Technician's Terminal which report minor and major cycles which are too long. Two types of Technician's Terminal fault message are provided for excessive length minor cycles; for Panel Requests and for minor cycles which contain too much data. See [GS/SI8300](#), The Design Workstation User Guide (Issue 8, Revision A, May 93) Section 4, for details of the messages displayed. It should be noted that excessive minor cycles due to panel requests are only reported when the panel request is processed. On the other hand, minor cycles which contain too much regularly processed data, or major cycles which contain a large number of long but not excessive minor cycles, may cause an error report on each major cycle. This action can "jam" other fault messages and prevent Technician's controls being applied.

If the minor cycle limit is exceeded there is a risk that some of the Trackside Functional Modules will interpret the gaps between the messages as evidence of Trackside Data Link faults, causing the Modules to reject the messages from the Central Interlocking and enter the "red-retaining" mode of operation. In some cases, clusters of excessively long minor cycles may be masked by the inability to report more than one error, and synchronisation between MPMs may be unable to maintain correct timing. This behaviour is an indication that the MPM is operating outside specified limits and its security fuse may be blown. It is possible that this can occur in more than one MPM, resulting in the shutdown of an Interlocking.

If the major cycle limit is exceeded the ability to tolerate occasional missing messages on the Trackside Data Links is reduced, and the track circuit, approach locking and elapsed timers will run slow (these need to be updated every second, but cannot be updated more than once per major cycle).

The time taken to process any section of geographic data is determined both by the complexity of the data itself, and the current "state of the railway". For instance the "output telegram special" data construct for a signal may include several sets of control data, one for each route from the signal. The time taken to process the data will be determined by which route is set, and the complexity of the data for that route. As the data for the other routes is not processed in these circumstances, their complexity has no effect on the processing time. As the output telegram data for

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signals tends to be the most complex part of the data, the worst case overall major cycle time is reached when the maximum possible number of routes is set.

In practice this tends to be self limiting, as in a complex area with many routes, the Interlocking logic will allow only a small proportion of the routes to be set simultaneously. Experience has shown that major cycle timing problems are comparatively rare, and have only occurred in complex station areas, or on overseas applications of SSI using non-standard aspect sequencing rules. The risk of exceeding the minor cycle timing constraint as a result of a single route of particular complexity is much more likely, and it is this which forms the subject of the remainder of this document.

Measurement of quiescent (i.e. where no routes are set) major cycle time can be useful in revealing potential timing difficulties. High quiescent timing values near to the maximum limit are often indicative of inefficient, poorly optimised data. If there is a suspicion that there is likely to be a problem with excessive major cycles, then setting as many routes as possible will produce the maximum amount of regularly processed data. This in turn will reveal minor cycles which exceed the limit and potentially excessive major cycle timing.

It is important that these timing constraints are taken into account when the data is being prepared, as major retrospective data alterations may be required if timing problems are discovered during testing or in service. A Technician's Terminal fault report is produced if timing limits are exceeded, and in most circumstances this will be observed during testing on the Design Workstation simulation system, but this should not be regarded as a substitute for the designing and checking of data to the rules described below.

1.4 File Processing Order

Within each minor cycle, the Interlocking will process a specific part of data in the following order:

IPT

IPT-IDL – in odd minor cycles and 1st half of major cycle only

FOP

OPT

OPT-IDL – in even minor cycles and 2nd half of major cycle only

PRR – if there is a request waiting and sufficient time remaining

Figure 1 shows which IDL telegrams are processed in each minor cycle. The MAP & PFM files are only accessed if requested by the data processed in the above files.