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Issue:	7
Date:	03/03/2012
Compliance date:	01/09/2012

Module

Data/Compiler/Program Compatibility

For endorsement, authorisation and issue record of this document, please refer to the SSI Applications Manual Contents, NR/L2/SIG/17002.

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User information

This Network Rail standard may contain requirements that are colour-coded according to the following Red–Amber–Green classification.

Red – Mandatory requirements

- **Requirements** that **will** be complied with, and achieved under all circumstances.
- Accountability for the efficacy of these requirements lies with the Professional Head/Standard Owner.
- These requirements are monitored for compliance.
- Local non-compliances, discovered through engineering verification visits, will be reported and monitored through the quarterly Engineering Verification Report.
- Corrective actions will be enforced where local non-compliances remain open beyond the agreed mitigation plan dates.
- These are presented in a red box **and with the word “shall” or a direct instruction.**

Amber – Conditional requirements

- **Requirements** that **will** be complied with unless deviation has been approved.
- Accountability for the efficacy of these requirements lies with the Professional Head/ Standard Owner, or their nominated Delegated Authority.
- These requirements are monitored for compliance.
- Derogations **may** be permitted; which are to be approved by Standard Owner in advance.
- Derogations and Temporary Non-Compliances **may** be granted through the existing Delegated Authority arrangements.
- These are presented with an amber sidebar **and with the word “shall” or a direct instruction.**

Green – Guidance

- Guidance based on good practice; representing supporting information, based on good practice, to help achieve **RED** and **AMBER** requirements.
- This guidance is **not mandatory** and is not monitored for compliance.
- Alternative solutions may be used, which do not need to be formally approved.
- Decisions made by a competent person to use alternative solutions should be backed up by appropriate evidence/documentation.
- This is presented with a dotted green sidebar **and with the word “should” (usually in notes).**

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Issue record

Issue	Date	Comments
6	August 2004	6 th Issue
7	03/03/2012	7 th Issue

Compliance

This Network Rail standard is mandatory and shall be complied with by Network Rail and its contractors if applicable from 03/03/2012.

When this standard is implemented, it is permissible for all projects that have formally completed GRIP Stage 3 (Option Selection) to continue to comply with the issue of any relevant Network Rail standards current when GRIP Stage 3 was completed and not to comply with requirements contained herein, unless stipulated otherwise in the scope of this standard.

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1 Introduction

The data structures used with SSI have remained remarkably stable since the changes made immediately after the pilot scheme at Leamington Spa, but minor developments in data, and associated changes to data compilers and decompilers, and to programs which process the data, whether in the target SSI systems or in SSI Design Workstation (DWS) Simulation Systems have led to a requirement for data compatibility checks. A small number of errors found in the above programs have resulted in constraints on data design, and thus further data compatibility checks are required to confirm these constraints are complied with.

Section 2 has a list which is used to establish which data compatibility checks, on a per Central Interlocking basis, have to be made during the data preparation and checking process. These checks are then detailed in the following Sections, together with any required data changes which may result. Background information is also included for each check. The Central Interlocking Status Record, (CISR) Part 6, is then used to record that these checks have been made.

Once these checks have been made, the data will be compatible with compilers and decompilers on the DWS and with the data-processing program issues that the data will be either tested with on the DWS Simulation System or tested or commissioned with in the target Interlocking. Testing of a particular Interlocking's data on the DWS (or on-site) has to be carried out using data-processing program issues that equate to those intended to be used in this Interlocking on-site when it is commissioned. Where the program issue is subsequently changed, then some retesting may be required to address any changes in data functionality or increases in data processing times.

Program changes in the backwards direction are banned unless site-specific specialised advice, approved by the Infrastructure Owner, is obtained and followed.

Data used in the pilot schemes (category 1A) with original programs (i.e. Leamington Spa, prior to its conversion, and concurrent South African schemes) is a special case and thus outside the scope of this document.

The integrity of these checks depends in part on the use of the CISR to record data Versions/Sub-versions, the associated SSI Design Workstation software issue and on-site program issues.

2 Check List

Every item in this check list shall be examined by both the Data Producer and the Data Checker whenever new data is prepared, or existing data is altered, before the data is passed on for testing. It shall also be used before on-site programs that operate on the data, (as listed in the CISR Part 6), are changed. The check list advises which Sections are to be referred to for the data compatibility checks ("Data Checks") that are to be made, these in turn advising where data changes ("Data Solutions") are required. The successful completion of these actions by both persons shall be recorded in Part 6 of the related CISR.

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2.1 Interlocking MPM Programs

2.1.1

Is this new or changed Version/Sub-version of Interlocking data to be installed in Mkl MPMs fitted with program issue **SSI4303-B3** or in Memory Modules fitted with program issue **SSI4303-C1**?

If the answer is yes then carry out the Data Check in Section 6.

2.1.2

Is this new or changed Version/Sub-version of Interlocking data to be installed in Extended Memory Modules fitted with program issue **SSI4303-D2**, or are such Memory Modules to be introduced at an existing installation?

If the answer is yes then carry out the Data Check in Section 7.

2.1.3

Is this Version/Sub-version of Interlocking data to be tested in a SSI Design Workstation **Simulation System** with an **Extended Memory Module** in its Interlocking MPM?

If the answer is yes then carry out the Data Check in Section 7.

If the answer is no then endorse Part 2 of the master print of the CISR: "This data is not to be tested in a DWS fitted with an Extended Memory Module in its I/L MPM".

2.1.4

Is the new data type "Input telegram special for track circuit (**delayed**)" used in this data?

If the answer is yes and the data is to be installed in a Memory Module then carry out the Data Check in Section 4.1. If the answer is yes and the data is to be installed in Mkl MPMs then carry out the Data Check in Section 5.2

2.1.5

Does this Version/Sub-version of Interlocking data, when compiled, have an **address range that exceeds AFFFH**?

If the answer is yes then confirm via the CISR that the data is installed in an Extended Memory Module fitted with an extended memory variant of the Interlocking MPM Main Processor program SSI4303-D2 or later D issue. Note that the DWS Simulation System used to test this data shall have an Extended Memory Module fitted in its Interlocking MPM.

2.1.6

Is the program, being installed in the same Memory Modules as this Interlocking data, being changed to SSI4303-D4 or later issue?

If the answer is yes then carry out a check on the QST identity file to confirm that the keyword INTERNAL is in the correct place and is effective, i.e. not commented out of use.

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2.1.7

Is the program, being installed in the same Memory Modules as this Interlocking data, being changed to SSI4303-D4 or later issue? Are alternative routes used in this Interlocking?

If the answer to both questions is yes then carry out the Data Check in Section 10.

2.1.8

Is this new or changed Version/Sub-version of Interlocking data to be installed in MkALIII Extended Memory Modules fitted with program AL4303-G2 or later issue or MkWSIII Extended Memory Modules fitted with program WS4303-K1 or later issue?

If the answer is yes then endorse Part 2 of the master print of the CISR: "This data shall only be tested in a DWS3AL Simulation System fitted with a MkALIII MM/MPM as its I/L MPM" or "This data shall only be tested in a DWS3WS Simulation System fitted with a MkWSIII MM/MPM as its I/L MPM", as appropriate.

2.1.9

Is the program, being installed in the same Memory Modules as this Interlocking data:

- Being changed to SSI4303-D4, or is the data being modified with the program already at D4?
- Is it a baseband installation?
- Is Internal Input Telegram 64 in use?

If the answer to all three questions is yes, then a check is required to confirm that both minor cycles one and two process sufficient data to exceed the minimum minor cycle time of 9.5 ms. Data should be transferred to these cycles if necessary by re-arranging FOP data, and or its full stops, or using non-current telegram data in OPT.

If insufficient data is available for transfer (typically during early stage-work), then tests on suitably complex points free both ways with null execution clauses can be used for padding with minimal extra data.

if Pnnn cfn , Pnnn cfr then \ / Dummy data, see SSI8003-54 Section 2.1.9

2.1.10

Is the program, being installed in the same Memory Modules as this Interlocking data:

- Being changed to either WS4303-K1 or AL4303-G2 2MHz interlocking, or is the data being modified with the program already at K1 or later or G2 or later?
- Is it a baseband installation?
- Are there any signals with flashing yellow or flashing double yellow aspects?
- Is there any possibility that they may be controlled by Mk III TFMs, or Mk II TFMs with SSI4311-C4 or D1 software, now or in the future?

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If the answer to all four questions is yes, then the data constructs shown in SSI8003-69B Section 4.2 should be used, although, if the interlocking is so full that it is difficult to squeeze in the extra lamp proving data, then the major cycle time will be long enough that it does not need it.

If the answer to the first bullet is no, but it is yes to the other three, then this construct is also needed in very lightly loaded 1MHz Interlockings with major cycle times below 632 ms.

2.2 Panel Processor Module Programs

2.2.1

Is this new or changed Version/Sub-version of Panel Processor data to be installed in Mki PPMs fitted with program issue **SSI4302-D3** or in Memory Modules fitted with program issue **SSI4302-E1**?

If the answer is yes then carry out the Data Check in Section 6.

2.2.2

Are there more than 32 identities in the **PTS** file of this data?

If the answer is yes then carry out the Data Check in Section 8.

2.2.3

Is this a **panel** controlled scheme employing the **new point key data** introduced in SSI8003 Amendments 91/5 & 91/8 or the **new FM contact data** introduced with Amendment 91/6, otherwise known as **post-Newton data**? (Recognition features: the former utilises a timer per point key and the latter has data in the POD file to generate signal button pulled requests.)

If the answer is yes then carry out the Data Check in Section 9.

2.3 Diagnostic MPM and Technician's Terminal Programs

2.3.1

Is Diagnostics data, compiled from new or changed TFM schedules, to be installed in **Mki MPMs**?

If the answer is yes then carry out the Data Check in Section 5.1

2.3.2

Does this Version/Sub-version of Diagnostics data, when compiled, have an **address range that exceeds AFFFH**?

If the answer is yes then confirm via the CISR that the data is installed in an Extended Memory Module fitted with an extended memory variant of the Diagnostics MPM Main Processor program SSI4306-E1 or later E issue. Note that the DWS Simulation System used to test this data shall have an Extended Memory Module fitted in its Diagnostics MPM.

2.4 Simulator MPM Programs

Data designed for use in 1Mhz Interlockings shall be tested using a 1Mhz simulator.