

### DIS106

## TFM Mk III Flashing Yellow Lamp Proving

### Issue 8

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Approved by:

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#### Distribution: (this issue only)

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## SSI Signalling Principles Group

### TFM Mk III Flashing Yellow lamp proving

## 1 DOCUMENT STATUS

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## 3 PURPOSE OF PAPER

This document provides an "umbrella" for grouping and identifying changes to documents in the SSI Applications Manual for the subject involved whilst the changes are proceeding through the SSI SPG approval process.

## 4 REMIT

To develop a data method for overcoming a software problem in Mk III TFMs when used to feed flashing aspects in association with fast baseband interlockings. It is a problem with at least some Mk II TFMs where fitted with software originally intended for Mk IIIs. This is just to cover flashing (single or double) yellow aspects. This document is restricted to two historic sets of data and one to be used on future schemes.

There is also one related item to tidy up:-

- SSI8003-54 should cover the problem of 'insufficient data' in minor cycles one and two upsetting 1 MHz MPMs on baseband interlockings with D4 software, with Internal input telegram 64 in use if those minor cycles are at or very near minimum minor cycle time of 9.5 ms, due to a timing problem with the ICP interface.

### 4.1 Background

Signal Module software has been through various modifications. When the software changed from SSI4311-C1 to C2, the flashing aspect timing became out of specification. Both light and dark periods became extended. When the module had its EMC enhanced, the software (separately, but in both Alstom [SSI4311-C4] and WRSL [SSI4311-D1] Modules) was further modified with a longer settling time for current proving. As a result, it has become possible for the Module to report lamp proved alight with no lamp present while attempting to display a flashing aspect. For this to happen, the major cycle time has to be very short to allow all the dark period reads to take place and not more than one light period within one interlocking major cycle scan. The vulnerable major cycle time is believed to be in the range 608-632 ms for

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SSI4311-D1 and 608-611 ms for SSI4311-C4, so it can not affect Long Line Link installations. It has been observed in a lightly loaded Westinghouse 2 MHz interlocking, and is theoretically possible with a very lightly loaded 1 MHz interlocking. When this situation occurs, the TFM generally reports lamp proved alight in one cycle in 9, and occasionally during a fifth hour Power Disable Test. During the testing of Proof House Interlocking, it was discovered that the Westinghouse 2MHz interlocking there was fast enough to expose this problem, and as a temporary solution to allow the commissioning to take place, the Mk III Signal Modules were replaced with Mk II Signal Modules for signals displaying flashing aspects.

## 5 DATA SOLUTIONS

### 5.1 Historic Data Solutions

As a precaution for schemes in production at that time (Euston and Willesden), it was decided that a data solution should be created to avoid the intermixing of Mk II and Mk III Signal Modules and the configuration management workload that this would incur. The data solution was created as a temporary fix, but it has been decided that it should be left in place as a permanent feature, even when [if] the Signal Module is modified as it would take some time for the existing stock to be updated.

Three data methods were proposed at the SSISPG meeting 18th October 2000, the first of which was used at Willesden and Euston, and subsequently retro-fitted to Proof House.

The data is contained wholly within the IPT file and requires an extra latch per flashing aspect. The same data construct should be used for single or double flashing aspects, although only the fy data is presented, fyf data is otherwise identical.

This is the method used at Euston & Willesden and Proof House.

This is a stick feature method whereby if a flashing yellow(s) aspect is being displayed and the (bottom yellow) lamp fails the latch is set preventing the lamp proving being set until the stick is primed when any other aspect (including steady yellow(s)) is displayed. This is very much a one shot method, when the lamp proving for the flashing aspect is lost it stays out until the fault is rectified.

/Address 07 - Signal Module

\*I07

"S313 7

/ sets lamp proving if module healthy and bit 7 set

/ The aspect which was supposed to be lit during the major cycle just completed

/ is lamp proved

if S313 set fy

then if S313 clear lp then L313FL(S) s \

if L313FL(S) s then S313 clear lp \

else L313FL(S) xs

\

/6 not used

/5 is EK

/4 is EK

/3 not used

/2 not used

/1 not used

/0 not used

. / end of tgm 07

Subsequent testing at Ashford identified a small chance of the problem recurring with this method, and the following method was tried.