

Parameter extraction techniques for the European mini test chip

ICS 31.200

Committees responsible for this Published Document

The preparation of this Published Document was entrusted to Technical Committee GEL/93, Design automation, upon which the following bodies were represented:

- British Aerospace plc
- Department of Trade and Industry
- Federation of the Electronics Industry
- Institution of Electrical Engineers
- Manchester Metropolitan University
- University of Manchester
- University of Southampton

This Published Document, having been prepared under the direction of the Electrotechnical Sector Board, was published under the authority of the Standards Board and comes into effect on 15 May 1996

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Amendments issued since publication

Amd. No.	Date	Text affected

The following BSI references relate to the work on this Published Document:
Committee reference GEL/93
Special announcement in *BSI News* January 1996

ISBN 0 580 25604 9

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National foreword

This Published Document has been prepared by Technical Committee GEL/93 and is identical with CENELEC Report R117-006 : 1995 *Parameter extraction techniques for the European mini test chip*.

The document is part of a series of six closely related documents describing a technology assessment cycle of submicron CMOS technologies. The other five cover:

- the steps and objective of the assessment cycle;
- the transistor model relating to the effects of submicron CMOS technologies;
- test structures for the extraction of MOS transistor parameters;
- measurements of the test structures;
- a data exchange format which can be used with existing data evaluation programs.

August 1995

English version

Parameter extraction techniques for the European mini test chip

This CENELEC Report has been prepared by Technical Committee CENELEC TC 117, Electronic Design Automation. It was approved by TC 177 on 1995-01-31 and endorsed by the CENELEC Technical Board on 1995-07-04.

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B-1050 Brussels

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Ref. No. R117-006 : 1995 E

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Chapter 1

Introduction

This document is part of a series of documents describing a technology assessment cycle of submicron CMOS technologies. The series consists of six closely related documents [1, 2, 3, 4, 5] in addition to this one. A documentation of the steps and the objective of the entire technology assessment cycle¹ is the contents of [1]. The transistor model which is able to deal with the effects of modern submicron CMOS technologies is presented in [2]. Test structures useable for the extraction of MOS transistor parameters are described in [3]. The documentation of the measurements of these test structures is the objective of [4]. The purpose of document [5] is the presentation of a data exchange format which can be used with existing data evaluation programs.

This report documents the procedures for the extraction of MOS transistor model parameters. These parameters are either common to most MOS transistor models (see chapter 2) or specific to the JESSI 0.8 μ m CMOS model (see chapter 3). The series of parameter extraction routines presented and discussed in this report are developed and verified as a part of the work of the JESSI AC 41 consortium². The extractions are implemented into commercially available programs.

The parameter extraction procedures base on the measurement results which are derived from the modules of the **Parameter extraction Test Chip (PTC)**. The PTC is a part of the **European Mini Test Chip (ETC)** [3]. This mini test chip provides a minimum set of test structures to characterize a technology. The test structures of the ETC are generated automatically by a computer program [3] for a given MOS technology. The measurements which are the base of the extractions presented in this report are documented in [4]. A common data exchange format (Interchange format for Simulated and Measured Data (ISMD)[5]) can be used to ship measured data of the PTC to companies which have no access to the PTC of the desired technology or the required measurement equipment.

The JESSI 0.8 μ m CMOS model is physics-based. Consequently, the extraction procedures of this report are organized in modules. Each module determines the parameters of one physical effect. The measured data required by the extraction modules show the corresponding effect as clearly as possible. As a result, there is a strong correlation between the measured data base and the model parameters to be determined within the extraction module. Within these well defined limits the use of an optimizing algorithm for the determination of model parameters yields accurate results. Since the more accurate model equations which are required for the modeling of submicron MOS transistors often can not be solved algebraically, the use of numerical techniques is inevitable in such cases. The quality of the extracted parameters strongly depends on the careful performance of the required measurements of adequate test structures. The recommended sequence of parameter extractions is shown in figure 1.1. Of cause, the

¹ The Technology Assessment Support Center (TASC) provides detailed informations about the computer programs which support the measurement and extraction routines. Send a FAX or an E-Mail to: TASC, Technology Assessment Support Center, c/o H. Richter, IMS, Allmandring 30a, D-70569 Stuttgart
FAX: +49-711-685-5930
E-Mail: tasc@svls1.mikro.uni-stuttgart.de

² This work is part of the JESSI Program 'Application'-Project AC 41 'Technology Assessment' and is sponsored by the national Public Authorities of Belgium, France, and Germany.

Parameter Extraction - Cycle for the JESSI 0.8 μ m Model

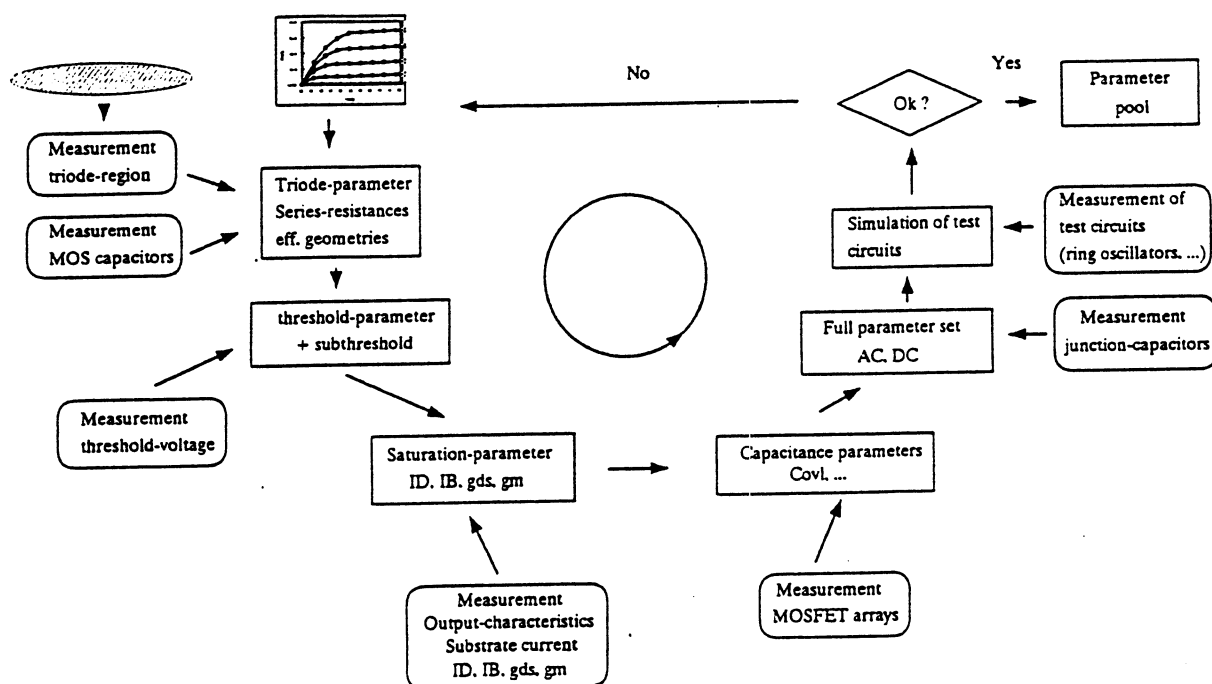


Figure 1.1: The measurement and parameter extraction cycle used for the characterization of a MOS process.

underlying measurements may be performed at any time earlier! A verification procedure used for the extracted model parameters is discussed in section 3.7 of chapter 3.

Finally, the extraction techniques documented here were verified at least with three different CMOS technologies of the JESSI AC 41 project. The feature sizes of these CMOS technologies range from 0.8 μ m down to 0.5 μ m. But, the extraction techniques were also applied to in-house MOS technologies which are not subject of the JESSI project. Consequently, the base of the verification of the extraction procedures is even wider than the three JESSI test chips indicate.

Chapter 2

Extraction of common MOS parameters

The common or basic MOS parameters are the parameters of those equations which are common to most MOS models describing hard doped drains/sources. These models used for circuit simulation. These model parameters describe the triode region of the MOS transistor¹ and the MOS capacitor. In addition the extraction of the pn-junction capacitance parameters of the source and drain implantation areas are documented. The parameter extraction procedures are divided in four modules:

Table 2.1: Table of modules which establish the model-independent parameter extraction routines.

Module COX	Extraction of oxide thickness
Module COVL	Extraction of overlap capacitance parameters
Module CJUNC	Extraction of pn-junction capacitance parameters
Module TRIOD	Extraction of effective geometry and transport parameters

The physical constants used for the parameter extraction are based on [6]:

$$\epsilon_{ox} = 3.9 \cdot 8.854 \cdot 10^{-12} = 3.453 \cdot 10^{-11} \frac{F}{m} \quad (2.1)$$

$$\epsilon_{Si} = 11.8 \cdot 8.854 \cdot 10^{-12} = 1.045 \cdot 10^{-10} \frac{F}{m} \quad (2.2)$$

In the following all voltage values are appropriate for N-channel devices. They have to be reversed for P-channel devices. The maximum operating voltage for the devices is $V_{ds,max}$. Nonlinear optimization means curve fitting of the model equations to the measured device data using nonlinear least square optimization techniques.

¹ Similar extraction techniques can be found in [8] and references therein. The parameter techniques documented in this CEN-ELEC document were verified with at least three different MOS technologies with feature sizes between $0.8\mu m$ and $0.5\mu m$.

2.1 Module COX

2.1.1 Objective

The determination of the thickness of the gate oxide T_{ox} of the MOSFETs is the objective of this module. The gate oxide thickness is extracted from the capacitance data $C(V_{cap})$ of a MOS capacitor with large area (see also table 2.2). The size of the area must be large enough to neglect any differences between designed and electrically active area. For details about the test structure see [3]. The detailed measurement rules are in [4].

Table 2.2: Parameters extracted in the module COX

Name	Type	Synonym	SI unit	Description	PTC test structure
TOX	COX	T_{ox}	m	gate oxide thickness	moscap_20

2.1.2 Model

The model equation for the oxide capacitance C_{acc} of a MOS capacitor in accumulation is:

$$C_{acc} = \frac{Area \cdot \epsilon_{ox}}{TOX} \quad (2.3)$$

The term *Area* designates the area of the active region of the oxide capacitor. The parameter TOX is the oxide thickness. The determination of the correct oxide thickness depends on a negligible difference between the designed and the electrical effective geometry of the MOS capacitor. The designed dimensions of the large area are documented in [3].

2.1.3 Extraction

The accumulation capacitance C_{acc} is extracted at the operating point $V_{cap} = -V_{ds,max}$. The oxide thickness T_{ox} is computed using the equation:

$$TOX = \frac{Area \cdot \epsilon_{ox}}{C_{acc}} \quad (2.4)$$

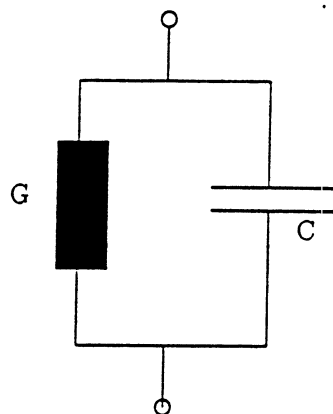


Figure 2.1: Equivalent circuit of the MOS capacitor used for the determination of the gate oxide thickness parameter TOX.

2.2 Module CJUNC

2.2.1 Objective

This module is used to determine the parameters which characterize the pn-junction capacitance of a pn-junction diode (see table 2.3). The parameter determination is based on the capacitance-voltage-measurement (C-V) of a rectangular-shaped and a finger-shaped pn-junction diode. The extraction of the pn-junction capacitance parameters CJ, CJSW, MJ, MJSW and PB is discussed.

Table 2.3: Parameters extracted in the module CJUNC

Name	Type	Synonym	SI unit	Description
CJ	CJUNC	C_j	$\frac{F}{m^2}$	zero bias bottom pn-junction capacitance
CJSW	CJUNC	$C_{j,sw}$	$\frac{F}{m}$	zero bias perimeter pn-junction capacitance
MJ	CJUNC	M_j	1	bottom pn-junction grading factor
MJSW	CJUNC	$M_{j,sw}$	1	perimeter pn-junction grading factor
PB	CJUNC	P_b	V	built-in pn-junction potential

2.2.2 Model

The model equation for the pn-junction capacitance of a reverse-biased pn-junction diode is:

$$C_j(V_j) = \frac{\text{Area} \cdot CJ}{\left(1 - \frac{V_j}{PB}\right)^{MJ}} + \frac{\text{Perimeter} \cdot CJSW}{\left(1 - \frac{V_j}{PB}\right)^{MJSW}} \quad (2.5)$$