

Measurement techniques for the characterization of the European mini test chip

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National foreword

This Published Document has been prepared by Technical Committee GEL/93 and is identical with CENELEC Report R117-005 : 1995 *Measurement techniques for the characterization of the European mini test chip*.

The document is part of a series of six closely related documents describing a technology assessment cycle of submicron CMOS technologies. The following have been published:

- CENELEC Report R117-004 : 1995 *JESSI 0.8 μ m CMOS Transistor Model 117(Sec)51*;
- ENV 50218 : 1996 *Description of a parametrized European mini test chip*;
- CENELEC Report R117-006 : 1995 *Parameter extraction techniques for the European mini test chip*.

The other two documents are in preparation and cover the following areas:

- the steps and objective of the assessment cycle;
- a data exchange format which can be used with existing data evaluation programs.

August 1995

English version

Measurement techniques for the characterization of the European mini test chip

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CENELEC

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Chapter 1

Introduction

This document is part of a series of documents describing a technology assessment cycle of submicron CMOS technologies. The series consists of six closely related documents [1, 2, 3, 4, 5] in addition to this one. A documentation of the steps and the objective of the entire technology assessment cycle ¹ is the contents of [1]. The transistor model which is able to deal with the effects of modern submicron CMOS technologies is presented in [2]. Test structures usable for the extraction of MOS transistor parameters are described in [3]. The documentation of the extraction of the model parameters based on the measurements of these test structures is the objective of [4]. The purpose of document [5] is the presentation of a data exchange format which can be used with existing data evaluation programs.

This report documents the procedures for the measurements required for the extraction of MOS transistor model parameters. These parameters are either common to most MOS transistor models (see chapter 2) or specific to the JESSI 0.8 μ m CMOS model (see chapter 3). The series of measurement procedures presented and discussed in this report are developed and verified as a part of the work of the JESSI AC 41 consortium². The extractions are implemented into commercially available programs. The parameter extraction procedures base on the measurement results which are derived from the modules of the **Parameter extraction Test Chip** (PTC). The PTC is a part of the **European Mini Test Chip** (ETC) [3]. This mini test chip provides a minimum set of test structures to characterize a technology. The test structures of the ETC are generated automatically by a computer program [3] for a given MOS technology. The extraction procedures which are based on the measurements presented in this report are documented in [4]. A common data exchange format (Interchange format for Simulated and Measured Data (ISMD)[5]) can be used to ship measured data of the PTC to companies which have no access to the PTC of the desired technology or the required measurement equipment.

The JESSI 0.8 μ m CMOS model is physics-based. Consequently, the extraction procedures of this report are organized in modules. Each module determines the parameters of one physical effect. The measured data required by the extraction modules show the corresponding effect as clearly as possible. As a result, there is a strong correlation between the measured data base and the model parameters to be determined within the extraction module. Within these well defined limits the use of an optimizing algorithm for the determination of model parameters yields accurate results. Since the more accurate model equations which are required for the modeling of submicron MOS transistors often can not be solved algebraically, the use of numerical techniques is inevitable in such cases. *The quality of the extracted parameters strongly depends on the careful performance of the required measurements using adequate test structures.* A survey of the recommended extraction cycle and the measurements required

¹The Technology Assessment Support Center (TASC) provides detailed informations about the computer programs which support the measurement and extraction routines. Send a FAX or an E-Mail to: TASC, Technology Assessment Support Center, c/o H. Richter, IMS, Allmandring 30a, D-70569 Stuttgart
FAX: +49-711-685-5930

E-Mail: tasc@svlsi1.mikro.uni-stuttgart.de

²This work is part of the JESSI Program 'Application'-Project AC 41 'Technology Assessment' and is sponsored by the national Public Authorities of Belgium, France, and Germany.

Parameter Extraction - Cycle for the JESSI 0.8 μ m Model

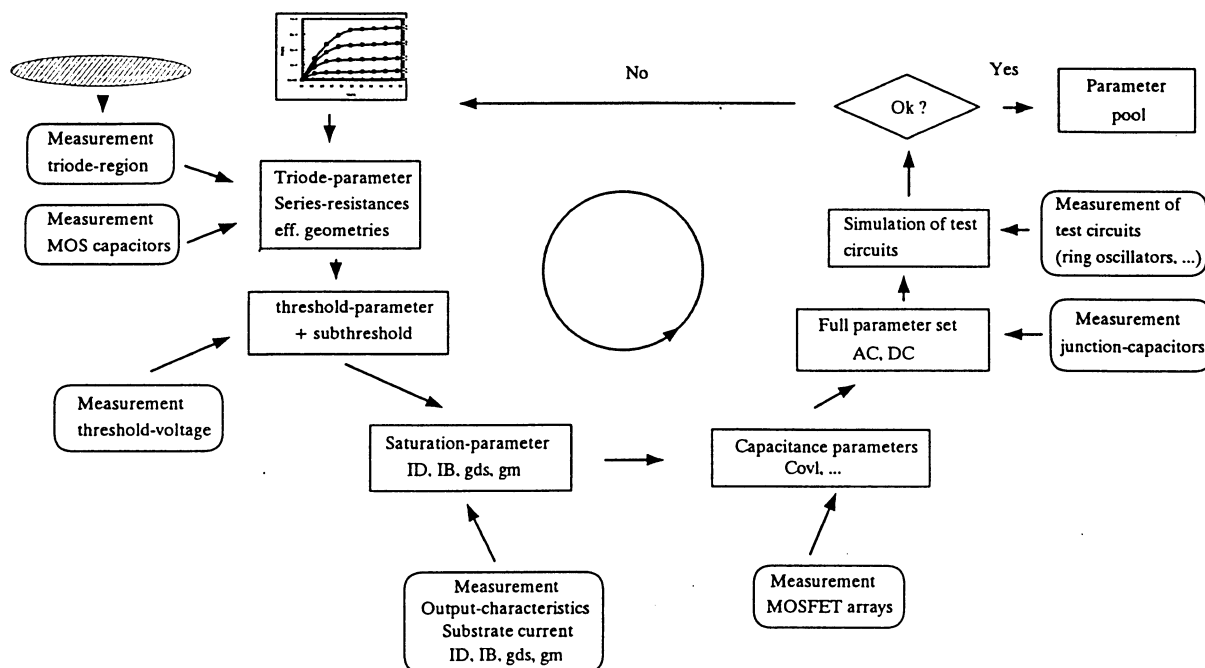


Figure 1.1: The measurement and parameter extraction cycle used for the characterization of a MOS process.

is given in figure 1.1. Of course, the measurements may be performed at any time prior to the parameter extractions!

Last, but not least: The measurements documented in the following chapters may be used in combination with *any* MOS transistor model.

Chapter 2

Measurements for common MOSFET parameters

The common or basic MOS parameters are the parameters of those equations which are common to most MOS models used for circuit simulation. These model parameters describe the triode region of the MOS transistor and the MOS capacitor. In addition the measurements required for the determination of the pn-junction capacitance parameters of the source and drain implantation areas are documented. The measurement procedures are divided into four modules:

Table 2.1: Table of measurements required for the extraction of the model-independent parameters.

Module COX	Measurement of oxide thickness
Module COVL	Measurement of overlap capacitance parameters
Module CJUNC	Measurement of pn-junction capacitance parameters
Module TRIOD	Measurement of effective geometry and transport parameters

In the following sections of this chapter all voltage values are appropriate for N-channel devices. They have to be reversed for P-channel devices. The maximum operating voltage for the devices is $V_{ds,max}$. This quantity is supplied by the vendor of the MOS process.