

JESSI 0.8 μ m CMOS transistor model for analogue and digital circuit simulation

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National foreword

This Published Document has been prepared by Technical Committee GEL/93 and is identical with CENELEC Report R117-004 : 1995 *JESSI 0.8 μ m CMOS transistor model for analogue and digital circuit simulation*. The document is part of a series of six closely related documents describing a technology assessment cycle of submicron CMOS technologies. The following have been published:

- PD 6598 : 1996 (CENELEC Report R117-005 : 1995) *Measurement techniques for the characterization of the European mini test chip*
- ENV 50218 : 1996 *Description of a parametrized European mini test chip*;
- CENELEC Report R117-006 : 1995 *Parameter extraction techniques for the European mini test chip*

The other two documents are in preparation and cover the following areas:

- the steps and objective of the assessment cycle;
- a data exchange format which can be used with existing data evaluation programs

August 1995

English version

JESSI 0.8 μ m CMOS transistor model for analogue and digital circuit simulation

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CENELEC

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1 Introduction

This work has been performed as part of the European Microelectronics program JESSI within project AC41 Technology Assessment".

This report describes the complete model equations of the **JESSI 0.8 μ m** CMOS transistor model for analog and digital circuit simulation in the deep submicron region.

The **JESSI 0.8 μ m** transistor model was developed to provide a MOS transistor model for circuit simulation, applicable to CMOS technologies with device dimensions down to 0.7 μ m.

Details concerning the description of geometry effects and concerning the parameter extraction methods for the **JESSI 0.8 μ m** model will be described in separate reports.

For VLSI/ULSI system design it has become necessary to start circuit design in the early stages of technology development to predict circuit behaviour before the circuit is actually fabricated. Since the device characteristics of sub micron devices are highly sensitive to parameter variations, optimal circuit design becomes even more difficult than before. Therefore it is necessary to get as soon as possible a more accurate link between the technology development and the circuit behaviour with a physically based analytical MOSFET model as a transmitter [1].

In the deep submicron region the influence of the parasitic elements and the LDD-effects grow up dramatically and dominate the behaviour and the performance of the transistor.

In addition to the effects commonly included in a MOSFET model, it is found that the influence of the increased lateral electric field E_y on the bulk charge (threshold voltage), the hot-electron induced output conductance increase, the voltage dependent channel length and drain/source parasitic resistance are the important factors to be considered in deep submicron LDD-MOSFET devices [2].

This model includes all short and narrow channel effects and a substrate current model; special emphasis was placed on the voltage dependent effective channel length and series resistance of LDD devices [3]. It is based on the charge-sheet approximation by Brews [4], including the diffusion and drift current components. To avoid discontinuities at the transitions from subthreshold to linear and from triode to saturation region, transition functions are introduced in a physical way [5], [6].

The model consists of only one equation, is continuous in all regions of operation and needs no internal iteration procedures.

A global overview to the implementation of the model equations is given in figure 1. The complete description of the entire implementation of the MOS model into a simulation program depends on the details of the target simulation program and is beyond the scope of this report. The source codes of the model can be obtained from TASC¹.

¹The Technology Assessment Support Center (TASC) provides detailed informations about the computer programs which support the measurement and extraction routines. Send a FAX or an E-Mail to: TASC, Technology Assessment Support Center, c/o H. Richter, IMS, Allmandring 30a, D-70569 Stuttgart
FAX +49-711-685-5930
E-Mail: tasc@visi1.mikro.uni-stuttgart.de

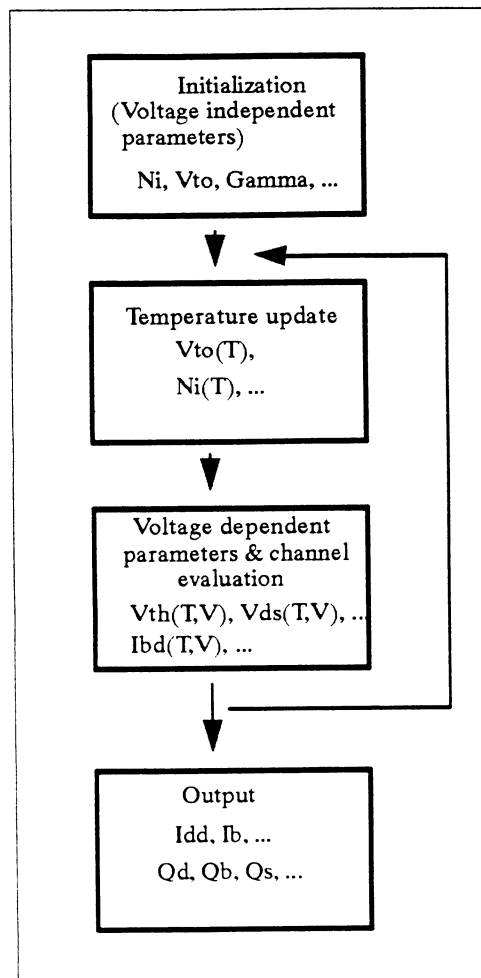


Figure 1: Overview of the implementation of the model equations. It is divided into four parts. The first part initializes the model using voltage and temperature independent values. The second part performs the update of variables describing temperature dependent properties. The third part updates the voltage dependent functions of the model. The model equations use effective voltages. These voltages are determined by external resistances. In order to get the effective voltages right the parts two and three need to be iterated. The fourth part displays the output of the model: currents and charges.

2 Device Geometries

2.1 Channel Length

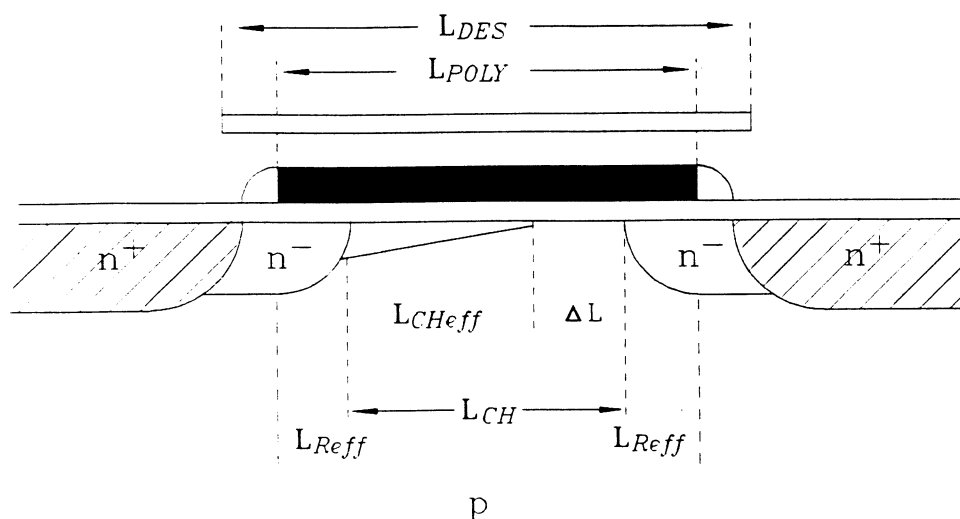


Figure 2: Schematic cross section of an n-channel LDD MOSFET

The channel length of an MOSFET transistor is defined as follows:

$$\begin{aligned} L_{POLY} &= L_{DES} + L_{CORR} \\ L_{CH} &= L_{POLY} - 2 L_{Reff} \\ L_{CHeff} &= L_{CH} - \Delta L \end{aligned} \quad (1)$$

with

- L_{DES} : Designed channel length
- L_{CORR} : Constant correction to L_{DES} to consider process variations
- L_{POLY} : Final poly gate length
- L_{Reff} : Underdiffusion per edge
- L_{CH} : Electrical channel length
- L_{CHeff} : Resulting electrical channel length in saturation
- ΔL : Channel length modulation function in saturation

2.2 Lateral Underdiffusion

For conventional HDD (Hard Doped Single Drain) devices the term L_{Reff} is constant:

$$L_{Reff}^{HDD} = L_D \quad (2)$$

where L_D represents the normally constant underdiffusion per edge from the drain and source regions under the poly gate.

For LDD (Lightly Doped Drain) devices the term L_{Reff} becomes a bias dependent function:

$$L_{Reff}^{LDD} = F(V_{GS}, V_{TH}, \dots) \quad (3)$$

The bias dependent function $L_{Reff} = F(V_{GSeff})$ can be measured, based on channel resistance measurement methods.

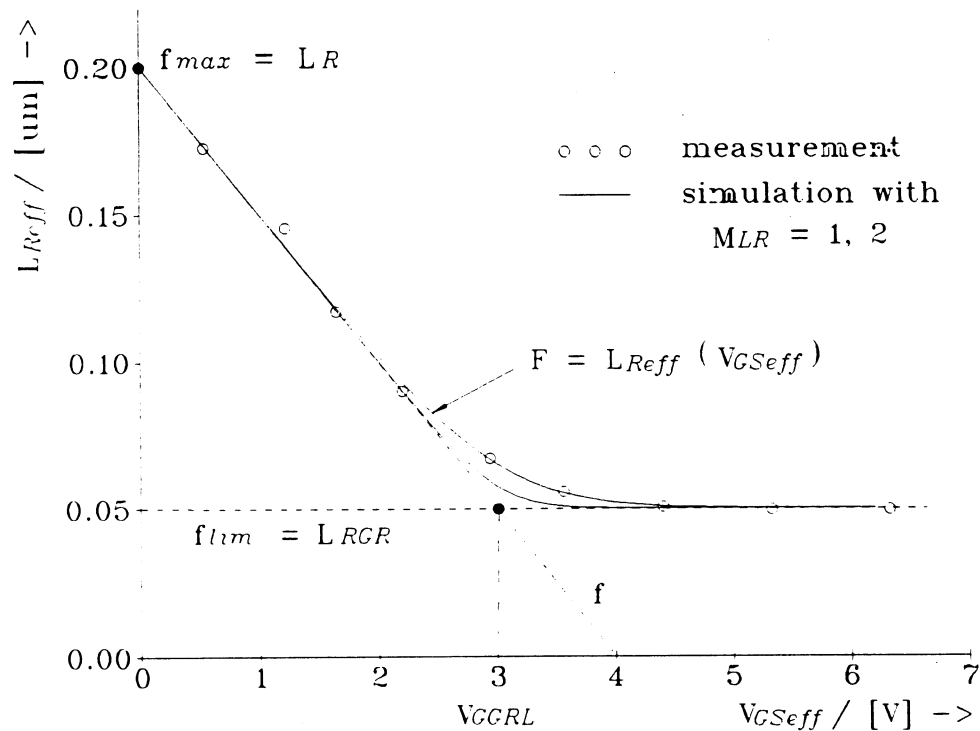


Figure 3: Measurement and simulation of L_{Reff} with the function F

The function L_{Reff} decreases from a high value near threshold to a limit value at high V_{GSeff} voltage. Therefore a transition function is introduced:

$$F = f + \frac{\ln(1 + e^{[m \cdot k \cdot f_{lim} (f_{lim} - f)])}}{m \cdot k \cdot f_{lim}} \quad (4)$$

with

$$k = \frac{10 \ln(2)}{f_{lim} (f_{max} - f_{lim})} \quad (5)$$

For simplicity f is chosen as a linear function in V_{GSeff} , f_{max} is the maximum of f and f_{lim} is a constant value.

From Fig. 3 the function $F = L_{Reff}$ is defined by the following definitions:

$$f = \left(\frac{L_{RGR} - L_R}{V_{GGRL}} \right) V_{GSeff} + L_R \quad (6)$$

$$f_{max} = L_R$$

$$f_{lim} = L_{RGR}$$

$$m = M_{LR} \quad (7)$$

The parameters L_R and L_{RGR} describe the maximal underdiffusion at threshold and the limit value for high V_{GSeff} voltages.

The transition takes place at $V_{GSeff} = V_{GGRL}$.

Under the control of the parameter M_{LR} there is a soft transition between L_R and L_{RGR} .

2.2.1 Definition of the Lateral Underdiffusion for a conventional HDD Transistor

If the device exhibits no voltage dependence of the electrical channel length, only the parameter L_R is to be user-specified. The channel length is calculated as:

$$L_{CH} = L_{POLY} - 2 L_R \quad (8)$$

2.2.2 Definition of the Lateral Underdiffusion for a LDD Transistor

If the parameters L_R , L_{RGR} , M_{LR} and V_{GGRL} are user-specified, then the voltage dependent channel length is calculated as:

$$L_{CH} = L_{POLY} - 2 L_{Reff} \quad (9)$$

2.3 Channel Width

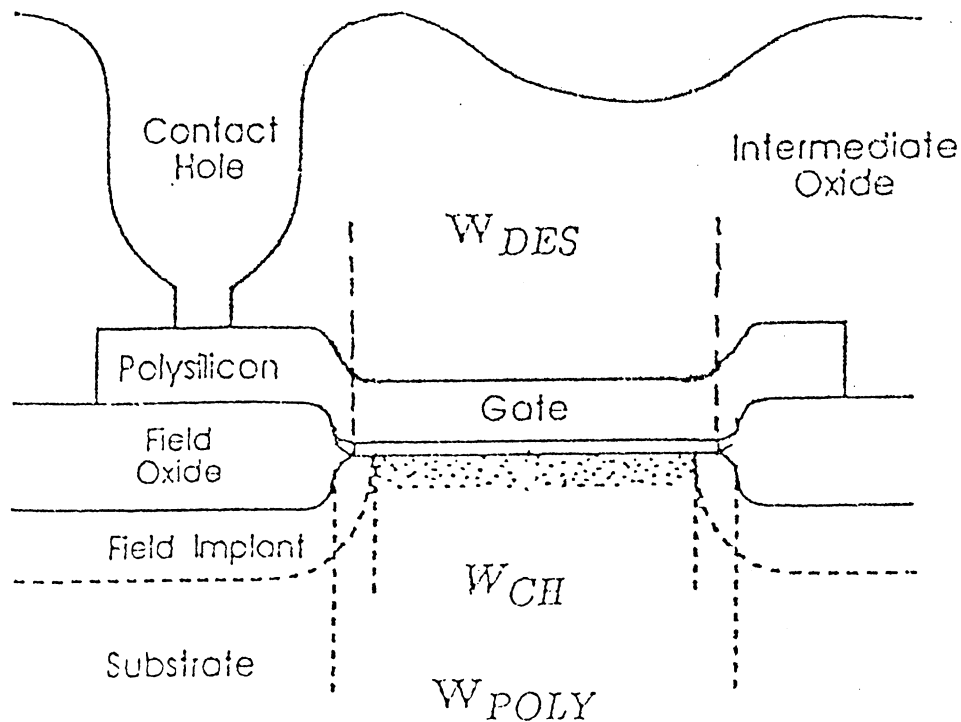


Figure 4: Schematic cross section of an isoplanar MOSFET, Width Cut

The channel width of an MOSFET transistor is defined as follows:

$$W_{POLY} = W_{DES} + W_{CORR} \quad (10)$$

$$W_{CH} = W_{POLY} - 2 W_R \quad (11)$$

with

- W_{DES} : Designed channel width
- W_{CORR} : Constant correction to W_{DES} to consider process variations
- W_{POLY} : Final poly gate width
- W_R : Depleted or accumulated channel
- W_{CH} : Electrical channel width