

Language requirements for high-level synthesis

ICS 35.060

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Contents

	Page
Committees responsible	Inside front cover
National foreword	ii
Foreword	2
Text of CENELEC Report R117-008	5

National foreword

This Published Document has been prepared by Technical Committee GEL/93 and is identical with CENELEC Report R117-007:1995 *Language requirements for high-level synthesis* published by the European Committee for Electrotechnical Standardization (CENELEC).

Summary of pages

This document comprises a front cover, an inside front cover, pages i and ii, pages 1 to 12 and a back cover.

This standard has been updated (see copyright date) and may have had amendments incorporated. This will be indicated in the amendment table on the inside front cover.

English version

Language requirements for high-level synthesis

This CENELEC Report has been prepared by the Technical Committee CENELEC TC 117, Electronic Design Automation (EDA). It was approved by TC 117 on 1995-07-06 and endorsed by the CENELEC Technical Board on 1995-09-20.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Foreword

This Technical Report is a revised version of the report delivered on the 19th of January, 1995, which was sent for commenting to the National Committees. The main improvements introduced in this new version follow the comments received from the National Committees and experts such as Dr. Holger Veit from the GMD, Germany. The authors would like to thank all of them for their valuable contributions.

This work is a result of Task 2 of Workpackage 2 of the ESPRIT 8370 ESIP project. The authors of the report are Eugenio Villar, from the Microelectronics Group of the University of Cantabria, Spain, and Märt Altmäe, from SYNTHESIA, Sweden.

The contents of the Technical Report are not intended for direct standardisation. Nevertheless, they may constitute the technical basis for future standards related with the synthesis application of VHDL. In fact, this report will be used in some of the pre-standards which are considered in the workprogram of WG2 of CLC/TC117. It may also contribute to the synthesis standardisation activities carried out by the IEEE 1076.3 Synthesis Package.

The text of the report was approved for publication by TC 117 on 1995-07-06 and endorsed by the CENELEC Technical Board on 1995-09-20.

Contents

	Page
Foreword	2
1 Introduction	5
2 VHDL high-level synthesis language requirements	6
2.1 Introduction	6
2.2 VHDL high-level synthesis methodology	6
2.3 VHDL for behavioral synthesis	8
3 Conclusions	11
4 References	11