



BSI Standards Publication

Space product assurance — Techniques for radiation effects mitigation in ASICs and FPGAs handbook

National foreword

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Ingénierie spatiale - Guide sur les techniques de durcissement des ASICs et FPGAs vis-à-vis des effets des radiations

Raumfahrtproduktsicherung - Handbuch zu Minderungsmethoden von Strahlungseffekten auf ASICs und FPGAs

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European Foreword

This document (CEN/TR 17602-60-02:2021) has been prepared by Technical Committee CEN/CLC/JTC 5 "Space", the secretariat of which is held by DIN.

It is highlighted that this technical report does not contain any requirement but only collection of data or descriptions and guidelines about how to organize and perform the work in support of EN 16602-60.

This Technical report (CEN/TR 17602-60-02:2021) originates from ECSS-Q-HB-60-02A.

Attention is drawn to the possibility that some the elements of of this dmocuent may be the subject of patent rights. CEN [and/or CENELEC] shall not be held responsible for identifying any or all such patent rights.

This document has been prepared under a mandate given to CEN by the European Commission and the European Free Trade Association.

This document has been developed to cover specifically space systems and has therefore precedence over any TR covering the same scope but with a wider domain of applicability (e.g.: aerospace).

1

Scope

This ECSS-Q-HB-60-02 handbook provides a compilation of different techniques that can be used to mitigate the adverse effects of radiation in integrated circuits (ICs), with almost exclusive attention to Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs) to be used in space, and excluding other ICs like power devices, MMIC or sensors.

The target users of this handbook are developers and users of ICs which are meant to be used in a radiation environment. Following a bottom-up order, the techniques are presented according to the different stages of an IC development flow where they can be applied. Therefore, users of this handbook can be IC engineers involved in the selection, use or development of IC manufacturing processes, IC layouts and ASIC standard cell libraries, analogue and digital circuit designs, FPGAs, embedded memories, embedded software and the immediate electronic system (printed circuit board) containing the IC that can experience the radiation effects.

In addition, this handbook contains an overview of the space radiation environment and its effects in semiconductor devices, a section on how to validate the good implementation and effectiveness of the mitigation techniques, and a special section providing some general guidelines to help with the selection of the most adequate mitigation techniques including some examples of typical space project scenarios.

The information given in this ECSS Handbook is provided only as guidelines and for reference, and not to be used as requirements. ECSS Standards provide requirements that can be made applicable, while, ECSS Handbooks provide guidelines.

2 References

EN Reference	Reference in text	Title
EN 16601-00-01	ECSS-S-ST-00-01	ECSS system - Glossary of terms
EN 16603-10-04	ECSS-E-ST-10-04	Space engineering - Space environment
EN 16603-10-12	ECSS-E-ST-10-12	Space engineering - Methods for the calculation of radiation received and its effects, and a policy for design margins
TR 17603-10-12	ECSS-E-HB-10-12	Space engineering - Calculation of radiation and its effects and margin policy handbook
EN 16602-60	ECSS-Q-ST-60	Space product assurance - Electrical, electronic and electromechanical (EEE) components
EN 16602-60-02	ECSS-Q-ST-60-02	Space product assurance - ASIC and FPGA development
EN 16602-60-15	ECSS-Q-ST-60-15	Space product assurance - Radiation hardness assurance - EEE components
	ESCC 22900	ESCC Basic Specification: Total dose steady-state irradiation test method
	ESCC 25100	ESCC Basic Specification: Single event effects test method and guidelines
	JEDEC JESD57	Test Procedures for the Management of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation
	JEDEC JESD89A	Measuring and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices
	MIL-STD-883/ 1019	Test Method Standard Microcircuits / Ionizing radiation (total dose) test procedure

Terms, definitions and abbreviated terms

3.1 Terms from other documents

- a. For the purpose of this document, the terms and definitions from ECSS-S-ST-00-01 apply.
- b. For the purpose of this document, the terms and definitions from ECSS-Q-ST-60-02 apply, in particular for the following terms:
 1. **application specific integrated circuit (ASIC)**
 2. **cell**
 3. **cell library**
 4. **HDL model**
 5. **intellectual property (IP) core**
 6. **netlist**

3.2 Terms specific to the present document

3.2.1 burst error

burst error is a continuous sequence of data containing errors

3.2.2 critical charge (Q_{crit})

minimum charge a particle deposits in an integrated circuit's node to corrupt its state

3.2.3 data block

group of bits that have an entity of their own, a pre-defined structure and can be subjected to mitigation mechanisms to detect or correct bit errors when verifying the structure correctness

NOTE 1 The term is synonymous to "data groups".

NOTE 2 Examples of groups of bits that have entity of their own include "data frames", "data packets", "data files", "memory pages", "memory words".

NOTE 3 Examples of pre-defined structure are a given bit group size, headers and tails.

NOTE 4 Examples of mitigation mechanisms include EDAC functions and ECC.

3.2.4 data groups

See "data block"

3.2.5 fault masking

phenomena happening when the occurrence of a Single Event Transient (SET) in a circuit does not result in a functional error at the output(s) of the circuit

NOTE 1 Fault masking can happen spontaneously thanks to a “natural” filtering away of the SET caused by the circuitry and the inputs at the time of the SET occurrence, or can be the result of deliberately introduced SET mitigation techniques.

NOTE 2 There are three types of “natural” fault masking phenomena, as explained in 12.2.3 : digital, electrical and temporal fault masking.

3.2.6 memory block

array of multiple memory cells normally organised in sets of bits that can be addressed independently to be read or overwritten in one go

NOTE These sets of bits are often called “words”.

3.2.7 memory cell

basic element of the integrated circuit where one bit of information can be stored, read and written

3.2.8 radiation hardening by design (RHBD)

design techniques that can be applied at physical layout level, at circuit architecture level or at electronic system level in order to mitigate radiation effects

NOTE 1 RHBD addresses both for TID and SEE mitigation.

NOTE 2 The use of RHBD techniques usually introduces a penalty in IC area, power consumption, timing, costs and/or longer development times.

3.2.9 radiation hardening by process (RHBP)

modifications at IC manufacturing process level in order to reduce radiation impact on integrated circuits

NOTE 1 This goal can be achieved by several means such as modifications of doping profiles in devices and substrates, deposition processes optimization for insulators and use of specific materials.

NOTE 2 RHBP mainly addresses TID and SEE effects.

3.3 Abbreviated terms

For the purpose of this document, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
μP	microprocessor
A/MS	analogue/mixed signal
ADC	analogue-to-digital converter
APS	active pixel sensor
ASET	analogue single-event transient
ASIC	application specific integrated circuit
ATSC	Advanced Television Systems Committee
BICS	built-in current sensors
BJT	bipolar junction transistor
BOX	buried oxide
BPSG	borophosphosilicate glass
BRAM	block select RAM
CAD	computer aided design
CCD	charge-coupled device
CED	concurrent error detection
CEU	code emulated upset
CFCSS	control flow checking by software signatures
CLB	configuration logic block
CME	coronal mass ejection
CMOS	complementary metal oxide semiconductor
CNES	Centre National d'Etudes Spatiales
COTS	commercial off-the-shelf
CPU	central processing unit
CRC	cyclic redundancy check
CWSP	code word state preserving
DAC	digital-to-analogue converter
DARE	design against radiation effects
DCC	differential charge cancellation
DCE	domain crossing event
DCM	digital clock manager
DFF	D-flip-flop
DICE	dual interlocked storage cell
DMR	dual modular redundancy
DMS	defense meteorological satellite
DMT	"Duplex Multiplexé dans le Temps", Dual Multiplexing in Time
DRAM	dynamic random-access memory

Abbreviation	Meaning
DROM	demultiplexer-router-multiplexer
DSET	digital SET
DSL	digital subscriber line
DSP	digital signal processor
DT2	double duplex, tolerant to transients
DUT	device under test
DVB	digital video broadcasting
DWC	duplication with comparison
ECC	error-correcting codes
EDA	electronic design automation
EDAC	error detection and correction
EDDI	error detection by duplicated instructions
EEPROM	Electrically Erasable Programmable Read-Only Memory
ELT	enclosed layout transistor
ESA	European Space Agency
ESCIES	European Space Components Information Exchange System
ESD	electrostatic discharge
eV	electron-volt
FEC	forward error correction
FF	flip-flop
FIFO	first in, first out
FIR	finite impulse response
FIT	failure in time
FSM	finite state machine
FOX	field oxide
FPGA	field programmable gate array
FTI	Fault tolerant insertion
FTIS	fault tolerant injection and simulation
GCC	GNU compiler collection
GCR	galactic cosmic rays
GEO	geostationary orbit
GNU	GNU's not unix
GPS	Global Positioning System
HBFT	hypervisor-based fault tolerance
HBT	heterojunction bipolar transistor
HDL	hardware description language

Abbreviation	Meaning
HIT	heavy-ion tolerant
HW	hardware
HWICAP	hardware internal configuration access port
I/O	input/output
IC	integrated circuit
ILO	injection-locked oscillator
IOB	input/output block
ISRO	Indian Space Research Organisation
ISS	international space station
LCL	latching current limiter
LDPC	low density parity codes
LED	light-emitting diode
LEO	low Earth orbit
LET	linear energy transfer
LET_{th}	linear energy transfer threshold
LHC	large hadron collider
LNA	low-noise amplifier
LOCOS	local oxidation of silicon
LPF	low pass filter
LTMR	local TMR
LUT	look-up table
LVDS	low-voltage differential signalling
LWS-SET	living with a star - space environment testbed
MAJ	majority voter
MBU	multiple bit upset
MCU	multiple cell upset
MDAC	Multiplying digital-to-analogue converter
MEO	medium earth orbit
MMU	memory management unit
MOS	metal oxide semiconductor
MOSFET	metal-oxide semiconductor field-effect transistor
MPTB	microelectronics and photonics testbed
MTBF	mean time between failures
MUX	multiplexer
NMOS	N-channel metal-oxide semiconductor
NPOESS	National Polar-orbiting Operational Environmental Satellite System

Abbreviation	Meaning
N-MR	N-modular redundancy
OA	operational amplifier
PCI	peripheral component interconnect
PDS	phase dependent sensitivity
PLL	phase-locked loop
PMCD	phase-matched clock divider
PMOS	P-channel metal-oxide semiconductor
POA	post oxidation anneal
POR	power-on reset
PUC	processing unit core
PVT	process, voltage and temperature
RAID	redundant array of independent disks
RAM	random access memory
RAR	Roshal ARchive
RHBD	radiation hardening by design
RHBP	radiation hardening by process
RoRa	reliability oriented place and route
RS	Reed-Solomon
RTL	register transfer level
SAA	South Atlantic anomaly
SEDR	single event dielectric rupture
SEGR	single event gate rupture
SEHE	single event hard error
SESB	single event snapback
SBIRS	space based infrared system
SCSI	small computer system interface
SE	soft error
SDRAM	synchronous dynamic random-access memory
SEB	single event burnout
SEC-DED	single error correction-double error detection
SEE	single event effect
SEFI	single event functional interrupt
SEGR	single event gate rupture
SEL	single event latch-up
SER	soft error rate
SerDes	serializer/deserializer

Abbreviation	Meaning
SET	single event transient
SEU	single event upset
SIFT	software implemented hardware fault tolerance
SiGe	Silicon Germanium
SNR	signal-to-noise ratio
SoC	system on chip
SOI	silicon on insulator
SOS	silicon on sapphire
SPE	Solar particle event
SPF	single point failure
SPICE	Simulation Program with Integrated Circuit Emphasis
SRAM	Static Random Access Memory
SSD	solid-state drive
STI	shallow trench isolation
STRV	space technology research vehicle
SW	software
S/H	sample on hold
TID	total ionizing dose
TMR	triple modular redundancy
TNH	track and hold
TNID	total non-ionizing dose
TPA	two-photon absorption
UART	universal asynchronous receiver-transmitter
UMC	United Microelectronics Corporation
USAF	United States Air Force
VCDL	voltage-controller delay line
VCO	voltage controlled oscillator
VHDL	VHSIC hardware description language
VHSIC	very high speed integrated circuits
WL	write line
WOV	window of vulnerability

Radiation environment and integrated circuits

4.1 Overview

Failures induced by radiation have become one of the most challenging issues for modern electronic systems, in particular for space applications. Many efforts have been spent in the last decades to measure, model, test and mitigate radiation effects, applying numerous different techniques approaching the problem at various abstraction levels.

Section 4 gives the reader a general overview of radiation in space and its effects on integrated circuits. Firstly, the radiation environment is briefly summarised. It is then followed by a discussion on the major radiation effects on integrated devices. Finally, the test and validation methods are shortly exposed.

The content of this section is not exhaustive. It is only informative with the purpose to provide generic information on sources of radiation in space and their effects on ICs.

NOTE The text of this handbook contains several bibliographic references, indicated with “[#]”. To find the appropriate title of the referenced document click on the “[#]”.

4.2 Radiation environment in space

This section provides a brief summary of information from ECSS-E-ST-10-04, ECSS-E-ST-10-12 and ECSS-E-HB-10-12.

The radiation environment [1] takes its origin either in the Sun (e.g. solar flares, coronal mass ejection [2] and solar wind) or from outside the solar system (e.g. the galactic cosmic rays [3]). Energetic charged particles, mainly electrons, protons and heavy ions, are encountered throughout the Earth's magnetosphere, in interplanetary space and in the magnetospheres of other planets. Part of the particle spectra with energies in the MeV range or above are able to traverse spacecraft shielding and irradiate electronic components. In particular, spacecraft orbiting the Earth crosses the Earth's radiation belts (also named Van Allen belts), that extend from 100 km to 65000 km and consist principally of electrons and protons.

In addition to these primary particles, secondary radiation, such as X-rays produced by the interaction of electrons with shielding (e.g. Bremsstrahlung photons) are able to deposit large radiation doses in EEE components. Another example of secondary radiation are the secondary ionising particles (protons, ions) produced by the interaction of high energy protons with the component materials [4]. Some neutrons are also encountered in space, for example ejected by the Sun, or as secondary radiation in planetary environment, such as around Mars or the Earth. For LEO orbits around the Earth (incl. ISS), neutrons can be significant depending on the geomagnetic latitude and the solar activity. They come from the Earth's atmosphere, some of them being emitted back into space as atmospheric albedo neutrons.

The flux of particles in the Earth atmosphere at avionic and ground levels (from the cosmic ray shower in the atmosphere, and from the Earth telluric activity) are several orders of magnitude lower than the flux of particles encountered in space. Hardening of electronics at ground or avionic levels are not

addressed here. This handbook only considers radiation effects and mitigation for the space radiation environment.

For each space mission, the radiation environment is specific; it is established including all types of radiation, depending on the orbit or voyage characteristics, the mission duration and possible shielding. Note that the space radiation environments are highly dynamic, depending on solar activity and “flares” (more correctly, solar particle events), and for specific missions (for example in the vicinity of Jupiter’s moons) significant uncertainties remain. Therefore it is important that these large variations of the space radiation exposure are considered in the radiation design margins for EEE components selection and test.

4.3 Radiation Effects in ICs

4.3.1 Overview

This section provides a brief summary of information from ECSS-E-HB-10-12, ECSS-E-ST-10-12 and ECSS-Q-ST-60-15. It applies to EEE components in the spacecraft payload and launcher.

Radiation effects in EEE components can be separated into cumulative effects, which lead to a progressive degradation of the component characteristics, and single event effects, which gather different types of events, destructive or non-destructive, induced by a single particle.

4.3.2 Cumulative effects

Exposure to primary and secondary radiation produces relatively stable, long-term changes in devices and circuit’s characteristics that can result in parametric degradation and ultimately in functional failure. Cumulative effects include both Total Ionizing Dose (TID) and displacement damage (DD), also called Total Non-Ionizing Dose (TNID):

- TID effects are induced by the transfer of ionising energy from the radiation exposure, which thermalized in the creation of electron-hole pairs in the component material. These charges typically get trapped in dielectric layers (e.g. oxides or nitrides) either in the bulk of the dielectric, or at or near the interface with the semiconductor where the electrostatic effect on the device operation is maximum. This produces a variety of effects on the device characteristics such as flatband and threshold voltage shifts, leakage currents and timing skews. TID is expressed in Gray (Gy) or rad (100 rad = 1 Gy), with 1 Gy = 1 J/kg. TID effects in semiconductors are discussed further in Clause 7 of ECSS-E-ST-10-12C, Section 6 of ECSS-E-HB-10-12C. TID test methods are described in ESCC22900. TID engineering approach for radiation hardness assurance is given in ECSS-Q-ST-60-15, section 5.1 TID effects are of concern for integrated circuits. Depending on the spacecraft mission and orbit, and the device shielding, the received TID typically ranges from few krad(Si) to several 100’s krad [8]. Mitigation techniques to TID are addressed in this Handbook.
- TNID effects are induced by the non-ionising transfer of energy, i.e. by the interaction of primary and secondary energetic particles with component atoms, eventually creating damage and stable electrically active defects in the semiconductor crystal lattice. This gives rise to a variety of effects in bipolar devices and all types opto-electronics including CCD and APS detectors, LED and laser diodes. Typically ASICs and FPGAs are not be affected by TNID. This Handbook does not address mitigation techniques for TNID.

4.3.3 Single Event Effects (SEEs)

4.3.3.1 Overview

The charge deposited by a single ionizing particle can produce a wide range of effects. Some of them, such as Single-Event Transient (SET), Single-Event Upset (SEU) and Single-Event Functional Interrupt (SEFI) are temporary and can be recovered. Others can lead to permanent damage such as Single-Event Latch-up (SEL) or Single-Event Gate Rupture (SEGR).

These effects can be produced, as also illustrated in Figure 4-1.

- By direct ionization, for example in the case of heavy ions and low energy protons (for deep sub. The heavy ion ionising effect is usually expressed by the linear energy transfer (LET), in $\text{EV}\cdot\text{cm}^2/\text{mg}$, which is the ionising energy transferred along the ion path, normalised by the material volumetric mass density.
- By secondary particles issued from nuclear reactions or elastic collisions, as typically produced by protons. In this case particle (e.g. proton) energy is usually expressed in MeV.

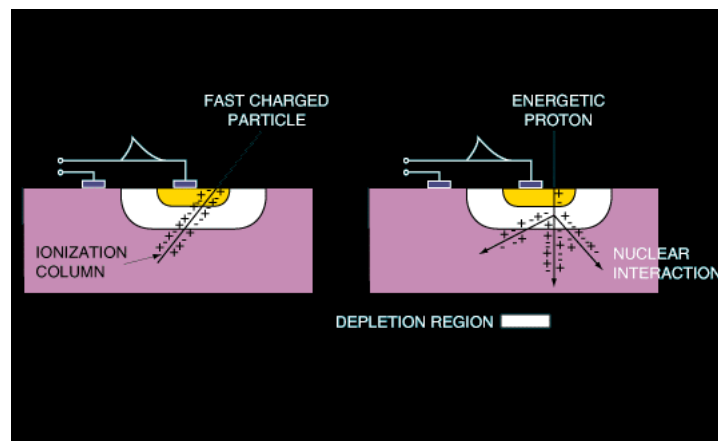


Figure 4-1: Schematic showing how galactic cosmic rays deposit energy in an electronic device, after Lauriente and Vampola [321]

The sensitivity of a device to SEE is often expressed by the cross-section σ as a function of the ion LET or proton energy. σ is defined by the ratio of the number of observed single events by the particle fluence (particles per cm^2) received by the component under test as explained in ESCC25100[5]:

$$\sigma = \text{number of events} / \text{fluence}$$

The cross-section represents the probability that an impinging particle provokes a single event. The unit of SEE cross-section is cm^2 for all types of circuits. In the particular case of upsets in memories, it can be normalised by the number of bits, i.e. expressed in cm^2/bit . When SEE are induced by direct ionisation from ions, the cross-section is representative of a sensitive area. For indirect ionisation from high energy protons, the SEE cross-section also includes the probability of nuclear interaction, which renders its interpretation more complex.

A non-exhaustive list of destructive and non-destructive SEE effects is provided in 4.3.3.2. These are summarised from Clause 9 of ECSS-E-ST-10-12C, Section 8 of ECSS-E-HB-10-12C, and ESCC25100. Other information about SEE test methods are exposed in ESCC25100, and SEE engineering approach for radiation hardness assurance in ECSS-Q-ST-60-15, Clause 5.3.

The non-destructive SEEs, also called soft errors, such as Single-Event Transient (SET), Single-Event Upset (SEU) and Single-Event Functional Interrupt (SEFI) are temporary and can be recovered. The

destructive SEEs, such as Single-Event Latch-up (SEL), Single-Event Burnout (SEB) or Single-Event Gate Rupture (SEGR), lead to permanent damage. Those of interest for this handbook are detailed, while others, rarely encountered in ASICs and FPGA, are only shortly described.

4.3.3.2 Non-destructive SEE

4.3.3.2.1 Single-Event Transient (SET)

A SET is a temporary voltage excursion (voltage spike) at a node in an integrated circuit. It is generated by a single particle ionising the semiconductor and passing through or near a sensitive junction. SETs are usually separated in two categories:

- Analogue SET (ASET) in analogue and RF designs, and opto-electronics.
- Digital SET (DSET) in digital design, including all functions of combinatorial and sequential logic.

SETs are non-destructive. They result in a large variety of effects at the circuit level, ranging from a SEU (see 4.3.3.2.2) if the SET is captured by a storage element, to spurious voltage transients, false signal or miss counts, temporary disability of the circuit, or at worst SEFI (see 4.3.3.2.4).

4.3.3.2.2 Single-Event Upset (SEU)

An SEU is a single bit flip, i.e. the change of state of a storage element, such as flip-flops, latches or SRAM cells. SEUs can be either silent if unused or corrected by error correction code (ECC), or result in different types of effects at the circuit level, including circuit malfunction or SEFI.

As for SETs, the sensitivity to SEU greatly varies depending on the technology, design and electrical operation. In particular, small transistor dimensions and reduced supply voltage tend to decrease the critical charge (i.e. the minimum charge collected at a sensitive node able to induce a state change), and thus increase the sensitivity to SEEs.

4.3.3.2.3 Multiple-Cell Upset (MCU) and Multiple-Bit Upset (MBU)

- MCU is the change of state of two or more logic cells induced by a single particle strike. The corrupted cells are usually, but not always, physically adjacent.
- MBU is a particular case of MCU when the corrupted cells are in the same word. Note that MBU cannot be corrected by a simple (single-bit) error correction code.

Integrated circuits tend to be increasingly sensitive to multiple upsets as gaps between transistors are becoming smaller with technology scaling. Charge deposited by an energetic particle can be collected by several sensitive nodes and thus results in SEUs in several memory cells.

4.3.3.2.4 Single-Event Functional Interrupt (SEFI)

As defined in ECSS-E-HB-10-12, a SEFI is a soft error that causes the component to reset, lock-up, or otherwise malfunction. SEFI typically occurs in complex devices with built-in state/control sections like in modern memories (e.g. SDRAM, DRAM or NOR- and NAND-Flash), all types of processors, FPGA or ASICs, or mixed-signal devices [9]. Two main types of SEFI are distinguished depending on the actions required to restore operability: reset by software or by power cycling. The stored data can or cannot be lost.

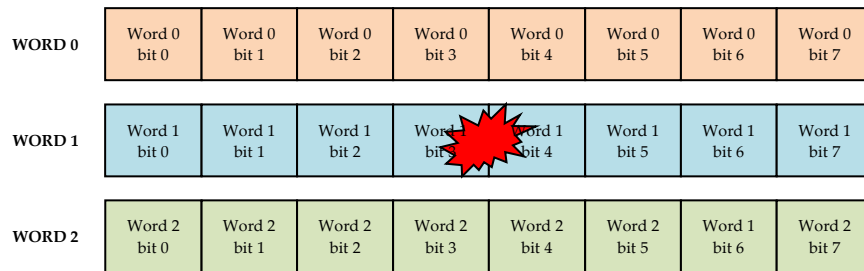


Figure 4-2: Two upsets in the same word induced by a single particle (MBU)

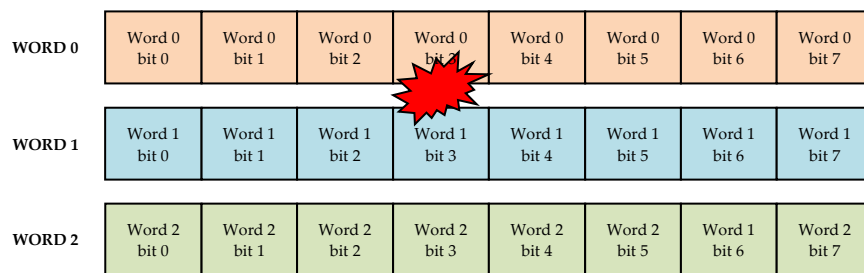


Figure 4-3: Two upsets in the different words induced by a single particle (MCU)

4.3.3.3 Destructive SEE

4.3.3.3.1 Single-Event Latch-up (SEL)

A Single-Event Latch-up is the result of the triggering of a parasitic thyristor (PNPN or NPNP structures) mainly existing in CMOS circuits [345]. When it occurs, a high current flows and if the power supply is maintained, the device can be destroyed by thermal effect. The SEL signature is a self-sustainable current flowing in the low impedance path of the triggered parasitic thyristor structure whose gain increases with temperature. The only way to remove SEL is to power-reset the circuit. SEL are not to be mistaken with temporary current spikes resulting from SET induced logic conflicts or SEFI.

4.3.3.3.2 Single Event Snap-Back (SESB)

Another type of potentially destructive SEE, very similar to SEL with a self-sustainable current signature but less common, is the single event snap-back (SESB). The SESB is the result of the triggering of a parasitic bipolar structure (NPN or PNP). For example when each transistor is dielectrically isolated from its neighbours, SOI MOS is not sensitive to SEL, but it can be sensitive to SESB because of floating body effects when body contacts are insufficient.

4.3.3.3.3 Single Event Hard Error (SEHE)

As per ECSS-E-HB-10-12 and ESCC25100, a SEHE (also called “stuck bit” or hard error) is an unalterable change of state associated with a permanent or semi-permanent damage of a cell by an ion strike. This is typically encountered in all types of memories and digital devices.

4.3.3.3.4 Single Event Burnout (SEB)

As defined in ECSS-E-HB-10-12, SEB is the triggering of the parasitic bipolar structure in a power transistor (typically n-channel), accompanied by regenerative feed-back, avalanche and high current condition. SEB is potentially destructive unless suitably protected.

SEB is not frequent in ASICs and FPGAs, except in the case of embedded lateral or vertical power devices.

4.3.3.3.5 Single Event Gate Rupture (SEGR) or Single Event Dielectric Rupture (SEDR)

As defined in ECSS-E-HB-10-12, SEGR or SEDR is the destructive rupture of a gate oxide or any dielectric layer by a single ion strike. This leads to leakage currents under bias and can be observed in power MOSFETs, linear integrated circuits (with internal capacitors), or as stuck bits in digital devices. The energy transfer and damage induced by energetic heavy ions in dielectrics is so fast ($\ll$ ps) compared to the time response of any electrical protection (e.g. filtering), that there is no possible protection against SEGR / SEDR.

4.3.3.4 Summary

Table 4-1 summarises the major single event effects (SEEs) typically encountered in different types of component technologies and families.

Table 4-1: Summary of single event effects (SEE) as a function of component technology and family

Technology	Family	Function	SEL, SESB	SEGR, SEDR	SEB	SEU	MCU/MBU	SEHE	SEFI	SET
			destructive SEE			Non-destructive SEE				
Power MOS				X	X					
CMOS, BiCMOS and SOI	Digital	SRAM	X			X	X	X		
		DRAM	X			X	X	X	X	
		FPGA	X			X	X	X	X	X
		Flash EEPROM	X			X		X	X	
		μ P / μ controller	X			X	X		X	X
	Mixed signal	ADC	X	X	X	X			X	X
		DAC	X	X	X	X			X	X
	Linear		X	X	X					X
Bipolar	Digital			X	X	X				X
	Linear			X	X	X				X

Choosing a device hardening strategy

5.1 The optimal strategy

In the vast majority of cases, not just one but several mitigation techniques are applied to protect ASICs or FPGAs from the radiation effects.

There are multiple parameters that determine what makes one group of techniques more or less suitable in each case. There are always compromises to be made between the technical requirements and goals, and the actual financial, development time and resources constraints.

There is no ideal decision-flow-chart or recipe to guide a system and/or component designer about which techniques are the best ones for his/her case, however this Section gives some general guidelines on what to consider. Multiple aspects, expertise and inputs are taken into account:

- Space radiation environment experts and system engineers providing the radiation environment requirements,
- System and product assurance engineers providing the reliability, performance and availability (can the system tolerate pauses in its operation?) targets,
- Vendor provided information on the radiation effects sensitivity of the candidate technologies (or existing part) to be used,
- Any independent or internally acquired complementary information about the sensitivity of the technology to be used (more radiation effects tests results),
- Experience (and access to relevant IC design tools) of the actual IC designers in applying safely and efficiently rad effects mitigation,
- Experience (and access to relevant PCB/electronic system design tools) of the system engineers where the device is intended to be used in applying safely and efficiently rad effects mitigation.

A simplified flow to make correct decisions over which mitigations can be applied (or selected) can look like this:

1. Define the radiation environment that can affect your IC (what radiation levels for my orbit, mission duration?).
2. Define the reliability targets, i.e. how many errors (of a given fault class) per time unit (e.g. year) can be tolerated by the user.
3. Identify candidate IC technologies or existing parts and collect data on their sensitivity to TID and SEE.
4. Identify and quantify all the effects (pros and cons) of mitigation techniques which can be introduced at the various levels.
5. Choose the best compromise of mitigation that allows to meet the reliability targets while also respecting the rest of the requirements. In doing this, the expected levels of final fault tolerance (e.g. error rates) are estimated by analysis, simulation or tests.
6. Once implemented, validate the selected approach by fault-injection and/or radiation testing.

The best choice of basic technology and mitigation that allows to meet all technical requirements and cost and schedule constraints often requires several iterations along points 3 - 6 above.

While insufficient protection can cause costly corrections at a late stage in the flow, it is emphasised here that over-protecting can be equally detrimental to the success of a development, as it can lead to excessive complexity, performance degradation or long development times.

In the following sections these steps are explained and linked to the rest of the sections of this handbook.

5.2 How to use this handbook

This handbook has been written and structured as a compilation of known mitigation techniques, preceded by an overview of basic concepts about the radiation environment and its potential negative effects in ASICs and FPGAs (Section 4) and ending with guidelines to validate that those mitigation techniques are working as expected (Section 16).

It is important to understand that these mitigation techniques can be applied at “different levels” or stages of the creation or use of the integrated circuit, and therefore by different types of specialists. Mitigation techniques presented in this handbook are classified according to the following identified “levels” of abstraction:

- Manufacturing Process level: techniques concerning manufacturing processes, also known as Radiation Hardening By Process. These approaches generally concern modifications of doping profiles in devices and substrates, deposition processes optimization for insulators and use of specific materials.
- Physical Layout level: techniques aiming at optimizing transistor’s layout and placement in order to reduce radiation sensitivity of the final circuit.
- Circuit Architecture level: techniques devoted to this level are most often specific to circuit’s nature (digital, analogue or mixed signal) and/or to circuit’s family (ASICs, FPGAs or embedded memory). Moreover, a majority of them belong to main approaches such as redundancy (hardware or temporal) or Error Detection And Correction (EDAC).
- Electronic System level: these techniques apply at component level (e.g. microprocessor redundancy), unit level or embedded software level (e.g. computer redundancy).

These different “levels” and the naming conventions used in this handbook are explained graphically in Figure 5-1.

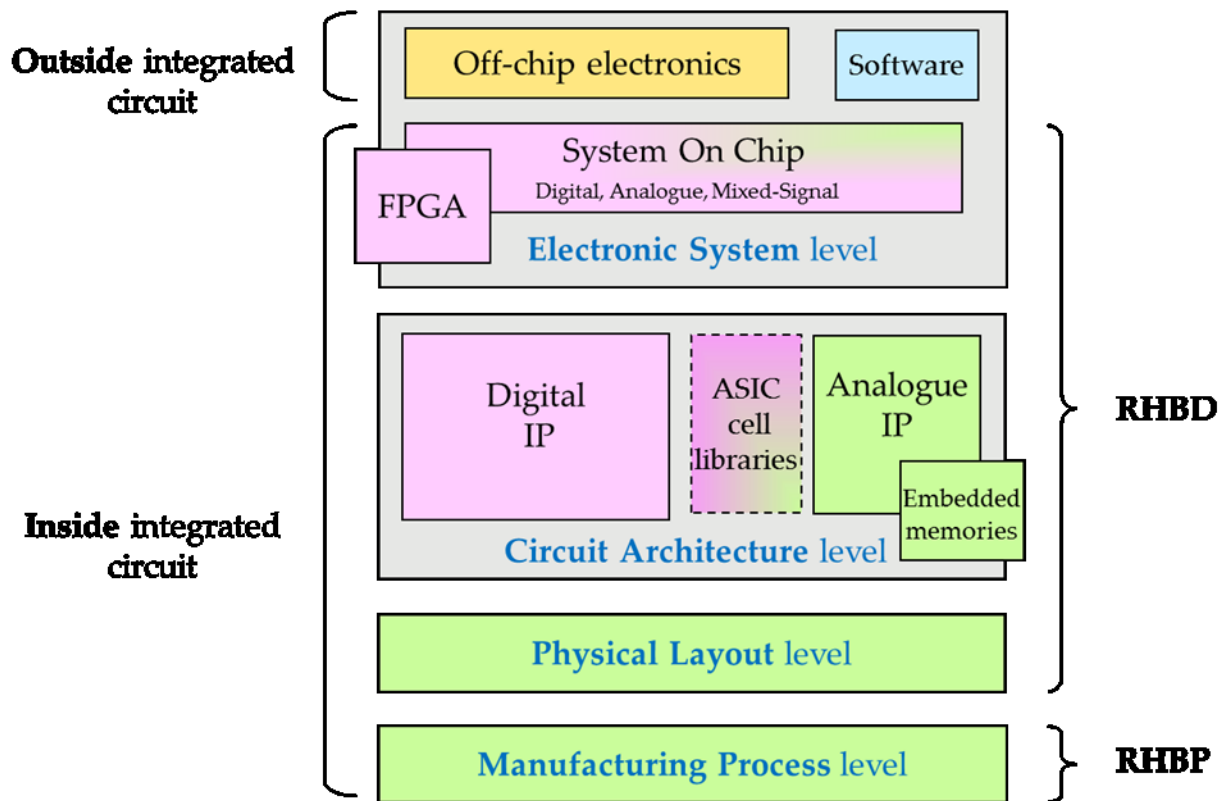


Figure 5-1: Different abstraction levels where mitigation techniques can be applied and naming convention for this Handbook.

In fact, it was difficult to decide how to classify and present to the readers the various mitigation techniques, since many of them, conceptually are the same, and yet, can be applied at different “levels”. For example, the well-known “TMR” technique (hardware redundancy and voting), can be applied at “cell” level, by designers creating a rad hard flip-flop for an ASIC cell library or rad-hard memory elements to be pre-diffused in rad-hard FPGAs. This work is done by IC designers who do design at transistor, full-custom analogue level. However, the same TMR concept can be applied at a higher-level by the IC designers making use of the ASIC or FPGA design kits, and choosing to triplicate non-rad-hard cells and majority vote afterwards. At an even higher-level of abstraction, we can choose to triplicate an entire non-rad hard ASIC or FPGA on the PCB, and majority vote on their outputs, to discard a bad output due to radiation.

In an effort to avoid repetitions, the strategy adopted in this handbook is to explain each mitigation technique only once, in the Section corresponding to the level where the technique is most often applied. In other abstraction levels addressed in other Sections of this handbook where the same technique can be applied, a cross-reference is made to where the technique is fully described.

Depending on the actual background and role of the reader of this handbook, one or another Section is more relevant in order to find, decide or apply the relevant mitigation techniques according to his/her area of expertise and his/her role in the ASIC or FPGA development or utilisation.

Depending on the orbit type, the mission duration and the expected solar activity during the mission, the worst case radiation levels are investigated and communicated to the system and component engineers who have to decide how to protect the ICs. If standard components are developed, it is important to consider multiple orbit types. Section 4 gives an overview on the radiation environment affecting ICs and the expected radiation effects. Section 4 also includes a list of the standards and handbooks that explain how the radiation levels can be calculated and the relevant modelling tools (e.g.

dose depth curves, 3D Monte Carlo, SHIELDOSE2, Geant4, Novice, SPENVIS or OMERE) and the physical parameters and units used to quantify these effects (e.g. LET threshold and SEU cross-sections).

Different ASIC and FPGA vendors offer different levels of (intrinsic) radiation protection, depending on their exact ASIC or FPGA family type, the choice of library cells and the package type.

Annex A provides the link to the several vendors of ASIC and FPGA technology that already incorporate radiation effects mitigation techniques in their technology and which either have acquired or are pursuing some level of qualification for use in space. These are examples, the list is certainly not complete, and it is of course subject to future updates as new company or institution provided solutions become available, and some technology or tools become obsolete or discontinued.

Sections 6, 7, 8, 9 and 10 describe some of the techniques that are often applied by ASIC and FPGA vendors but also by IC designers, at different levels, in order to achieve various levels of radiation hardness. The datasheets of these products normally indicate to the users/designers, what is the sensitivity per device or per cell inside the device, for a given typical orbit case or radiation profile. However, detailed information is often not contained in public datasheets, it can only be provided on request and under Non-Disclosure-Agreement (NDA). Users are therefore advised to contact the vendors to provide the necessary details over the actual radiation tests and results obtained when characterising the technology.

Mitigation introduced by the IC designer. In addition to selecting a base technology or existing part, additional mitigation that can be added by the IC designer (for new designs) is explained in sections 8, 11, 12 and 13.

All sections in the handbook try to summarise which are the costs and the added value of applying each method. Some concrete examples, including sometimes improvements on the failure rate, are provided for many of the proposed techniques. However, it is emphasised that the actual cost and benefit of each individual measure can strongly vary depending on technology, design, radiation environment and the implementation details. The effect is therefore to be evaluated for every individual case.

As Sections 14 and 15 explain, there are additional mitigation techniques that can be applied by the software and hardware system engineers. Moreover, many applications already contain an intrinsic fault-tolerance, e.g. the forward error correction present in many communication protocols. Together with technology selection and mitigation during IC-design, it is important to assess the system-level mitigation in a holistic approach, in order to determine the optimal strategy.

Technology selection and process level mitigation

6.1 Overview

Section 6 provides guidance for the selection or modification of existing processes in order to reduce the consequences of radiation in integrated circuits. Radiation-Hardening-By-Process (RHBP), as this approach is sometimes named, can be achieved by several means such as modifications of doping profiles in devices and substrates, optimization of deposition processes for insulators and use of specific materials. These techniques deal with two main effects: TID and SEEs. The effects of technology scaling for TID and SEE are discussed at the end of this section.

Solutions devoted to reduce the impact of TID focus on modifying insulator's properties and doping levels in active regions nearby interfaces. Currently, Shallow Trench Isolation (STI) is one of the main concerns for TID effects in CMOS technology, particularly the parasitic sidewall and top corner regions. Therefore, most of the presented techniques devoted to mitigate TID concern STI oxide.

SEEs are associated to instantaneous failures in active regions and thus can be mitigated by modifications of used materials and/or structures or by using alternative substrates such as Epitaxial layers, Silicon On Insulator (SOI) or Silicon On Sapphire (SOS).

A summary of mitigation techniques and the radiation effects they address are given in Table 6-1.

Table 6-1: Summary of mitigation techniques at manufacturing process level and the radiation effects they address

Mitigation techniques		Radiation effects			
		TID	SET	SEU	SEL
6.2.1	Epitaxial layers				X
6.2.2	Silicon On Insulator		X	X	X
6.2.3	Triple wells			X	X
6.2.4	Buried layers		X	X	X
6.2.5	Dry thermal oxidation	X			
6.2.6	Implantation into oxides	X			

6.2 Mitigation techniques

6.2.1 Epitaxial layers

6.2.1.1 Description of the concept

One alternative to bulk substrate is the substrate with an epitaxial layer. This technique consists in growing a thin monocrystalline film on the substrate. Because the substrate acts as a seed crystal, the deposited film takes on a lattice structure and orientation identical to those of the substrate.

Epitaxial layers are used in manufacturing processes both for Bipolar Junction Transistors (BJT) and modern CMOS Figure 6-1).

For radiation hardening, the main interest of epitaxial layers is in the reduction of the gain in the PNP thyristor parasitic structures that benefits from the lower substrate resistance. The epi layer acts as a higher resistivity barrier between the heavily doped P+ substrate and the N-well, thus reducing the risk of latch-up.

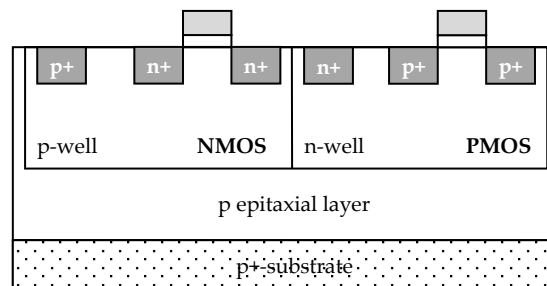


Figure 6-1: Example of epitaxial layer in CMOS technology

P-type epitaxial layer on P+ substrates is a common choice for latch-up mitigation, and it is important to tune and optimise this epitaxial layer.

6.2.1.2 Available test data (simulations, radiation testing, in-flight)

In the case presented in [12] the EPI layer needed to be thinner than 2.75μm to eliminate soft-error induced single event latchup. Other test cases are presented in [11].

6.2.1.3 Known issues (weaknesses, elements to be considered)

The efficiency of the epitaxial layer depends on:

- the control of the amount and uniformity of the deposition's resistivity and thickness,
- the cleanliness and purity of the surface and the chamber atmosphere,
- the prevention of the typically much more highly doped substrate wafer's diffusion of dopant to the new layers,
- the imperfections of the growth process,
- the protection of the surfaces during the manufacture and handling.

The brief summary of key characteristics for epitaxial layers is given in the Table 6-2.

Table 6-2: Summary of key characteristics for epitaxial layers

Abstraction level	Manufacturing process
Pros	Increase SEL hardness
Cons	Fabrication cost
Mitigated effects	SEL
Suitable validation methods	Ground accelerated tests

6.2.2 Silicon On Insulator

6.2.2.1 Description of the concept

6.2.2.1.1 Overview

The Silicon On Insulator (SOI) technology [14] is an alternative to bulk silicon substrates in CMOS semiconductor manufacturing. In Silicon On Insulator (SOI) fabrication process, transistors are implemented in a silicon layer, built over a silicon dioxide insulating layer (SiO_2), called Buried Oxide (BOX), (Figure 6-2(b-c)). This substrate architecture can improve device density and eliminates current paths to parasitic devices.

6.2.2.1.2 Fully/partially depleted SOI

Applying a positive voltage to a NMOS transistor's gate depletes the body of P-type carriers and induces an N-type inversion channel on the surface of the body. If the transistor body depth is thin, due to the insulator layer being close the substrate surface, then the transistor body can be fully depleted (Figure 6-2(c)).

On the other hand, if the insulated layer is thicker, the inversion region does not extend the full depth of the body, the volume is then said to be "partially depleted" (Figure 6-2(b)). In this case, the most buried part of the body is not depleted, and thus not connecting to anything. However it is coupled to the gate by the gate capacitance and to the source and drain by diode junctions. The voltage relies on the recent transistor electrical activity ("history effects") as described in [15].

6.2.2.2 Impact on radiation effects

6.2.2.2.1 SEL immunity

SOI inherently eliminates latch-up, which can occur in CMOS devices due to a parasitic condition in which at least one PNP and at least one NPN transistor act like a thyristor if turned on as a consequence of prompt dose event or a single event transient. Because the wells in an SOI device are completely oxide isolated, the parasitic thyristor effect cannot occur.

6.2.2.2.2 SET and SEU hardening

SOI's charge collection volume is about 10 times less than that of bulk silicon, so SOI is far less likely to experience bit-switching current pulses. Moreover, this inherent advantage can be improved upon by fabricating a connection to the body of a device that provides a place for ion charges to go to ground. This structure contrasts with most commercial SOI processes, which use a floating body and are less SEU resistant [16]. Commercial SOI generally avoids the body tie because it imposes a 30 percent area

penalty, but hardened SOI technology can substantially reduce this penalty by means of specialized techniques where the area penalty of body-ties can be reduced [285].

6.2.2.2.3 TID sensitivity

As seen before, SOI helps mitigating SEE. However, the BOX layer presents an additional insulator for charge trapping and a resulting intra-device leakage path along the bottom of the active silicon device layer.

Reference [17] presents how TID charge in partially-depleted device's BOX layer can reduce the back channel threshold voltage and increase leakage.

Reference [18] shows that the gate oxide and the BOX layer are electrically coupled through the fully depleted silicon body. In this case, trapped charge in the BOX can also cause shifts in the effective threshold voltage of the front gate. Since the silicon is so thin, it is not possible to increase the doping and maintain the fully depleted mode of operation. In this case, mitigation strategies involve either hardening of the BOX insulator (see section 6.2.6 implantation into oxide), or removal of the substrate and thinning or removal of the BOX layer [19].

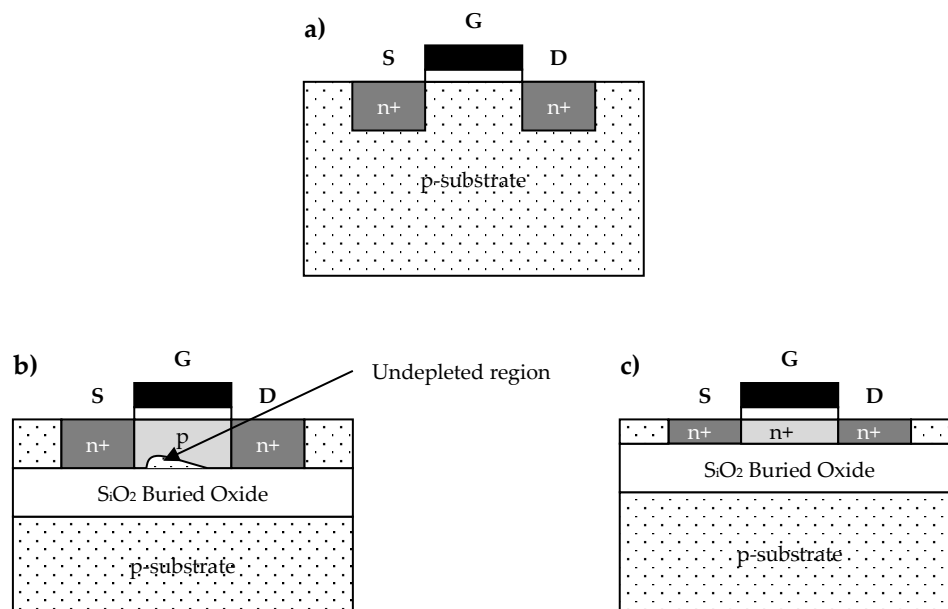


Figure 6-2: a) Conventional bulk NMOS transistor, b) Partially depleted SOI, c) Fully depleted SOI

As an example, Silicon On Sapphire (SOS) [20] is a hetero-epitaxial technique where a silicon film is grown on a sapphire (Al_2O_3) substrate. SOS was the first mature SOI technology [21], [22], [23], [24]. According to [17], until the 1980s, it was the only SOI technology able to produce LSI-VLSI circuits, such as for example microprocessors, SRAMs, gate arrays or ADCs.

Due to its inherent resistance to radiation, Silicon On Sapphire is mainly used in aerospace and military applications. One of the most important advantages of SOS, alike SOI, relies on the insulating layer which virtually eliminates the parasitic drain capacitance that is present in bulk silicon. Thus, it leads to an important improvement in transistor performance as this capacitor does not need to be charged and discharged on every cycle. This performance increase allows producing circuits with the same performance as bulk silicon ones but using less advanced manufacturing processes. Finally, another advantage of this technology is that it is manufactured using the same facilities than common bulk

silicon wafers. However, due to the high substrate weight, commercial facilities are often not able to produce such wafers.

SOS is produced by a more complex manufacturing process than bulk silicon. This reason, combined with the expensive sapphire substrate, prevents this technology from leaving specific applications like military and space applications or some RF devices.

6.2.2.3 Available test data (simulations, radiation testing, in-flight)

- The first SET and SEU experimental results obtained on SRAM devices processed with 2,5 μm partially depleted SOI technology showed error rates comparable to the ones of SOS and lower than those of bulk CMOS [25].
- The Soft Error Rate (SER) for an SRAM, developed with 0,35 μm partially depleted SOI technology (with body ties), was improved by 1,5 orders of magnitude at 1,5V with respect to the one of bulk CMOS SRAMs [26].
- Alpha-particles irradiation performed on a 4M-bit SRAM using a 0,1 μm partially depleted SOI technology with body ties, showed a SER two orders of magnitude lower for SOI than for bulk chips [27].
- Circuit simulations and experimental data were correlated in order to compare the intrinsic hardness of 0,25 μm SOI and bulk technologies [28]. The main conclusion is that bulk and SOI technologies optimized for consumer applications (non-hardened by the use of body ties) exhibit comparable LET threshold for SEU. Nevertheless, due to the smaller saturated cross-section (sensitive area), the SOI error rate is significantly lower than the bulk one, even in the worst case when the SOI supply voltage is lower than the one of bulk.
- A study reports the SER impact of process scaling over four technology generations (0,35, 0,25, 0,18 and 0,13 μm) and provides an experimental assessment of alpha and neutron SER [29]. The results show that SER is reducing on a per-bit basis in future technologies. For the 0,25 μm technology node, partially depleted SOI provides a reduction in SER over its bulk counterpart. However, for the 0,18 μm node, both bulk and partially-depleted SOI technologies are equally sensitive to neutron induced SER.
- A study explored the production and propagation of SETs in digital CMOS circuits [30]. Scaling trends to the 100 nm technology node are explored using three-dimensional mixed-level simulations, including both bulk CMOS and SOI technologies. Transients approaching 1 ns in duration are predicted in bulk CMOS circuits. Body-tied SOI circuits produce much shorter transients than their bulk counterparts, making them more amenable to transient filtering schemes based on temporal redundancy. Body-tied SOI circuits also maintain a significant advantage in single-event transient immunity with scaling.
- The proton response of a 0,35 μm SOI technology on UNIBOND material was investigated [31]. Threshold-voltage shifts of the front-gate and back-gate transistors are observed. The conclusion is that this technology can perform well in a proton-radiation environment.
- Body-ties effects on SEU resistance were analysed for a 0,2 μm fully depleted SOI SRAM [16]. 3D simulations revealed an increase in the threshold LET from 5,8 MeV/(mg/cm²) to 8,1 MeV/(mg/cm²).

6.2.2.4 Added value (efficiency)

Up to 30 % lower power consumption, 20 % higher performance and 15 % higher density than traditional bulk CMOS at the same feature size. The advantage of using an insulating layer is an increased performance by reducing the junction capacitance as the junction is isolated from the bulk

silicon. Moreover the decrease in junction capacitance also reduces the overall power consumption of the circuit.

6.2.2.5 Known issues (weaknesses, elements to be considered)

- If SOI improves SEU and SEL hardness, its buried oxide layer increases sensitivity to TID.
- The primary barrier to SOI implementation is the drastic increase in substrate cost, which contributes an estimated 10 % - 15 % increase to total manufacturing costs compared to bulk substrate device.

The brief summary of key characteristics for silicon on insulator is given in the Table 6-3.

Table 6-3: Summary of key characteristics for silicon on insulator

Abstraction level	Manufacturing process
Pros	Power consumption, performance, density Vs traditional CMOS
Cons	Substrate cost (+ 10-15%)
Mitigated effects	SEL (Immunity), SET and SEU
Suitable validation methods	Ground accelerated tests

6.2.3 Triple wells

6.2.3.1 Description of the concept

Hardening devices against Single Event Effects can be done by reducing charge collection at critical device nodes. This can be accomplished by introducing extra doping layers to limit substrate collection [11], [32]. In SRAMs, triple-well structures have been used to decrease SEU and SEL sensitivity [11], [12], [33].

In CMOS, both NMOS and PMOS transistors are used in association with P-wells and/or N-wells depending on the substrate doping and the process. We now describe three different well structures:

- The single-well process, illustrated in Figure 6-3 (a), uses an N-well to build a PMOS in a P-type substrate. This technology can make use of a heavily doped substrate, which increases the probability of having SEL due to PNP parasitic paths that use the low resistivity substrate.
- Twin-well process uses a lightly doped substrate that is either P-type with P-wells for NMOS transistors or N-type with N-wells for PMOS transistors (Figure 6-3(b)). This technology provides the basis for separate optimization of the NMOS and PMOS transistors, thus making it possible for threshold voltage, body effect and the channel transconductance of both types of transistors to be tuned independently. Because of the lightly doped substrate, thus providing a high resistivity zone, the risk of latch-up is decreased compared to the single-well process.
- In the triple well process, assuming a P-type substrate as illustrated in Figure 6-3 (c), the PMOS devices are constructed in a N-well (as in the single or double well process), however the P-well of the NMOS devices is constructed within a deep N-well (the third well). This means that both device types are isolated from the substrate by a reversed biased junction.

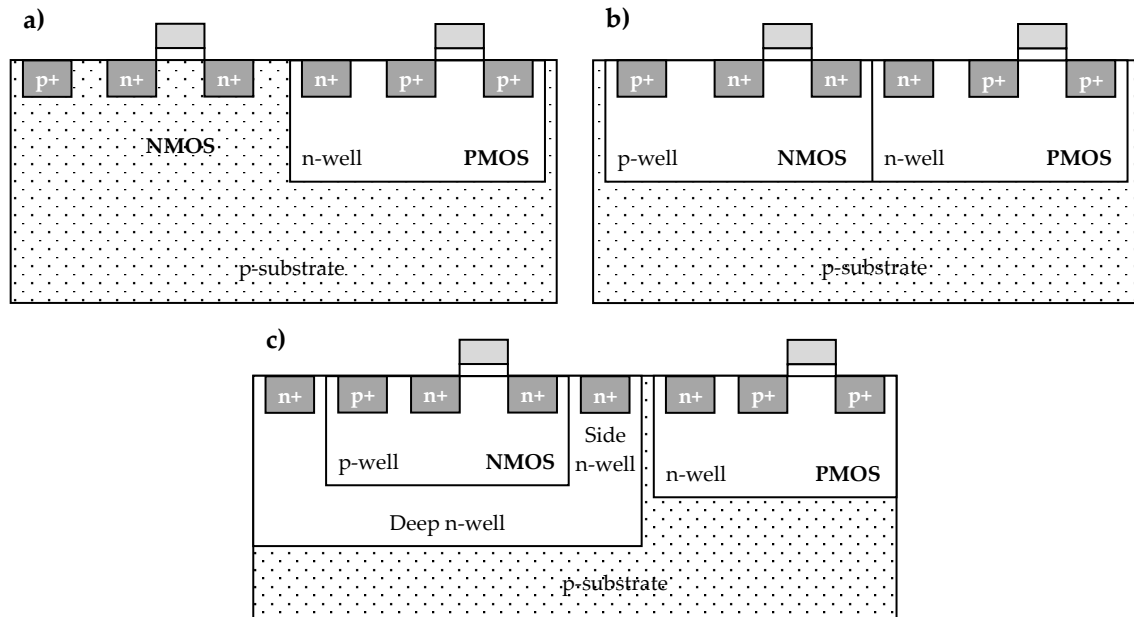


Figure 6-3: a) single-well technology, b) twin-well technology, c) triple-well technology implementing a deep n-well to isolate the p-well forming the NMOS from the substrate

6.2.3.2 Available test data (simulations, radiation testing, in-flight)

Triple well has been found to result in reduced alpha-particle and neutron Soft Error Rates (SER) in 130 nm and 90 nm latches and [11], [34]. A study [34] showed a 40 % lower SER (alpha & neutron) for SRAM and latches with triple well.

6.2.3.3 Known issues (weaknesses, elements to be considered)

- Triple-well has been demonstrated to increase the SER in 150 nm memory devices [35]. This study showed that lower triple-well implant energy produces a higher SER.
- Depending on the well doping and depth, and placement of well contacts, the triple well can increase the well resistance and exacerbate the single event response [12].
- This condition can also be problematic for dose rate photocurrents with the added junction areas. Retrograde wells and buried layers can also be used to provide an internal electric field that opposes collection of charge deposited in the substrate [36], [37].

The brief summary of key characteristics for triple wells is given in the Table 6-4.

Table 6-4: Summary of key characteristics for triple wells

Abstraction level	Manufacturing process
Pros	Increase SEU and SEL hardness
Cons	Increase manufacturing cost, in some cases SET can increase
Mitigated effects	SEU, SEL
Suitable validation methods	Ground accelerated tests

6.2.4 Buried layers

6.2.4.1 Description of the concept

Buried layers are, generally highly doped zones buried inside the well or substrate and placed beneath sensitive nodes, such as storage nodes, in order to collect or repel excess charge deposited by particles, diverting it from the devices on the surface.

The use of a buried layer of high doping in a lightly doped substrate is an alternative to the use of highly doped substrates [38]. The doping profiles and the presence of buried layers (which can include doped layers, insulating layers, or layers of modified material properties) can impact the radiation response of devices [11], and therefore it is important to consider this in the study of radiation effects and mitigation options. For example, an increase in the current necessary to trigger electrical latch-up results in an increase of Single Event Latch-up immunity.

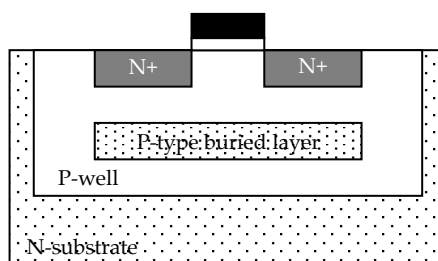


Figure 6-4: Schematic view of a P-type buried layer in a P-well

A few examples:

- In a vertical BJT structure, the use of a highly doped layer below the collector helps to confine prompt dose collection volumes, so that the base-collector junction current is much less than the collector-substrate junction [39].
- In addition to global buried layers, buried layers can be selectively added below device regions to optimize performance or for radiation effects mitigation. Examples include buried P+ layers (Figure 6-4) within the P-well [40] or an N-grid [41] to reduce alpha particle single event sensitivity. While buried layers in CMOS remain an effective strategy for latch-up mitigation, results of [11], [33], [12], [42] suggest limited effectiveness for mitigation of single event errors, and demonstrate that proper triple well designs can be a more effective strategy for advanced CMOS.
- A buried P+ layer below a deep trench isolated SiGe Heterojunction Bipolar Transistor (HBT) has been shown to reduce electrostatic discharge (ESD) and latch-up [43], and thus has been proposed

to reduce heavy ion charge collection [13]. Device simulation shows that the impact of the buried layer on the charge collection reduction happens at somewhat longer times [13].

- In GaAs technology, a buffer layer grown at Low Temperature (LT) during the epitaxial growth process causes the As to precipitate and form recombination sites, reducing the recombination lifetime in the layer beneath the active device [44]. While this is not a silicon device, the concept is interesting and can be applicable.

6.2.4.2 Available test data (simulations, radiation testing, in-flight)

Simulation of the device shows the impact of the buried layer on the reduction of charge collection happens at somewhat longer times [13].

6.2.4.3 Added value (efficiency)

Buried layers in CMOS are an effective strategy for latch-up mitigation.

6.2.4.4 Known issues (weaknesses, elements to be considered)

Buried layers offers limited effectiveness for mitigation of SER, results demonstrate that proper triple well designs can be a more effective strategy for advanced CMOS [11], [33], [12], [42]. Brief summary of key characteristics for buried layers is given in the Table 6-5.

Table 6-5: Summary of key characteristics for buried layers

Abstraction level	Manufacturing process
Pros	Increase SEL and SER hardness
Cons	Increase fabrication costs
Mitigated effects	SET, SEU, SEL
Suitable validation methods	Ground accelerated tests

6.2.5 Dry thermal oxidation

6.2.5.1 Description of the concept

As explained in section 6.1 the dominant problem provoked by TID is the net positive charge. Consequently, the general idea is either to increase electro trapping and to increase the overall quality of oxides or to reduce hole trapping. Trapping properties can be adjusted by modifying process recipe parameters (e.g. growth/deposition rates and times, temperatures, gas cocktail), or by pre-, co- or post-processing such as specialized implantation or annealing steps

A few examples:

- The growth temperature is an important parameter as it was demonstrated that hole trapping varies inversely with dry-oxygen growth temperatures over 900 °C - 1200 °C [45].
- Nitrogen incorporation during growth can degrade the TID hardness, while use of Argon instead does not degrade the hardness [45].
- Post Oxidation Annealing (POA), also dependent on ambient gasses, can alter the trapping properties, generally decreasing the hole trapping as long as the oxygen concentrations are high

enough. Otherwise, POA annealing in nitrogen can degrade the hardness more than POA in argon. POA in nitrogen also reduces electron traps. This is common practice for thermal oxides in commercial technologies; however not desirable for hardened technologies [45].

- Nitrogen implantation into silicon prior to oxidation improved the proton radiation hardness of oxynitride gate NMOS transistors [46].

These process parameters are verified by test. There are several other parameters that play a role during thermal oxidation, like defects due to contamination or internal wafer stress which could also impact the TID hardness. In addition, other oxidation processes applied during the back-end (e.g. CVD or PVD) could also have an impact in the final TID hardness of the oxides.

6.2.5.2 Available test data (simulations, radiation testing, in-flight)

The available test data presented in [45] and [46] showing impact of thermal oxidation process parameters on TID hardness is summarised in the Table 6-6.

Table 6-6: Impact of thermal oxidation process parameters on TID hardness

Process variable	Value	Impact
Temperature	1/T (900 °C < T < 1200 °C)	Hardness degradation (hole trapping increased)
Ambient gases	N Ar	Hardness degradation No hardness degradation
Post Oxidation Anneal	O N Ar	Hardness degradation Hardness degradation No hardness degradation
Pre-oxidation low energy N ₂ ⁺ implant	5 keV 10 ¹⁴ cm ⁻² < Fluence < 10 ¹⁵ cm ⁻²	Forms thin SiO _x N _y with improved proton TID hardness up to proton fluences of 10 ¹² .cm ⁻² (~7,5 Mrad)

6.2.5.3 Added value (efficiency)

Silicon Oxynitride gate NMOS transistors formed by nitrogen implantation into Silicon prior to radiation enhance proton induced TID up to fluencies of 10¹² cm⁻², corresponding to 7,5 Mrad.

6.2.5.4 Known issues (weaknesses, elements to be considered)

For some parameters that degrade hardness, see Table 6-7. The brief summary of key characteristics for dry thermal oxidation is given in Table 6-7.

Table 6-7: Summary of key characteristics for dry thermal oxidation

Abstraction level	Manufacturing process
Pros	Improved proton TID hardness
Cons	Increased fabrication cost
Mitigated effects	TID
Suitable validation methods	Ground accelerated tests

6.2.6 Implantation into oxides

6.2.6.1 Description of the concept

Implantation of elements, such as Al, Si, P, F and As, into oxides has been shown to improve the TID hardness primarily by increasing electron trapping [47], [48], [49].

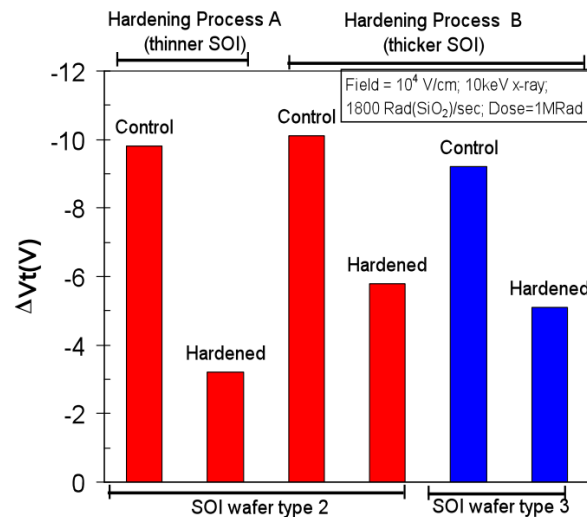


Figure 6-5: Radiation-induced back channel threshold voltage shifts for different SOI substrates types, SOI layer thickness and hardening process conditions [1]

SOI technology is presently used in many commercial applications, particularly microprocessors, and in some rad-hard CMOS applications. As presented in 6.2.2, SOI helps to mitigate single event effects. However the Buried OXide (BOX) layer presents an additional insulator for charge trapping. This can induce back-channel leakage in partially depleted SOI and front-channel threshold voltage shifts in fully depleted SOI. One strategy is hardening the BOX layer by the mean of Fluorine implantation into the BOX layer. This technique proved its efficiency by improving interface hardness and reducing the transconductance degradation [48]. Test results, illustrated in Figure 6-5, show that the hardening process reduces the radiation-induced threshold-voltage shift (ΔV_t) of the BOX layer by 45%-65% compared to the respective unhardened wafer counterparts [50].

6.2.6.2 Available test data (simulations, radiation testing, in-flight)

- Fluorine doping has been shown to improve the radiation hardness of gate and field oxides [48], [51].
- The TID degradation of current gain of lateral PNP transistors is reduced with As implanted SiO₂ passivation on the emitter base junction [48]. The use of SiC passivation has also been demonstrated to improve the TID hardness of bipolar transistors [52].
- Arsenic implanted SiO₂ reduces TID degradation in lateral PNP BJT [49]. However As in MOS gate oxides can be detrimental [53].

6.2.6.3 Known issues (weaknesses, elements to be considered)

- Hardness degradation was observed with As implantation in gate oxide [53].
- Boron doping (such as comes from the Boron gate doping in CMOS processes) has been shown to degrade the hardness [6], [54].
- Implantation of Si into oxide was shown to increase the electron trap density [55]. Subsequent analysis of the Si implanted oxides indicated that the mechanism for reduction of flatband voltage shifts is the formation of silicon nanoclusters in the oxide and proton trapping. Note that the analysis of [56] indicates that the reduction in shift with Si dose is due to proton trapping by Si nanoclusters, and not due to the electron traps which have a much smaller capture cross-section.

The brief summary of key characteristics for implantation into oxides is given in the Table 6-8.

Table 6-8: Summary of key characteristics for implantation into oxides

Abstraction level	Manufacturing process
Pros	Improved radiation hardness
Cons	Increased fabrication cost
Mitigated effects	TID
Suitable validation methods	Ground accelerated tests

6.3 Technology scaling and radiation effects

6.3.1 General

The impact of technology scaling on the response of integrated circuits to radiation effects cannot be evaluated only by taking into account the channel size and the geometry of the transistors. As explained in reference [57], studies have shown that differences in size and geometry affect the radiation-induced response of transistors in a non-consensual way. Moreover, the size and the geometry of the transistors are not the only parameters to be taken into account. Indeed, improving manufacturing processes does not strictly consist in reducing the size of the transistors. Change of materials (e.g. substrates) or new process techniques can twist the predictions. The effects of device scaling on soft-error rate depend on several competing factors. Among them the critical charge necessary to upset a memory bit is expected to decrease as depicted in early studies [58]. In fact, the increase of radiation effect immunity exists but is not less obvious [59]. Another factor to take into account is the charge collection depth which generally decreases with scaling, hence improving robustness of the circuits [61]. Power supply is also decreasing

with scaling which generally has a negative effect on radiation effect tolerance. A smaller transistors also means smaller sensitive volume and is, thus, less likely to be hit by a particle, which tends to increase its immunity. One of the advantages of reducing the transistor's channel length is that it allows increasing its switching speed. But increasing the frequency also implies increasing the probability of capturing a transient. Indeed, in low frequency systems most of the upsets are provoked by particles directly hitting the transistors, whereas in fast systems, upsets provoked by propagating SETs are important to take into consideration as they are not negligible anymore[60].

SEE sensitivity varies with technology scaling depending on the nature of the components. A general observation is that for most devices the sensitivity of a single bit was decreased over several generations of chips. However, this improvement is counterbalanced by the increase of density and thus, the overall sensitivity for a whole system has not changed or in some cases it has even increased.

6.3.2 Microprocessors

The main effect of heavy ions and protons on microprocessors is the upset in the internal memory cells. Since the last 15 years, the feature size of the CMOS transistors has been reduced by more than one order of magnitude but the LET threshold to generate an upset on these devices has remained unchanged [59]. However, the cross-section of the Power PC750 (0,25 μm) is one order of magnitude lower than the one of the Power PC603e (0,35 μm) while both are manufactured using thin epitaxial layers over highly doped substrates. Reference [59] also mentions that the decrease of the device size can potentially increase the upset rate in the terrestrial environment as the range of recoil atoms is increasing when devices become smaller and thus the energy level at which the device is upset is lower.

The study presented in reference [59] concludes on the fact that the cross-section generally decreases when devices become smaller but the rise of the frequency increases the cross-section. However, the magnitude of the frequency dependency decreases as the circuit becomes smaller.

6.3.3 DRAM memories

DRAM is currently one of the most robust devices in term of soft errors[10], [59]. The single bit sensitivity has been reduced by a ratio of about four or five per generation. This is attributed to the shrinking junction volumes, the relatively high node – capacitance and the relatively gradual voltage scaling. From the one-megabit to the one-gigabit DRAM generations, the DRAM cell single error sensitivity has been reduced by a factor of 1000, thus the overall DRAM system sensitivity has remained essentially unchanged. As frequency continuously increases, transient errors in bit lines and sense amplifiers around the memory cells become dominant in the next memory generations, thus soft error rate is expected to increase.

6.3.4 SRAM memories

Early SRAMs were more robust against SER because of high operating voltage and the fact that data was stored as the state of a bi-stable circuit made up of two large cross-coupled inverters, each strongly driving the other to keep the bit in its programmed state [10]. The evolution through successive generations of SRAM devices showed an increase of the single bit SER due to the shrinking of the cells volume, big reductions in operating voltage and reduction in node capacitance. This happened particularly in products using BPSG as a passivation layer [17]. Most recently, with technologies below 0,25 μm , the SRAM single bit SER has saturated and can tend to decrease due to the saturation in voltage scaling, reductions in junction collection efficiency and increased charge sharing due to short-channel effect. But, with the rise of the amount of embedded SRAM in electronics, the overall SRAM system SER is increasing significantly with technology scaling and has now become a significant reliability concern

[59]. Error Detection And Correction (EDAC) codes is the best means to mitigate memory soft errors but the system failure rates can be challenged by the SER in sequential logic.

6.3.5 Sequential and combinatorial logic

Flip-flops and latches are similar to SRAM cells (they use cross-coupled inverters) but are much more robust against SET because they are usually made of much larger transistors and they are designed with more transistors for each node. Their SER sensitivity tends to increase as the technology is scaled down [10], [59]. Soft errors in logic are a concern for high reliability systems when memory has been protected by error correction mechanism: the peripheral logic failure rate can be dominant. A significant increase in SER was shown with technology scaling from 0,18 μm to 0,13 μm . This trend is high enough to limit the efficiency of memory error correction.

In combinatorial circuits, radiation-induced charge can generate a short transient in the output which can propagate to the input of a latch or a flip-flop. For older technologies, this was quickly attenuated due to a large load capacitance and large propagation delays. In advanced technologies, with the decrease of the propagation delay, SETs can more easily go through many logic gates, thus increasing the latching probability. In technology nodes beyond 90 nm and at high operating frequencies, there is an increasing risk of soft errors due to latched SET events.