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Space engineering — Guidelines for electrical design and interface requirements for power supply

National foreword

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Space engineering - Guidelines for electrical design and interface requirements for power supply

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Raumfahrttechnik - Richtlinien für das elektrische Design und die Schnittstellenanforderungen von Stromversorgung

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European Foreword

This document (CEN/TR 17603-20-20:2022) has been prepared by Technical Committee CEN/CLC/JTC 5 "Space", the secretariat of which is held by DIN.

It is highlighted that this technical report does not contain any requirement but only collection of data or descriptions and guidelines about how to organize and perform the work in support of 16603-20.

This Technical report (CEN/TR 17603-20-20:2022) originates from ECSS-E-HB-20-20A.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CEN shall not be held responsible for identifying any or all such patent rights.

This document has been prepared under a mandate given to CEN by the European Commission and the European Free Trade Association.

This document has been developed to cover specifically space systems and has therefore precedence over any TR covering the same scope but with a wider domain of applicability (e.g.: aerospace).

Introduction

The power distribution by Latching Current Limiters, or LCLs, has been widely used in almost all European satellites for some decades as an effective way to achieve a very controlled and reliable load connection and disconnection from the satellite main bus, including power management in case of overload and load short circuit failures.

Additionally, power distribution by LCLs minimises inrush current events due to load filters charging (see section 5.7.2.3), and for this reason effectively allows the reduction of the loads filters themselves.

On the other side power distribution by LCLs has always been matter of “local” discussion and review, while no attempt has been done so far to collect all the available information in a congruent and explanatory handbook and to allow a product-oriented specification as presently done with ECSS-E-ST-20-20.

This handbook complements ECSS-E-ST-20-20, and it is directed at the same time to power system engineers, who are specifying and procuring units containing LCLs for power distribution and protection, and to power electronics design engineers, who are in charge of designing and verifying power distribution by LCLs.

For the system engineers, this document explains the detailed issues at circuit level and the impacts of the requirements for the design of LCLs.

For design engineers, this document gives insight and understanding on the rationales of the requirements on their designs.

It is important to notice that the best understanding of the topic of Power Distribution based by LCLs is achieved by the contextual reading of both the present handbook and the ECSS-E-ST-20-20.

Note that the present issue of the handbook covers electrical design and interface requirements for power distribution based on Latching Current Limiters only.

Future issues of the present handbook will cover additional power interfaces.

1

Scope

In general terms, the scope of the consolidation of LCLs power distribution interface requirements in the ECSS-E-ST-20-20 and the relevant explanation in the present handbook is to allow a more recurrent approach for the specific designs offered by power unit manufacturers, at the benefit of the system integrators and of the Agency, thus ensuring:

- better quality,
- stability of performances, and
- independence of the products from specific mission targets.

A recurrent approach enables power distribution manufacturing companies to concentrate on products and a small step improvement approach that is the basis of a high quality industrial output.

In particular, the scope of the present handbook is:

- to explain the principles of operation of power distribution based on LCLs,
- to identify important issues related to LCLs, and
- to give some explanations of the requirements set up in the ECSS-E-ST-20-20 for power distribution based on LCLs, for both source and load sides.

2 References

EN Reference	Reference in text	Title
EN 16601-00-01	ECSS-S-ST-00-01	ECSS system - Glossary of terms
EN 16603-20-20	ECSS-E-ST-20-20	Space engineering - Electrical design and interface requirements for power supply
EN 16602-30-02	ECSS-Q-ST-30-02	Space product assurance - Failure modes, effects (and criticality) analysis (FMEA/FMECA)
EN 16602-30-11	ECSS-Q-ST-30-11	Space product assurance - Space product assurance, Derating – EEE components
	ESA PSS-02-10 Vol.1 Issue 1, Nov. 1992	Power standard
	IEEE CFP13APE-USB (2013)	MOSFET Gate Open Failure Analysis in Power Electronics, IEEE Applied Power Electronics Conference and Exposition, Long Beach, California, 17-21 March 2013, pp. 189-196 (reported as Annex G in the present HB)
	ESA SP-719 (2014)	Approach to design for stability a system comprising a non-ideal current source and a generic load, 10th European Space Power Conference, Noordwijkerhout, The Netherlands, 13-17 May 2014 (reported as Annex H in the present HB)
	ESA SP-719 (2014)	LCL current control loop stability design, 10th European Space Power Conference, Noordwijkerhout, The Netherlands, 13-17 May 2014 (reported as Annex I in the present HB)

Terms, definitions and abbreviated terms

3.1 Terms from other documents

- a. For the purpose of this document, the terms and definitions from ECSS-S-ST-00-01 apply, in particular for the following terms:
1. **redundancy**
 2. **active redundancy**
 3. **hot redundancy**
 4. **cold redundancy**
 5. **fault**
 6. **fault tolerance**
- b. For the purpose of this document, the terms and definitions from ECSS-E-ST-20-20 apply.

3.2 Abbreviated terms

For the purpose of this document, the abbreviated terms from ECSS-S-ST-00-01 and the following apply:

Abbreviation	Meaning
A	analysis
BJT	bipolar junction transistor
EOL	end-of-life
ESTEC	European Space Technology and Research Centre
I	inspection
LCL	latching current limiter
MFET	MOS field effect transistor
MOS	metal oxide semiconductor
OVP	overvoltage protection
PCDU	power conditioning and distribution unit
PDU	power distribution unit
RDS_{ON}	drain source resistance in on state (for MFET)
RLCL	retriggerable LCL

Abbreviation	Meaning
RoD	review of design
S3R	sequential unit switching regulator
SOA	safe operating area
SPFF	single point failure free
T	test
TWTA	travelling wave tube amplifier
UVP	undervoltage protection
WCA	worst case analysis

4

Explanations

4.1 Explanatory note

The present handbook refers to the electrical interface requirements defined in the ECSS-E-ST-20-20.

The ECSS-E-ST-20-20 requirements are referred to in this handbook by using following convention and are indicated in *italic font*:

[requirement number] feature - sub-feature.

For example:

Requirement 5.2.3.2.1a.

Clause Heading 3 title = "Current Limitation Section"

Clause Heading 4 title = "Switch element, positions"

→ *[5.2.3.2.1.a.] Current Limitation Section – Switch element, position*

See also, for more information, Annex A of ECSS-E-ST-20-20.

In addition:

- each requirement (i.e. any statement containing a “shall” in the standard) is marked with **red text**.
- each recommendation (i.e. any statement containing a “should” in the standard) is marked with **blue text**.

Keywords are highlighted in **bold**. A keyword is a word that either has a special meaning in the contest of the chapter in which it appears, or highlight a concept.

4.2 How to use this document

For the best utilisation of this document, it is recommended to print it together with the ECSS-E-ST-20-20 and to consult Annex A, Annex B and Annex C separately and at the same time when reading the document core.

In this way, the discussion and the rationale explanation of each individual requirement are clearer and there is the minimum risk of misunderstanding.

Power distribution by LCLs/RLCLs

5.1 General architecture

A generic architecture for a Latching Current Limiter, or LCL, is shown in Figure 5-1.

Note that the diagram in Figure 5-1 is given only as a reference, without losing generality, and some of the features thereby reported can be actually realised differently.

Common LCL design alternatives are discussed further in section 5.2.

Without losing in generality, the general architecture is hereby explained for the distribution by LCLs.

For the specific case of Retriggerable Latching Current Limiter, or RLCL, refer to section 5.3.

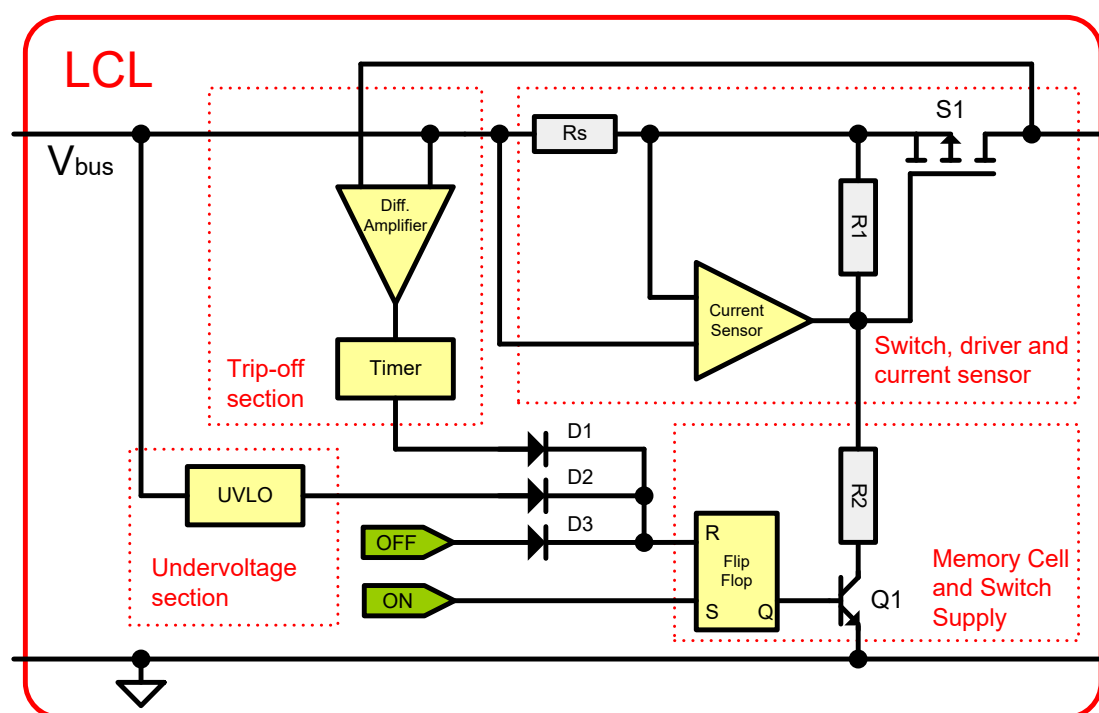


Figure 5-1: LCL generic block diagram

The Latching Current Limiter, or LCL, is a switch-able, latching, retriggerable over-current/overload protection placed between a power source and the relevant load.

The LCL can be commanded ON and OFF and its status is normally latched by a relevant memory cell.

Typically, an LCL presents a minimum residual resistance between power input and power output during nominal operation (i.e. when the switch is commanded closed).

In case of an overload, e.g. when the load current request exceeds a prefixed threshold, the LCL enters current limitation and a time counter is activated.

If the overload condition persists for a given time duration (called trip-off time), the time counter commands the LCL OFF.

Normally there should be an external command activation to reset the LCL into its original ON state.

Note that the LCL identifies a function: therefore it is independent from the number of power switches or MOSFETs used to implement the function itself.

The functionality of the LCL, in relation to the block diagram in Figure 5-1, is detailed in section 5.2.

5.2 Functionality

5.2.1 Overview

The basic elements of an LCL are the following:

- the section containing **the switch, the driver and the current sensor**,
- the section relevant to the **trip-off** timer,
- the section relevant to the **memory cell and switch supply** section,
- the **undervoltage protection** (UVP) section,
- the **auxiliary supply** section (not shown in Figure 5-1), and
- the **telemetry** section.

Each basic element is discussed in a dedicated section in the present chapter.

5.2.2 Switch, driver and current sensor

The switch is generally constituted by an enhancement MFET, either P or N channel, even though other devices could be used (for example, bipolar transistors for lower current applications).

It is called “switch” in relation to the switching capability of the LCL (e.g. it can apply or remove power from the load), but actually it operates either in ohmic “ON” mode or in linear mode according to the load current being below or above a specified threshold.

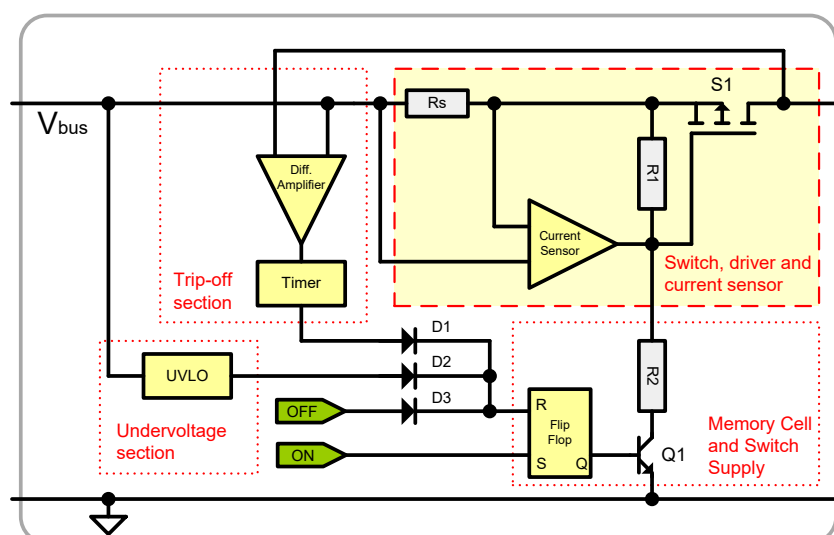


Figure 5-2: Switch, driver and current sensor

It is to point out that the **switch** and the **current sensing resistor** (or sensing element), is not placed on the power line connected to ground: this is a **mandatory** feature if the LCL power output is distributed outside the unit containing the LCL itself (as it happens on the main bus protected outputs in the power system Distribution Unit or PDU). The reason is that the power output lines need to be protected versus accidental short circuit to ground due to failures in the connectors, in the harness, or in the supplied load.

[5.2.3.2.1.a] Current limitation section – Switch element, position

[5.2.3.3.1.a] Current limitation section – Current sensing element, position

The relevant **switch driver** is usually inherently included in the same circuit implementing the **current sensing** feature: when the LCL is commanded ON, the switch is normally in ohmic “ON” mode and presents either a low ohmic characteristic (for MFETs, ON channel resistance, or $R_{DS(ON)}$) or anyhow a low voltage drop (as in the case of a BJT switch).

[5.4.5.1.1.a], [5.4.5.1.1.b], [5.4.5.1.1.c] Voltage drop – Voltage drop

In case of an overload, it is necessary that the switch is **quickly** brought outside ohmic “ON” mode condition and into linear one, in order to reduce the relevant surge current conditions (causing also relevant system EMC conducted and radiated disturbances) and the switch power/thermal stress.

The speed of response is function of the MFET gate charge and it is a figure of merit of the current sensing circuit.

[5.4.1.1.1.a], [5.4.1.1.1.b], [5.4.1.1.1.c], [5.4.1.1.1.d], [5.4.1.1.1.e], [5.4.1.1.1.f] Overall requirements - Current overshoot

The current sensor is in charge of regulating the current in overload situation, by modulating the gate voltage of the switch: the accuracy of the gate voltage is function of the current sensing circuit and the relevant reference voltages used in the design.

[5.2.1.1.1.a], [5.2.1.1.1.b] HLCL/LCL class – HLCL/LCL class

[5.2.2.1.1.a] RLCL class – RLCL class

[5.2.3.1.1.a] Current limitation section - Range

In case more than one MOSFET is used, it is important to have a dedicated current control per MOSFET to ensure current sharing in limitation.

If two or more MOSFETs are used in parallel with one single limiter, each MOSFET should be able to handle the total limitation current.

The current sensor is also sometimes used to derive a current telemetry signal, which is normally referred to ground.

An important observation is that the LCL/RLCL needs to contain a provision to circulate (free-wheel) the current circulating in the load (or harness) inductance, when the LCL/RLCL is either commanded OFF or it opens the line after an overload.

This is normally achieved by placing an anti-parallel diode to the output of the LCL itself.

[5.2.7.7.1.a] Conditions at start-up/switch-off – switch-off

5.2.3 Trip-off section

5.2.3.1 Overview

The LCL trip-off section is in charge to start the “counting” of the overload condition duration, and to set the LCL status to OFF after the relevant trip-off time has elapsed.

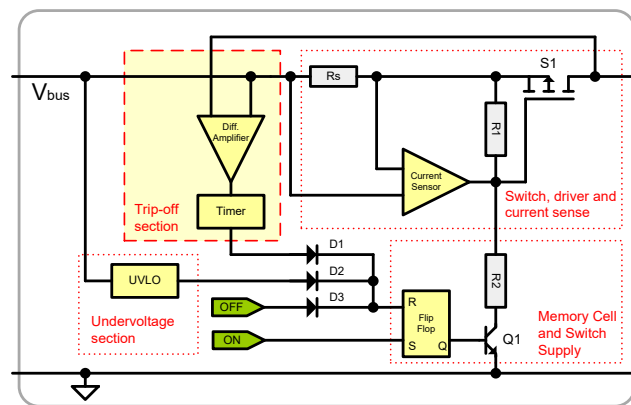


Figure 5-3: Trip-off section

[5.2.1.1.1.a], [5.2.1.1.1.b] LCL/HLCL class – LCL/HLCL class

NOTE Specifically minimum and maximum trip-off time.

[5.2.2.1.1.a] RLCL class – RLCL class

NOTE Specifically minimum and maximum trip-off time.

[5.2.4.1.1.a] Trip-OFF section - Range

It can be triggered by a signal coming from the current sense section, which identifies that the current limitation has been entered as a consequence of an overload, or by the differential reading of the voltage across the switch (as shown in Figure 5-1).

When the differential voltage across the switch is over a prefixed threshold, a timer is started to count the trip-off time.

The timer is usually implemented by means of a simple resistive-capacitive (RC) element in combination with a comparator, or a digital counter/comparator.

If the timer is implemented by a RC low-pass filter, the voltage across the capacitor mimics the temperature developed at the junction of the LCL MFET switch under current limiting conditions.

To understand this concept, it is useful to think of the electrical equivalence of a thermal network (see following Table 5-1 and Figure 5-4).

Table 5-1: Thermal electrical network equivalence

Electrical domain		Thermal domain	
Current	A	Power	W
Voltage	V	Temperature	°C
Resistance	Ohm	Thermal Resistance	°C/W
Capacity	F	Thermal Capacity	J/°C

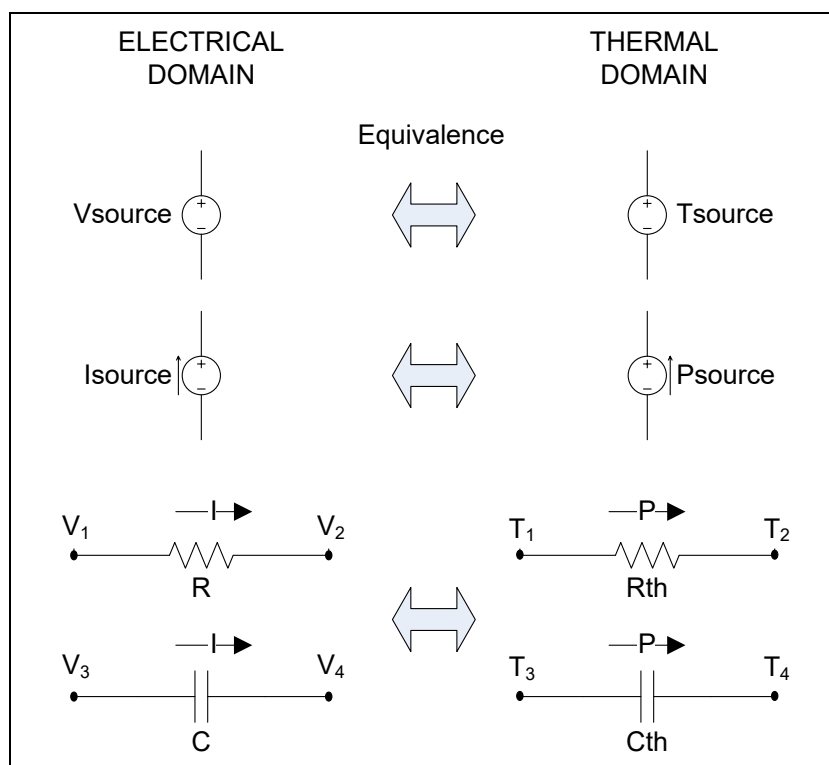


Figure 5-4: Thermal electrical network equivalence

When the timer predefined trip-off time duration is elapsed, the LCL is switched OFF.

A time diagram illustrating the qualitative current profile of an overload event is shown in Figure 5-5.

We can identify two different modes of operation for the current limitation:

- the first current limitation mode occurs when an LCL is enabled with a command and then starts to charge the input filter capacitance in the load (Figure 5-6, right). In this case a negligible overshoot in the current profile can be expected and achieved.
- the second case (Figure 5-6, left) is when the LCL is enabled and a sudden overload like a short circuit occurs (in this case, a larger current overshoot can occur).

The specification and understanding of these two cases are important to clarify when compatibility tests and analyses are made on real hardware at equipment level.

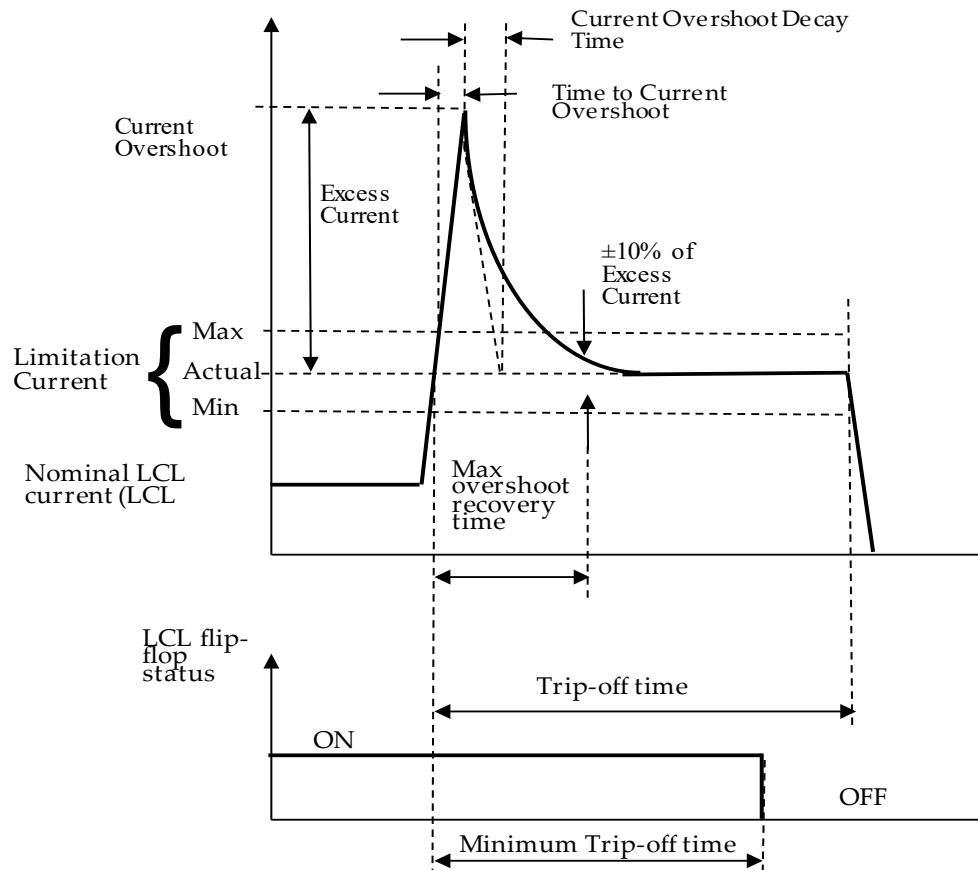


Figure 5-5: LCL overload timing diagram

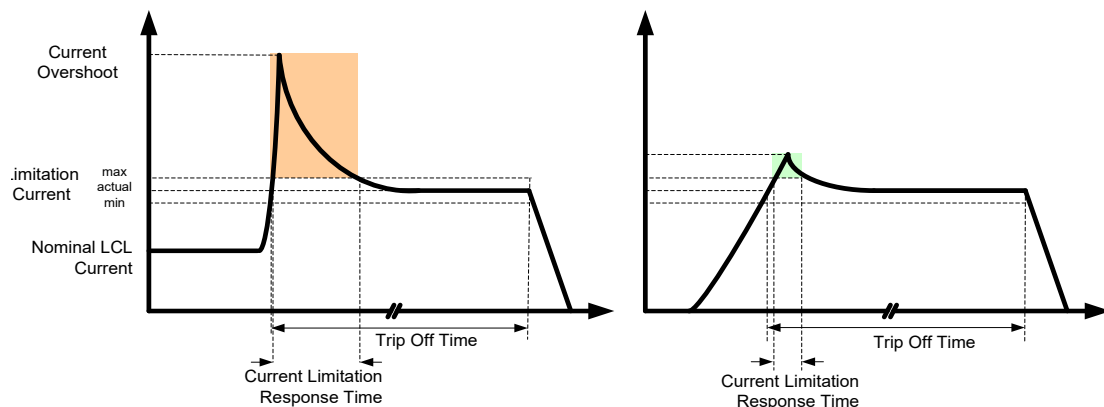


Figure 5-6: Comparison between nominal turn ON (right) and overload caused by a short circuit (left)

With respect to Figure 5-5, the minimum trip-off time is evaluated with respect to the flipping action of the relevant LCL memory cell (state flip-flop) and not with respect to the actual decay of the current from limitation value to zero: in fact, and depending on the adopted design solution, there can be a non-negligible delay before the LCL delivered current decays to zero and after the LCL memory cell has been commanded OFF by the relevant trip-off section.

This specific issue needs indeed a careful consideration during LCL design phase.

5.2.3.2 Verification

In case the trip-off is triggered by the differential voltage across the switch it should be verified that the switch dissipation/temperature is acceptable when the LCL is in limitation but the differential voltage threshold V_{diff} is not crossed (considering the worst case threshold value).

In this case the switch can continuously dissipate $V_{diff_max} \times I_{limitation_max}$.

5.2.4 Memory cell and switch supply section

The memory cell and switch supply section contains the “memory” of the LCL, which is by definition a latching function and therefore is characterised by two states (ON and OFF).

The circuit implementing this section is also designed to provide a predefined LCL status at start-up (e.g. when the bus voltage is ramped up).

The predefined LCL status at start-up should be OFF (while it is ON for a RLCL – see section 5.3).

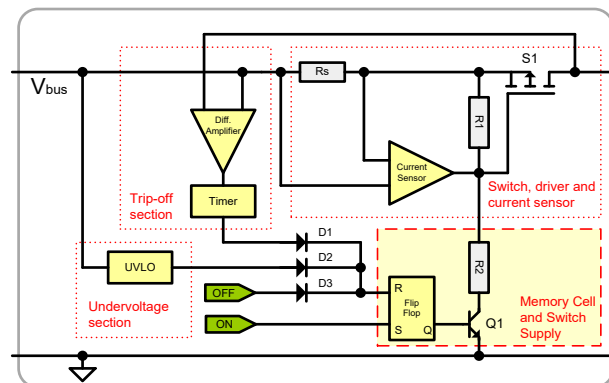


Figure 5-7 : Memory cell and switch supply section

The memory cell usually provides the signal enabling the supply of the switch, current sensor and switch driver that normally are referred at the hot side for the reasons explained in section 5.2.2.

The design of the switch supply is done in a way that the rate of rise (respectively fall) of the output current is within the specified limits during power up after command ON application (respectively power down after command OFF application).

The reasons to limit the current slope are essentially for reducing EMC interference (both conducted and radiated) and to have clear, reproducible conditions to ensure that no unwanted status change is caused by LCL activation or deactivation (especially after satellite integration).

[5.4.2.1.1.a] Start-up / switch-off requirements - Start-up current rate

[5.4.2.2.1.a] Start-up / switch-off requirements - Switch-off current rate

Increasing component densities and number of layers on PCBs make cross talk issues more and more difficult to deal with. Cross talk can occur between tracks when high dv/dt or di/dt are present and the distance between tracks is small. Typically, the design of the PCB should guarantee that power tracks, driver and current sense section tracks and sensitive signal tracks are sufficiently separated, such as any unwanted behaviour (such as spurious protection activation) is avoided.

5.2.5 Undervoltage protection section

The undervoltage protection section, or UVP, is provided to avoid the LCL from being switched ON when the MB voltage is below a critical threshold, and to switch it OFF in case of an abnormal low value of the MB voltage.

By switching the LCL OFF, the load is disconnected from the bus automatically: in this case, the bus itself can restore its nominal value in case the reason for the undervoltage events is a power deficit between the source capability and the load demand.

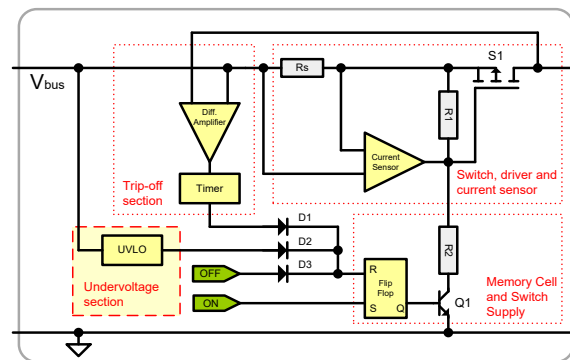


Figure 5-8 : Undervoltage protection section

Usually, when LCLs are used in the main bus power distribution, the UVP feature is used as the last resort to recover the bus to its nominal range (while higher main bus voltage thresholds for load shedding are usually managed by the on-board computer and software).

It is to point out that the UVP is also needed to ensure that no load enters unpredictable operation or reaction due to abnormally low power supply voltage.

[5.2.5.1.1.a] Undervoltage protection section - provision

The normal functioning of the LCL UVP is to operate on the relevant memory cell, e.g. to command the LCL in OFF state, in a way that an external command is needed to switch it ON again.

This is the normal implementation to avoid an uncontrolled “hiccup” mode of operation due to bus overload conditions: if the UVP is not latching, and a bus overload occurs, the bus voltage decreases, the UVP disables the LCL and therefore removes the overload, the bus voltage increases to its nominal range, the UVP becomes inactive and the overload condition reappears, etc.

[5.4.3.1.1.a] UV protection - Switch-off threshold, regulated bus

[5.4.3.2.1.a] UV protection - Switch-off threshold, unregulated bus

[5.4.4.1.1.a] Switch-on capability - Enable ON threshold Voltage, regulated bus

[5.4.4.2.1.a] Switch-on capability - Enable ON threshold Voltage, unregulated bus

The specified ranges for UVP switch-off threshold and LCL enable ON threshold voltages are intended as the envelope that the standard product of a power subsystem manufacturer need to be able to offer. The actual threshold values are normally established based on the specific mission needs.

For unregulated bus case, it is definitively necessary to provide the UVP with hysteresis to avoid uncontrolled “hiccup” mode for RLCLs or for LCLs that are not latched OFF after a trip-off event, while on a regulated bus the normal configuration is just to switch-off the LCL once the switch-off threshold is reached (and therefore it might not be necessary to implement a relevant hysteresis).

[5.2.5.2.1.a], [5.2.5.2.1.b] Undervoltage protection section - unregulated bus case

[5.4.3.5.1.a] UV protection – UV protection hysteresis

To avoid that the UVP is triggered by noise or by bus voltage transients, some noise immunity is implemented. The specified noise immunity value is usually not critical.

The generic UVP timing diagram, explaining the relevant noise immunity requirements and UVP operation, is given in Figure 5-9.

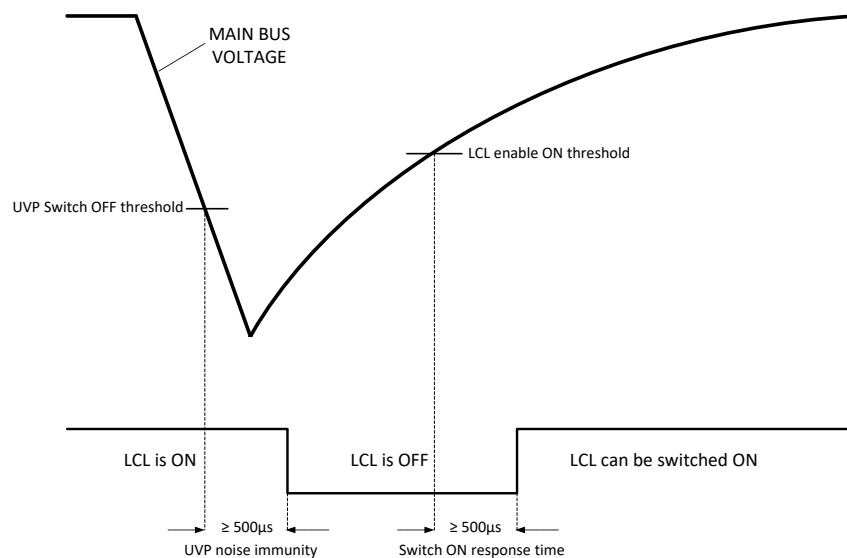


Figure 5-9, UVP timing diagram

In any case, the UVP activation timing is also of importance. A minimum activation delay is necessary at least for regulated buses, to avoid spurious switch-off in case of transients. In addition, at bus recovery, some noise immunity is also considered. The behaviour of the system is analysed considering that some LCL could have been tripped OFF by UVP and others not (depending on the bus transient).

[5.4.3.3.1.a] UV protection - UV protection noise immunity

[5.4.3.4.1.a] UV protection - UV protection noise immunity, verification

[5.4.4.3.1.a] Switch-on capability – Switch-on response time, value

[5.4.4.4.1.a] Switch-on capability – Switch-on response time, verification

The UVP feature is sometimes proposed as a **centralised** function (i.e. serving many LCLs) in addition or opposed to a **distributed** function, (i.e. local to each individual LCL).

In this case, a centralised UVP detector sends a command OFF to a number of LCLs.

If centralised, the UVP needs to be implemented as a Single Point Failure Free (SPFF) feature, e.g. no single failure should cause the deactivation of all the served LCLs. The reason is that even a non-permanent failure could happen in a critical operational time of the spacecraft and induce a heavy or

catastrophic consequence. This is why cold redundant circuits are generally not preferred for this function.

[5.2.5.3.1.a] Undervoltage protection section - Centralised protection

The centralised UVP protection is more critical and risky than the decentralised one, and the relevant advantage in terms of components used must be traded against all necessary redundancies and features like majority voting circuits.

5.2.6 Auxiliary supply section

The auxiliary supply section (not shown in Figure 5-1) is dedicated to the supply of the LCL functions.

Some of the LCL functions (typically, the current sensor and switch driver) are usually self-supplied by the bus voltage, at least for voltages up to 50V.

The other functions normally require one or more supply lines that can be **locally** derived from the LCL power input lines by means of dedicated power supplies, or could be **centralised**, e.g. serving many LCLs (even though centralisation normally increase the chances of common failure paths and therefore it could be less appealing).

In this case, the auxiliary power supplies (in active redundancy) are normally implemented as a Single Point Failure Free (SPFF) feature, e.g. no single failure causes the deactivation of all the served LCLs.

5.2.7 Telemetry section

5.2.7.1 Status telemetry

The LCL status is an important telemetry information: combined with the current telemetry (see section 5.2.7.2), it can be used to determine if failures are present in the power subsystem or in the load, and allow debugging and isolation of failures in flight.

The detailed explanation of the proposed ECSS-E-ST-20-20 requirements is presented in section 5.7.3.5: the proper definition of what the status signal represents allows the complete understanding of possible failure modes and allows a straight forward fault detection and recovery by the satellite operator.

5.2.7.2 Current telemetry

5.2.7.2.1 Overview

The current telemetry provides a low-level signal proportional to the current flowing on the hot distribution line of the LCL/RLCL.

The current telemetry is provided for main bus distribution, in order to give the satellite operator the information of the consumption of the relevant load.

[5.2.8.2.1.a] Telemetry section - Current telemetry

The current telemetry normally provides a full-scale reading up to the LCL/RLCL nominal limitation current, is linear and comes with a specified accuracy.

[5.2.8.3.1.a] Telemetry section - Current telemetry, full scale reading

[5.2.8.4.1.a] Telemetry section - Current telemetry, linearity and accuracy

The current telemetry meets a maximum offset specification and it is possible to read down to zero current without affecting the relevant accuracy.

[5.2.8.5.1.a] Telemetry section - Current telemetry, offset

[5.2.8.6.1.a] Telemetry section - Current telemetry, reading at zero current

The capability of the current telemetry to read down to zero current can be easily implemented by allowing a positive telemetry output offset (in case of a single telemetry circuit supplied by a single line with respect to ground). This solution has the advantage to remove the systematic telemetry error at low current due to the typical telemetry circuits output offset voltage (for example, due to operational amplifiers).

5.2.7.2.2 Verification

Current TM performances are verified by analysis and test, on a minimum number of points.

[5.2.8.7.1.a] Telemetry section - Current telemetry, verification

5.3 Retriggerable Latching Current Limiter case

The Retriggerable Latching Current Limiter, or RLCL, is an LCL including additional features.

It is basically an LCL not provided with an OFF command, which is set in any case in ON condition during start-up, and performing an automatic start-up, repeated switch-on sequence after an overload occurred, as long as the overload is present; in case the overload is removed, the RLCL automatically ends up in ON conditions, e.g. delivering power to the load.

The RLCL is normally used for supplying essential satellite loads, e.g. the ones that are essential for mission success (e.g. receivers and decoders).

An example of RLCL timing diagram is given in Figure 5-10.

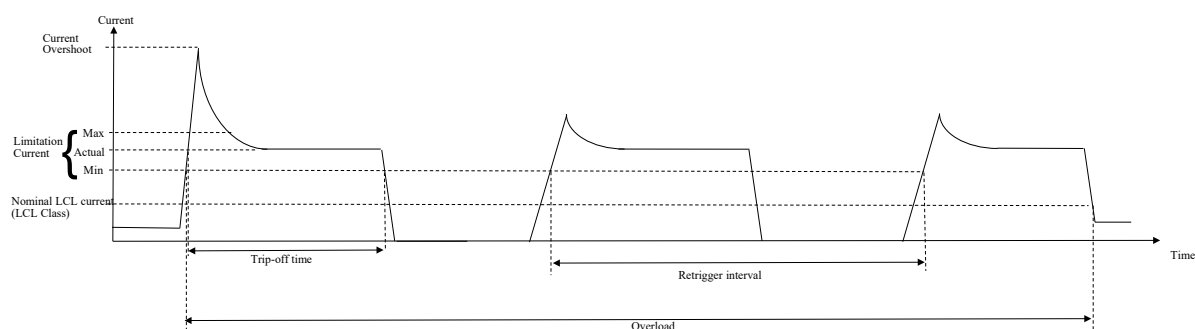


Figure 5-10: RLCL overload timing diagram

The RLCL retrigger rate in overload conditions is determined by design to respect the required stress limitations (derating) on the relevant RLCL switch; the RLCL retriggerability can be disabled under special circumstances should the load be acknowledged as definitively failed.

In any case, to allow the isolation of essential loads that can present an overload and malfunction, causing not allowable perturbations at spacecraft level, it is convenient to allow the possibility of enable or disable the retrigger function of an RLCL.

[5.2.6.2.1.a] Telecommand section feature - Retrigger function