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Surface mounting technology

Part 5-1: Surface strain on circuit boards — Strain gauge measurement applied to chip components

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Surface mounting technology –
Part 5-1: Surface strain on circuit boards – Strain gauge measurement applied to chip components

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Part 5-1: Surface strain on circuit boards – Strain gauge measurement applied to chip components

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The text of this Technical Report is based on the following documents:

Draft	Report on voting
91/1915/DTR	91/1927/RVDTR

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Report is English.

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This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 61760 series, published under the general title *Surface mounting technology*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn, or
- revised.

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INTRODUCTION

This Technical Report applies to electronic and electromechanical circuit board assemblies and describes current best-practices for dealing with mechanical stress induced cracks in the body of surface-mount ceramic components soldered onto circuit boards.

Circuit boards are becoming smaller and thinner, design margins are decreasing, and components are becoming more sensitive to mechanical stresses. In consequence in-depth strain control on a circuit board is getting more and more important to prevent mechanical damage to components.

This Technical Report is an informative document which serves to illustrate the technically feasible options and provides a basis for customer and supplier discussions and agreements. It is based on many years of experience of component manufacturers and users in measuring surface strain on circuit board surfaces during various assembly processes. It is not intended to be regarded as a specification or standard. Formulations and data expressed in the form of provision such as requirements or recommendations do not claim to be provisions and are just suggested as the results of the discussion.

Related standards are gathered in the bibliography.

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SURFACE MOUNTING TECHNOLOGY –

Part 5-1: Surface strain on circuit boards – Strain gauge measurement applied to chip components

1 Scope

This document describes examples of methods using electrical strain gauges for determination of critical mechanical stresses in assembly processes. These stresses can damage chip type ceramic components, causing so called “bending cracks”. Area-array components are excluded from the scope of this document.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194-2 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
- ISO Online browsing platform: available at https://www.iso.org/obp

3.1
principal strain
maximum and minimum normal strains in a plane, always perpendicular to each other and oriented in directions for which the shear strains are zero

3.2
maximum principal strain
maximum value of principal strain developed in the component body

Note 1 to entry: Failure of a material or component will occur when the maximum principal strain developed in the body exceeds the limiting value of strain for a certain component.

4 Damaging mechanisms of chip type ceramic components

4.1 Surface strain by board bending

When a board is bent, lands are pulled outwards and generate mechanical stress on the solder-joints, electrodes or components (Figure 1, Figure 2). This mechanical stress causes defects, for example a bending crack in a ceramic capacitor (Figure 3). The root cause of this defect is the local strain at the surface on which the component is mounted.

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