



BSI Standards Publication

EMC IC modelling

Part 4-1: Use of ICIM-CI model to predict the IC conducted immunity in a PCB

National foreword

This Published Document is the UK implementation of IEC TR 62433-4-1:2025.

The UK participation in its preparation was entrusted to Technical Committee EPL/47, Semiconductors.

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Published by BSI Standards Limited 2025

ISBN 978 0 539 21847 3

ICS 31.200

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This Published Document was published under the authority of the Standards Policy and Strategy Committee on 31 August 2025.

Amendments/corrigenda issued since publication

Date	Text affected
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TECHNICAL REPORT

**EMC IC modelling -
Part 4-1: Use of ICIM-CI model to predict the IC conducted immunity in a PCB**



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CONTENTS

FOREWORD	3
1 Scope	5
2 Normative references	5
3 Terms, definitions and abbreviations	5
3.1 Terms and definitions	5
3.2 Abbreviated terms	6
4 Philosophy	7
5 ICIM-CI model extraction flow	7
5.1 General	7
5.2 Failure criteria definition	9
5.3 PDN extraction	10
5.3.1 General	10
5.3.2 PDN extraction from SYZ-parameters measurements	11
5.3.3 PDN extraction from existing models	13
5.3.4 PDN extraction from package geometry import and simulation model generator	14
5.4 Conducted immunity characterization	15
5.5 IB extraction	18
5.6 Validation of the ICIM-CI model	23
5.7 Final ICIM-CI model	24
6 Use of ICIM-CI model for immunity prediction on an application PCB	25
6.1 General	25
6.2 Calculation of the power flowing into the under-test IC pin	26
Annex A (informative) Example of ICIM-CI model written as SPICE subckt	29
A.1 General	29
A.2 Example	29
Annex B (informative) Example of conducted immunity calculation applied to a LIN transceiver used in an automotive application	33
B.1 General	33
B.2 LIN driver ICIM-CI model	33
B.3 Application board modelling	34
B.4 Conducted immunity calculation	36
B.4.1 Calculation without non-linear element	36
B.4.2 Calculation with non-linear element	37
Bibliography	39
Figure 1 – Example of ICIM-CI model structure	8
Figure 2 – ICIM-CI model extraction flow proposal	8
Figure 3 – Pin description of the IC under test	9
Figure 4 – Example of PCB dedicated to S-parameters measurement	11
Figure 5 – Example of reflection coefficient measurement performed on the IC under test	12
Figure 6 – Example of LIN pin impedances depending on state	12
Figure 7 – Example of transmission coefficient measurement performed on the IC under test	13
Figure 8 – Structure of IBIS model	14

Figure 9 – Example of packaging extraction tool	14
Figure 10 – Example of parasitic elements computation with an advanced packaging extraction tool	15
Figure 11 – Example of DPI test setup	15
Figure 12 – Example of PCB dedicated to DPI test.....	16
Figure 13 – Example of a configuration for LIN driver DPI measurement	17
Figure 14 – Example of incident power at IB extraction board LIN input during DPI measurement of the initial configuration for each OO	17
Figure 15 – Example of block diagram for DPI setup modelling	19
Figure 16 – Example of DPI SPICE modelling to calculated power transmitted to VBAT pin during a 0 dBm power injection at IB extraction board input.....	20
Figure 17 – Example of IB extraction board trace modelling using SPICE subcircuit model.....	20
Figure 18 – Example of transmitted power and voltage magnitude calculated at VBAT pin of the IC under test during DPI SPICE simulation performed at 0 dBm.....	21
Figure 19 – Example of comparison incident vs transmitted power for a DPI on + 12 V board pin.....	22
Figure 20 – Example of transmitted power calculated at LIN pin input during DPI SPICE simulation performed at 0 dBm: validation vs IB extraction configuration.....	23
Figure 21 – Example of incident power calculated at LIN pin input inducing a fault on LIN pin during DPI SPICE validation simulation: calculation vs measurement	24
Figure 22 – ICIM-CI XML writer.....	25
Figure 23 – Example of white box construction of a DPI setup modelling at application level	26
Figure 24 – Example of transmitted power calculation at application board.....	27
Figure 25 – Example of voltage V and current I calculation	27
Figure 26 – Example of fault prediction.....	28
Figure A.1 – Example of ICIM-CI model written as SPICE subcircuit	32
Figure B.1 – Example of an automotive application board	33
Figure B.2 – LIN driver ICIM-CI model	34
Figure B.3 – Example of an automotive application board schematic.....	35
Figure B.4 – Example of an automotive application board 3D modelling	35
Figure B.5 – Example of conducted immunity calculation modelling	36
Figure B.6 – Example of comparison of the calculated transmitted power with the IB and the RF power injection measurement – without non-linear element-.....	37
Figure B.7 – Example of comparison of the calculated transmitted power with the IB and the RF power injection measurement – with non-linear elements-.....	37
Figure B.8 – Example of current and voltage calculation during a transient analysis	38
Figure B.9 – Example of calculated current and voltage at 10 MHz (Nyquist sampling)	38
Table 1 – Examples of OO, failure criteria and DI for different types of IC	9
Table 2 – Examples of OO, failure criteria and DI for the IC under test.....	10
Table B.1 – OO, failure criteria and DI for the LIN transceiver under test.....	34

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**EMC IC modelling -
Part 4-1: Use of ICIM-CI model to predict
the IC conducted immunity in a PCB****FOREWORD**

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The text of this Technical Report is based on the following documents:

Draft	Report on voting
47A/1191/DTR	47A/1197/RVDTR

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Report is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

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1 Scope

This part of IEC 62433-4 provides an overview of good practices to extract an ICIM-CI model from measurements and to build a numerical model of the PCB in which the ICIM-CI model is used to predict RF immunity of an IC in its application PCB.

This document also discusses factors which can be considered to obtain proper results in an ICIM-CI model extraction and use of the actual model at the PCB level.

2 Normative references

There are no normative references in this document.

3 Terms, definitions and abbreviations

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at <https://www.electropedia.org/>
- ISO Online browsing platform: available at <https://www.iso.org/obp>

3.1.1

PDN

Passive Distribution Network

block that describes the impedance network of one or more ports of the integrated circuit

[SOURCE: IEC 62433-4:2016, 3.1.13]

3.1.2

IB

Immunity Behaviour

block that describes the internal immunity behaviour of the IC

[SOURCE: IEC 62433-4:2016, 3.1.14]

3.1.3

DI

Disturbance Input

input terminal for the injection of RF disturbances

Note 1 to entry: It could be any pin of IC, an input, supply or an output.

[SOURCE: IEC 62433-4:2016, 3.1.9]

3.1.4

DO

Disturbance Output

terminal whose load influences the impedance of DI terminal, and/or the transfer characteristics of PDN, and that outputs a part of the disturbance received on the DI terminals

[SOURCE: IEC 62433-4:2016, 3.1.10]

3.1.5**OO**

Observable Output

output terminal where the immunity criteria are monitored during the test

[SOURCE: IEC 62433-4:2016, 3.1.11]

3.1.6**GND**

Ground terminal

terminal that is used as reference for return path

[SOURCE: IEC 62433-4:2016, 3.1.12]

3.1.7**internal terminal**

terminal of an integrated circuit macro-model's component which interfaces the component to other components of the integrated circuit macro-model

[SOURCE: IEC 62433-4:2016, 3.1.5]

3.1.8**external terminal**

terminal of an integrated circuit macro-model which interfaces the model to the external environment of the integrated circuit

[SOURCE: IEC 62433-4:2016, 3.1.4]

3.2 Abbreviated terms

ADC	Analog to digital converter
CAD	Computer-aided design
CAN	Controller area network
DPI	Direct RF power injection
DUT	Device under test
EM	Electromagnetic
IBIS	Input/output Buffer Information Specification
JTAG	Join test action group
LDO	Low dropout
LED	Light-emitting diode
LIN	Local interconnect network
PCB	Printed circuit board
PWB	Printed wiring board
PWM	Pulse width modulation
RFIP	Radio Frequency Injection Probe
SMA	Sub-miniature A-version
SOLT	Short-Open-load-Thru
S-Parameter	Scattering parameter
SPICE	Simulation program with integrated circuit emphasis

TL	Transmission line
TRL	Thru Reflect Line
VNA	Vector network analyser

4 Philosophy

This document proposes an overview of methods:

- to extract an ICIM-CI model,
- to calculate the current, voltage or power conducted into an IC pin during a direct power injection (DPI) test according to IEC 62132-4 [1]¹ performed at test board level,
- to compare the calculated current, voltage or power to the Immunity Behaviour (IB) data of the ICIM-CI model,
- to predict the immunity level of an IC in a PCB.

The use of ICIM-CI model allows the prediction of the RF immunity behaviour of an IC at PCB level. The simulation results of this model are, for example, used to predict the RF immunity of a second source IC without performing requalification test at PCB level.

5 ICIM-CI model extraction flow

5.1 General

The ICIM-CI model consists of a set of data describing two parts:

- PDN: the Passive Distribution Network describes the path which conducts the disturbances from the external environment to the internal IC blocks. The PDN is a multi-port circuit. It is composed of four different terminals:
 - DI: Terminals to which disturbances are applied,
 - DO: Terminals that can influence the impedance of the DI terminals and consequently receive a part of the disturbance applied on the DI terminals,
 - GND: PDN has one or more ground terminals (such as digital ground, analogue ground),
 - Internal terminals: Terminals that can influence the impedance of the DI terminals and are internal to the IC (at chip-level).
- IB: The Immunity Behaviour describes how the IC reacts to the applied disturbances (referenced to one ground terminal of the PDN). The immunity criterion is set on terminals that are called Observable Output (OO). These OO could be associated or not to the various DI, depending on the configuration of the IC.

NOTE 1 DI, DO, OO and GND terminals are external terminals and are interfaced at pin level. These pins connect to the external environment of the IC.

NOTE 2 OO terminals link the PDN to the IB. These terminals are used to obtain the IB by monitoring the immunity criterion. In Figure 1, they are virtually represented (internally) on the PDN of the ICIM-CI macro-model.

Figure 1 illustrates an example of ICIM-CI model structure.

¹ Numbers in square brackets refer to the Bibliography.

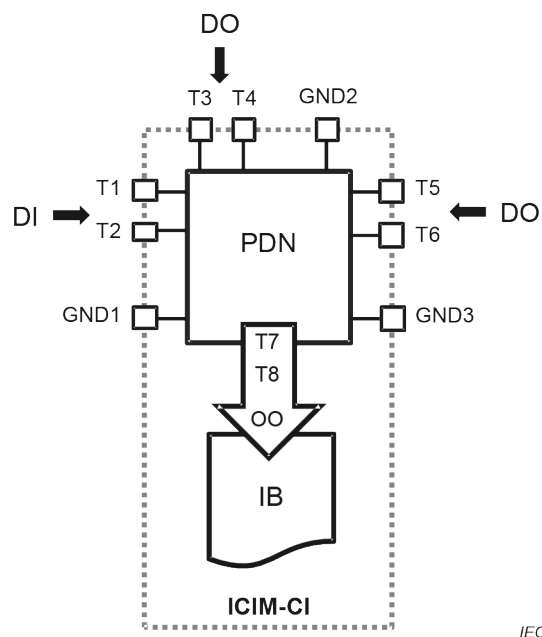


Figure 1 – Example of ICIM-CI model structure

The ICIM-CI model extraction flow is described in Clause 7 of IEC 62433-4:2016 [2]. The validation of the extracted model is described in Clause 8 of IEC 62433-4:2016. The flow described in Figure 2 groups these two steps to arrive at a final model. This flow is presented in [1] and will be described in detail in the following subclauses. Some ICIM-CI model extraction examples could be found in [4], [5], [6], [7] and [8].

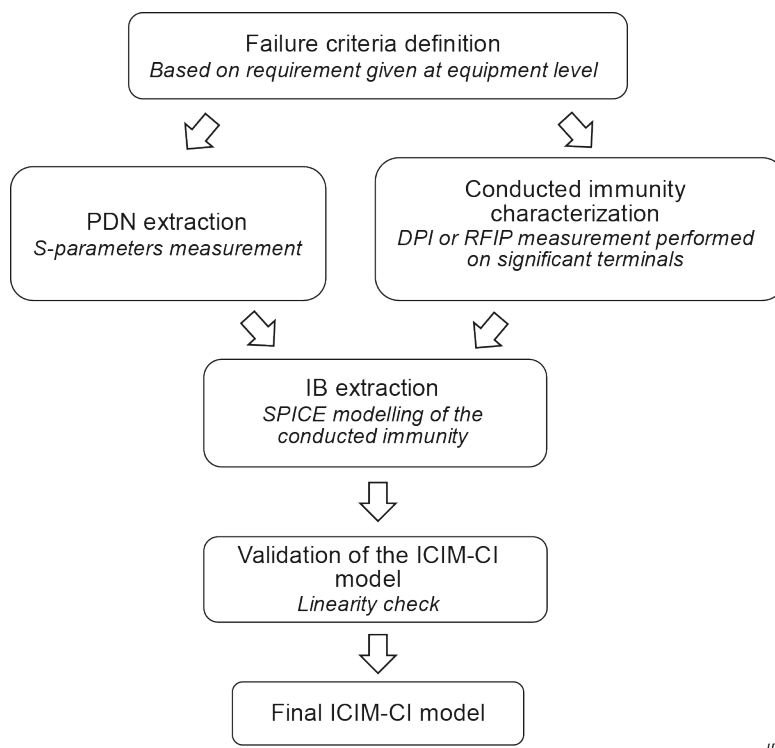


Figure 2 – ICIM-CI model extraction flow proposal

NOTE RFIP technique [9] is described in Annex G of IEC 62433-4:2016. This method allows to obtain the voltage and the current at the IC pin where the power is injected.

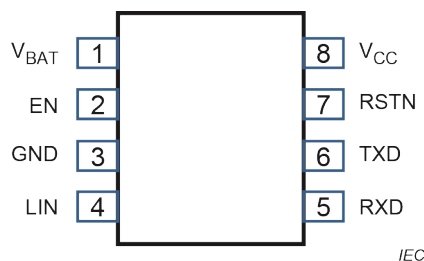
5.2 Failure criteria definition

The failure criteria could be multiple. They are based on requirements fixed at application level. Failure criteria are very dependent of the type of the IC. Table 1 gives some examples of OO, failure criteria and DI for different types of IC.

Table 1 – Examples of OO, failure criteria and DI for different types of IC

IC type	OO	Failure criterion	DI pin
Communication Bus transceivers	RX, TX, communication lines	Signal tolerance in time domain	Communication lines, Power
Voltage regulator	Output Reset	Tolerance of output voltage Reset generation	Input, output (if external)
Power components	Output	Tolerance of output voltage or tolerance in time domain if switched	Input, output if external
Logic gate circuits	Output	State change	Power, Input
Analogue circuits	Output	Tolerance in time domain	Input pin
ADC	Output	conversion error	Power, input
Sensors	Output	Tolerance in time domain	Power, output, input when present
Microcontroller	Memory Reset Output	data corruption Activation Tolerance in time domain	Power lines, input, output

The IC under test which will be used in this document to illustrate the ICIM-CI extraction flow is a LIN transceiver embedding a voltage regulator. Figure 3 describes the pins of the IC under test.



Key

- 1 V_{BAT} : Battery supply
- 2 EN: Enable input
- 3 GND: ground
- 4 LIN: LIN bus line
- 5 RXD: LIN received data output
- 6 TXD: LIN transmitted data input
- 7 RSTN: Reset output (active low)
- 8 V_{CC} : Voltage regulator output

Figure 3 – Pin description of the IC under test

The pins selected for conducted immunity test and for the PDN extraction are to be identified carefully. Typically, the following physical IC pins are considered as DI:

- IC pins with a direct access to the PCB connector,
- IC pins with an access to the PCB connector through filtering components or devices as supply lines,
- IC pins sensitive to external RF disturbance such as analogue I/O pins (current sensing, capacitive sensor, etc).

Typically, the following physical IC pins are considered as DO:

- IC pins which have an influence on the disturbance propagation path identified during the application review and IC functional block diagram analysis.

Table 2 gives some examples of OO, failure criteria, failure monitoring, DI and DO for the IC under test. OO, DI and DO are referenced to the same ground pin GND.

Table 2 – Examples of OO, failure criteria and DI for the IC under test

OO	Nominal behaviour	Failure criteria	Failure monitoring	DI	DO
LIN	PWM with same characteristics (frequency, duty cycle) as TX signal with a magnitude of 12 V.	$\pm 5 \text{ us}$ $\pm 2,5 \text{ V}$	Mask on oscilloscope	V_{BAT} , LIN	V_{CC}
RX	PWM with same characteristics (frequency, duty cycle) as TX signal with a magnitude of 5 V.	$\pm 5 \text{ us}$ $\pm 1 \text{ V}$	Mask on oscilloscope	V_{BAT} , LIN	V_{CC}
VCC	5 V DC	$\pm 0,2 \text{ V}$	Mean Value	V_{BAT}	
RSTN	5 V DC	$\pm 0,2 \text{ V}$	Mean Value	V_{BAT}	

5.3 PDN extraction

5.3.1 General

The PDN is constituted by passive elements representing the impedance of the disturbance path. This path is mainly constituted by the parasitic RLC elements of the package including the assembly of the die on a lead frame or on a substrate through a set of bonding wires.

The PDN describes the linear behaviour of the IC. The non-linear effects are not considered in the PDN of the ICIM-CI macro-model. Therefore, impedance measurements are carried out in the typical operating conditions in a steady state mode. The proposed PDN of ICIM-CI model is limited to a level so that the protection devices are not triggered. The activation of internal protection devices would induce non-linearity in the model definition, which is not considered in the PDN. However, non-linear effects are inherently considered in the IB.

The PDN is extracted with mandatory external components as specified by the manufacturer.

There are several methods to extract the PDN of an IC:

- PDN extraction from SYZ-parameters measurements;
- PDN extraction from available simulation models;
- PDN extraction from package geometry.