



BSI Standards Publication

Electrostatics

Part 5-6: Protection of electronic devices from electrostatic phenomena — Process assessment techniques

National foreword

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TECHNICAL SPECIFICATION

**Electrostatics -
Part 5-6: Protection of electronic devices from electrostatic phenomena -
Process assessment techniques**



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CONTENTS

FOREWORD	4
INTRODUCTION	6
1 Scope	7
2 Normative references	7
3 Terms, definitions, symbols and abbreviated terms	7
3.1 Terms and definitions	8
3.2 Symbols and abbreviated terms	8
3.2.1 Symbols	8
3.2.2 Abbreviated terms	10
4 Personnel safety	10
5 Experience level required	10
6 Measurement techniques for ESD risk assessment	11
7 ESD robustness of ESDS used in processes	13
7.1 General considerations	13
7.2 ESD withstand currents of single devices (components)	13
7.2.1 Human body model	13
7.2.2 Discharge of charged conductors	14
7.2.3 Charged device model	14
7.3 ESD withstand currents of electronic assemblies	16
7.3.1 Discharge of charged personnel	16
7.3.2 Discharge of charged conductors	16
7.3.3 Discharge of boards/systems	16
7.4 Voltage sensitive devices	17
8 ESD risk assessment flows	17
8.1 General considerations	17
8.2 Manual handling steps	18
8.2.1 General considerations	18
8.2.2 Parameter limits for ESD risk assessment in manual handling steps	18
8.2.3 Detailed ESD risk assessment flow	19
8.3 Conductors	21
8.3.1 General considerations	21
8.3.2 Parameter limits for ESD risk assessment of conductors	22
8.3.3 Detailed ESD risk assessment flow	22
8.4 Charged ESDS	24
8.4.1 General considerations	24
8.4.2 Parameter limits for ESD risk assessment of charged ESDS	24
8.4.3 Detailed ESD risk assessment flow	25
8.5 Risks due to process essential insulators	27
8.5.1 General considerations	27
8.5.2 Parameter limits for ESD risk assessment of process essential insulators	27
8.5.3 Detailed ESD risk assessment flow	28
8.6 ESD risk assessment by ESD event detection	30
8.6.1 General considerations	30
8.6.2 General procedure	31
8.6.3 Detailed ESD risk assessment flow	31

Annex A (informative) Measurement techniques and equipment.....	33
A.1 General considerations	33
A.2 Measurements of grounding	33
A.2.1 Resistance measurement apparatus	33
A.2.2 Low resistance meter (DC ohmmeter, multimeter).....	35
A.2.3 AC voltage check.....	36
A.3 Measurements of contact resistance	37
A.3.1 Background information and application to ESD risk assessment.....	37
A.3.2 Surface, point to point or volume resistance measurements at 10 V and 100 V.....	37
A.3.3 Surface, point to point or volume resistance measurements at voltages greater than 100 V.....	38
A.3.4 Determination of contact resistance under ESD conditions	39
A.4 Measurements of electrostatic fields	41
A.4.1 General considerations	41
A.4.2 Electrostatic field meter	41
A.5 Measurements of charges	42
A.5.1 General considerations	42
A.5.2 Faraday pail	43
A.5.3 Electrometer	43
A.5.4 Current probe or CDM discharge head or Pellegrini target	44
A.6 Measurements of electrostatic voltages	44
A.6.1 Charged plate monitor	44
A.6.2 Walking test kit.....	45
A.6.3 Non-contacting electrostatic voltmeter (ESVM)	46
A.6.4 Contact voltmeter	47
A.7 Measurements of discharge events.....	48
A.7.1 Antenna with oscilloscope	48
A.7.2 ESD event detectors	50
A.8 Measurements of discharge currents	50
A.8.1 General considerations	50
A.8.2 Current probe	51
A.8.3 Pellegrini target	53
A.8.4 CDM test head.....	54
Annex B (informative) Grounding of automated handling equipment (AHE)	56
B.1 Background information	56
B.2 Test equipment	56
B.3 Test procedure.....	57
B.4 Suggested equipment grounding guidelines	57
Annex C (informative) Preparation: What is necessary to prepare an effective ESD risk assessment?	59
C.1 Best practices	59
C.2 Measurement of temperature, humidity and basic electrostatic conditions.....	59
C.3 Further hints for preparation	59
Annex D (informative) ESD risk assessment and mitigation	60
Annex E (informative) Examples for defining limits in ESD risk assessment for risks due to charged personnel	61
Annex F (informative) Example for ESD risk assessment in a "pick and place" process	63

F.1	Process description	63
F.2	Parameter limits and equipment.....	64
F.3	ESD risk assessment of "Pick operation"	64
	Bibliography.....	66
Figure 1	– Direct (best correlation) and indirect (least correlation) measurements to assess an ESD risk.....	12
Figure 2	– Flow to assess ESD risk induced by personnel	21
Figure 3	– Flow to assess the ESD risk induced by conductors	24
Figure 4	– Flow to assess the ESD risk induced by charged ESDS	26
Figure 5	– Flow to assess the ESD risk induced by process essential insulators	30
Figure 6	– Flow to assess the ESD risk by detecting the electromagnetic radiation using ESD event detectors or antennas and oscilloscopes.....	32
Figure A.1	– Circuit diagram of experiments and simulations of contact resistance	39
Figure A.2	– Examples of current probes	52
Figure A.3	– Example of a 4-GHz Pellegrini target	53
Figure A.4	– Commercially available CDM test head used for discharge current measurements	54
Figure E.1	– Discharge current measured in the field and during device qualification [17]	61
Figure F.1	– Schematic representation of a "pick and place" operation with two handlers	63
Table 1	– Resistance ranges of materials used in this document.....	11
Table 2	– Overview of possible instruments used for different scenarios to assess ESD risk	12
Table A.1	– Peak current ranges of CDM discharges of small and large verification modules for oscilloscopes with a bandwidth of 1 GHz and 6 GHz according to ANSI/ESDA/JEDEC JS-002-2022 [28].....	55

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Electrostatics -**Part 5-6: Protection of electronic devices from electrostatic phenomena –
Process assessment techniques**

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This Technical Specification cancels and replaces IEC PAS 61340-5-6 published in 2022. This first edition constitutes a technical revision.

The text of this Technical Specification is based on the following documents:

Draft	Report on voting
101/734/DTS	101/741/RVDTS

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Specification is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 61340 series, published under the general title *Electrostatics*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

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INTRODUCTION

This document describes a set of methodologies, techniques, and tools that can be used to characterize a process where ESD sensitive items (ESDS) are handled. This document's procedures are meant to be used by those possessing knowledge and experience with electrostatic measurements.

This document provides methods to determine the level of ESD risk that remains in the process after ESD control items and materials are implemented.

These test methods' objective is to identify if possibly damaging ESD events are occurring or if significant electrostatic charges are generated on people, equipment, materials, components, or printed circuit board assemblies (PCBA) even though there are ESD control precautions in place.

Sensitivities of ESDS are characterized by industry standard ESD testing and rated by their withstand voltages or withstand currents. This document is intended to provide methods to determine whether items of a given withstand voltage or withstand current are at risk in the process.

The wide variety of ESD control items and materials and the environment in which these items are used can require test setups different from those described in this document. Users of this document can adapt the test procedure and setups described in Annex A to produce meaningful data for the user's application.

Organizations performing these tests can determine if on-going process characterization is necessary, and if so, the time interval between observations. These observations can also be made when new products are introduced or when process changes occur. Examples of process changes include tools, fixtures, equipment, new items/products, and additional manufacturing steps.

The topics below are not addressed in this document:

- Program management: see IEC 61340-5-1.
- Compliance verification: see IEC TS 61340-5-4 [1]¹.

¹ Numbers in square brackets refer to the Bibliography.

1 Scope

This part of IEC 61340 establishes a set of methodologies, techniques, and instruments to characterize a process where electrostatic discharge (ESD) sensitive items (ESDS) are handled. ESD risk assessment covers risks by charged personnel, ungrounded conductors, charged ESDS, charged insulators, and ESDS in an electrostatic field.

This document applies to activities that manufacture, process, assemble, install, package, label, service, test, inspect, transport, or otherwise handle electrical or electronic parts, assemblies, and equipment susceptible to damage by electrostatic discharges.

This document does not apply to electrically initiated explosive items, flammable gases and liquids or powders.

The document does not address program management, compliance verification or program manager/coordinator certification.

Risks due to electromagnetic sources that produce AC fields are not considered.

Descriptions of measurement techniques are given in Annex A.

Annex B provides best practices for grounding automated handling equipment (AHE), Annex C summarizes the best practices to prepare an effective ESD risk assessment, and Annex D introduces mitigation measures resulting from the ESD process assessment.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61010-1, *Safety requirements for electrical equipment for measurement, control, and laboratory use – Part 1: General requirements*

IEC 61340-2-3, *Electrostatics – Part 2-3: Methods of test for determining the resistance and resistivity of solid materials used to avoid electrostatic charge accumulation*

IEC 61010-2-030, *Safety requirements for electrical equipment for measurement, control, and laboratory use – Part 2-030: Particular requirements for equipment having testing or measuring circuits*

IEC 61340-5-1, *Electrostatics – Part 5-1: Protection of electronic devices from electrostatic phenomena – General requirements*

3 Terms, definitions, symbols and abbreviated terms

For the purposes of this document, the terms and definitions given in IEC 61010-1, IEC 61010-2-030, IEC 61340-5-1 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

3.1 Terms and definitions

3.1.1

ESD risk assessment

assessment of the risk of damage to ESDS resulting from ESD events or exposure to electrostatic fields

3.1.2

process

unique combination of tools, materials, methods, and people engaged in producing a defined output

Note 1 to entry: The term "process" can refer to a complete assembly process or a minor step, such as the pick operation of a pick-and-place process.

3.1.3

process assessment

methodological framework to evaluate the process capabilities regarding defined parameters

3.1.4

process capability

parameters for different ESD risks that allow safe handling of items with a given ESD withstand voltage or a given ESD withstand current

3.2 Symbols and abbreviated terms

3.2.1 Symbols

C	capacitance
C_{CDM}	capacitance of a device (component) in the CDM qualification tester
$C_{\text{conductor}}$	capacitance of a conductor in the process
C_{ESD}	source capacitance of an ESD model
C_{ESDS}	capacitance of the ESDS in the process
C_{HBM}	source capacitance of the HBM
C_g	gate capacitance
C_{MM}	source capacitance of the MM
$C_{\text{personnel}}$	capacitance of personnel in the process
$I, I(t)$	(time dependent) current
I_{atten}	current attenuation ratio
I_{CDM}	charged device model withstand current (device level qualification)
I_{HBM}	human body model withstand current (device level qualification)
I_{MM}	machine model withstand current (device level qualification)
$I_{\text{personnel}}$	discharge current of personnel
I_{ref}	peak discharge current of a metal object (reference object)
L	inductance
L_{series}	series inductance
Q	charge
Q_{br}	charge required for breakdown

$Q_{\text{conductor}}$	charge stored on a conductor in the process
Q_{ESD}	initial charge stored in the capacitance of the ESD model
Q_{ESDS}	charge stored on the ESDS
Q_{HBM}	initial charge stored in the capacitance of the HBM
$Q_{\text{personnel}}$	charge stored on personnel in the process
R	resistance
R_{arc}	arc resistance
R_{contact}	contact resistance
R_{g}	resistance point to ground
R_{HBM}	human body model network resistance (device level qualification)
R_{input}	input impedance of an oscilloscope
$R_{\text{p-p}}$	point-to-point resistance
R_{S}	surface resistance
R_{sample}	resistance of a sample under test
R_{series}	series resistance
R_{shunt}	shunt resistance (of a measurement target)
R_{total}	total resistance
R_{V}	volume resistance
t	time
t_0	start time (for example, of a discharge waveform)
t_{pm}	pulse length of a machine model pulse (device level qualification)
t_{end}	end time (for example, of a discharge waveform)
$V, V(t)$	(time dependent) voltage
V_0	voltage at time t_0
V_{CDM}	charged device level withstand voltage (device level qualification)
$V_{\text{conductor}}$	charging (voltage) of a conductor in the process
V_{ESD}	withstand voltage of an ESD model (device level qualification)
V_{ESDS}	voltage at the ESDS in the process
V_{gbr}	gate breakdown voltage
V_{HBM}	human body model withstand voltage (device level qualification)
V_{MM}	machine model withstand voltage (device level qualification)
$V_{\text{personnel}}$	charging (body voltage) of personnel in the process
W	electrical energy
W_{atten}	energy attenuation ratio
$W_{\text{conductor}}$	electrical energy stored on a conductor in the process
W_{MM}	machine model withstand energy (device level qualification)
ω	angular velocity

3.2.2 Abbreviated terms

AHE	automated handling equipment
CBE	charged board event
CDE	cable discharge event
CDM	charged device model
CPM	charged plate monitor
EGC	equipment grounding conductor
EMI	electromagnetic interference
EPA	electrostatic discharge protected area
ESD	electrostatic discharge
ESDS	ESD sensitive item or items
ESVM	non-contact electrostatic voltmeter
GFCI	ground fault circuit interrupter
HBM	human body model
IC	integrated circuit
MM	machine model
PCB	printed circuit board
PCBA	printed circuit board assembly
RCD	residual current device
RH	relative humidity
TC	test condition (stress level used in CDM qualification tests)

4 Personnel safety

The procedures and equipment described in this document can expose personnel to hazardous electrical conditions. Users of this document are responsible for selecting equipment that complies with applicable laws, regulatory codes, and both external and internal policy. Users are cautioned that this document cannot replace or supersede any requirements for personnel safety.

Safety requirements for electrical equipment for measurements are given in IEC 61010-1 and IEC 61010-2-030.

Residual current devices (RCD) or ground fault circuit interrupters (GFCI) and other safety protection should be considered wherever personnel can come into contact with electrical sources. Electrical hazard reduction practices should be exercised, and proper grounding instructions for equipment shall be followed.

Resistance measurements obtained through the use of the test methods described in this document shall not be used to determine the relative safety of personnel exposed to hazardous AC or DC voltages.

5 Experience level required

The procedures in this document are for use by personnel possessing advanced knowledge and experience with electrostatic measurements. The interpretation of the results from the measurements described in this document requires significant experience and knowledge of the physics of ESD and the process.

6 Measurement techniques for ESD risk assessment

Specific instruments are needed for specific measurement techniques to perform a proper ESD risk assessment. The appropriate instruments are required to measure if a material fulfils given requirements. The resistance of a material is an important parameter for ESD risk assessment. In many cases, the resistance range of a material that is conductive, dissipative or insulative range determines the risk scenario. The definition of the resistance ranges for the purpose of this documents are summarized in Table 1.

Table 1 – Resistance ranges of materials used in this document

Material classification	Test method	Method description	Limits
Conductor, conductive material	IEC 61340-2-3 ^a	R_S Surface resistance	$R_S < 1,0 \times 10^4 \Omega$
	IEC 61340-2-3 ^{b,c}	R_{p-p} Point-to-point resistance	$R_{p-p} < 1,0 \times 10^4 \Omega$
Dissipative material	IEC 61340-2-3 ^a	R_S Surface resistance	$1,0 \times 10^4 \Omega \leq R_S < 1,0 \times 10^{11} \Omega$
	IEC 61340-2-3 ^{b,c}	R_{p-p} Point-to-point resistance	$1,0 \times 10^4 \Omega \leq R_{p-p} < 1,0 \times 10^{11} \Omega$
Insulator, insulative material	IEC 61340-2-3 ^a	R_S Surface resistance	$R_S \geq 1,0 \times 10^{11} \Omega$
	IEC 61340-2-3 ^{b,c}	R_{p-p} Point-to-point resistance	$R_{p-p} \geq 1,0 \times 10^{11} \Omega$
^a Measurement of R_S according to IEC 61340-2-3 describes the use of a concentric ring electrode for planar material which is larger than the diameter of the concentric ring electrode. ^b IEC 61340-2-3 describes the point-to-point resistance measurement using either a two-point probe for non-planar materials and items with small samples or two 2,5-kg electrodes. Either of these test methods may be used. ^c The results of a measurement of R_{p-p} according to IEC 61340-2-3 can be different compared to the results of a measurement of R_S according to IEC 61340-2-3 due to the usage of different probes.			

In addition to resistances of materials, the charging status of an object or even the discharge current waveform of this object can be measured. Each process step can require a different technique and instrument to measure whether there is a risk to the ESDS being processed. Clause 6 describes the basic measurement techniques that can be used to assess various risks in different scenarios.

Table 2 lists instruments that can measure parameters to assess whether there is an ESD risk for the items handled in a process. Measurement of the actual discharge of the object under consideration is desirable. The discharge waveform can then be compared with the qualification waveform, and the risk can easily be assessed. However, measurement of the actual discharge current waveform is often difficult to achieve, especially in a production environment. Therefore, indirect parameters can be assessed, such as charging of the object, although this parameter does not tell the user whether a catastrophic discharge is happening. If it is not possible to measure charging, measurements such as resistance to ground can be used (see Figure 1). A detailed description of all the test methods is given in Annex A.

All measurements should be performed with verified instruments to ensure that the measurements are not influenced by defective instruments.

Due to the sampling nature of the procedures described in this document, deficiencies can exist that are not detected at the time the measurements are made. The measurement results obtained are valid only at the time the measurements are made, as validity can change with time.

Environmental parameters such as temperature, atmospheric pressure and relative humidity (RH) can significantly impact measurement results.

Table 2 – Overview of possible instruments used for different scenarios to assess ESD risk

Parameter (Annex A)	Personnel	Conductors	Insulators	Devices/PCBs
Discharge currents (Clause A.8)	Current probe Pellegrini target	Current probe Pellegrini target CDM test head	–	Current probe CDM test head
Discharge events (Clause A.7)	Antenna with oscilloscope ESD event detector	Antenna with oscilloscope ESD event detector	–	Current probe CDM test head
Electrostatic voltage (Clause A.6)	Charged plate monitor Walking test kit ESVM Contact voltmeter Field meter ^a	ESVM Contact voltmeter Field meter ^a	ESVM Field meter ^a	ESVM Contact voltmeter Field meter ^a
Charge (Clause A.5)	Electrometer Current probe	Faraday pail Electrometer Current probe	Faraday pail	Faraday pail Electrometer Current probe
Electrostatic fields (Clause A.4)	Field meter	Field meter	Field meter	Field meter
Resistance of material contacting ESDS (Clause A.3)	Resistance measurement apparatus	Resistance measurement apparatus Low resistance meter	Resistance measurement apparatus	Resistance measurement apparatus
Grounding (Clause A.2)	Resistance measurement apparatus	Low resistance meter Resistance measurement apparatus	–	–

^a Used as non-contact electrostatic voltmeter.

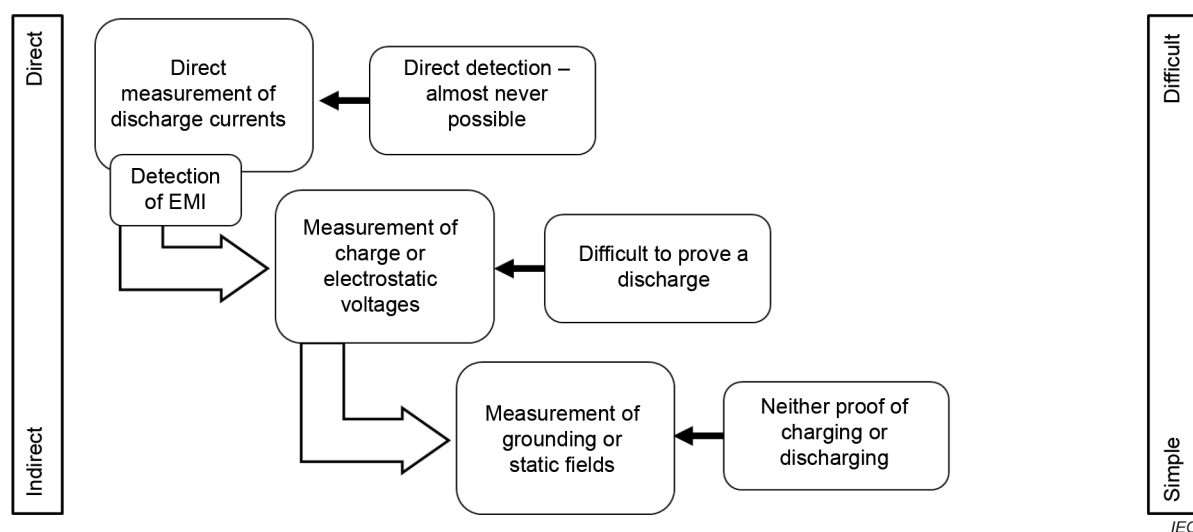


Figure 1 – Direct (best correlation) and indirect (least correlation) measurements to assess an ESD risk

7 ESD robustness of ESDS used in processes

7.1 General considerations

For a successful ESD risk assessment, one or more of the electrical/physical parameters listed in Table 2 and the ESD risk assessment flows in Clause 8 should be measured and compared against set limits. However, the parameters' limits depend on the process, measurement methodologies and techniques, and ESD robustness of the ESDS. Therefore, it is not possible to define one limit for the parameters of all ESDS and processes. It is particularly important to distinguish between handling single devices (components) and electronic assemblies. For example, a single device with relatively high robustness against a charged device model (CDM) discharge can be more susceptible to damage once installed on a PCBA. The PCBA has a larger capacitance than the single device, which can result in more severe stress (higher peak current, higher charge).

Defining limits requires some knowledge about the ESD robustness of the ESDS that is being handled in the process and knowledge about the process itself. As the ESD robustness of the ESDS in this process is better known, and the process is analysed in greater detail, more accurate limits can be determined. Otherwise, reasonable assumptions should be made.

The discharge event is the most critical point of a process or application and determining the discharge current is the most direct parameter for ESD risk assessment. Comparing the discharge current as measured in the process with the withstand current obtained during ESD qualification tests is theoretically the best approach. However, discharge currents from qualification data are often unknown and not easily obtainable directly in process measurements. Hence, more indirect parameters should be used for ESD risk assessment. In most cases, the charging and the ESD withstand voltage of the ESDS are used for the assessment. Each uncertainty in the ESD robustness of the ESDS or the knowledge about the process reduces the accuracy and, consequently, results in a higher effort combined with a possible larger margin that should be taken to exclude any risk.

Subclause 7.2 discusses how the withstand current of single devices of the different discharge scenarios can be derived either from qualification data or from limits defined in IEC 61340-5-1. A similar discussion of withstand currents of electronic assemblies is outlined in 7.3. These withstand currents are the basis for assessing the limits of the measurement parameters listed in Table 2 and the ESD risk assessment flows in Clause 8.

Subclause 7.4 discusses damage to voltage sensitive devices by charge injection from an electrostatic field or discharge source.

7.2 ESD withstand currents of single devices (components)

7.2.1 Human body model

Component manufacturers use the human body model (HBM) test to determine the sensitivity of the ESDS to discharge from a simulated charged person. The present HBM qualification procedure and the waveforms are described in IEC 60749-26 [4] or ANSI/ESDA/JEDEC JS-001 [5]. Typically, in HBM qualification, the HBM withstand voltage V_{HBM} is reported, not the HBM discharge current I_{HBM} , which is the real damaging parameter. However, the HBM withstand current I_{HBM} can be derived from the HBM withstand voltage by $I_{\text{HBM}} = V_{\text{HBM}}/R_{\text{HBM}}$ with $R_{\text{HBM}} = 1\,500\,\Omega$ being the serial resistance in the HBM discharge network. This relation is a worst-case assumption as the possible serial resistance in the ESDS is neglected.

- If the HBM robustness in terms of withstand voltage V_{HBM} of the component is known, the withstand current can be calculated by $I_{\text{HBM}} = V_{\text{HBM}}/R_{\text{HBM}}$.

EXAMPLE 1 A component with an HBM withstand voltage of 1 000 V has an HBM withstand current of $I_{\text{HBM}} = 1\,000\text{ V}/1\,500\,\Omega = 667\text{ mA}$.

- If the HBM robustness of the component is unknown, any of the following approaches can be adopted:
 - If similar products with the same power supply concept and set of I/O cells have been qualified according to HBM, these qualification values can be used as HBM withstand voltage.
 - 100 V HBM withstand voltage can be used as a reasonable lower limit of ESDS that can be handled in an EPA according to IEC 61340-5-1. For most components, this value can be quite conservative but still can be achieved rather easily in a process.

EXAMPLE 2 The maximum HBM withstand current for a component with 100 V HBM withstand voltage is then $I_{\text{HBM}} = 100 \text{ V} / 1500 \Omega = 67 \text{ mA}$.

- If the application does not tolerate any ESD related failures, the assumed HBM withstand voltage can be lowered; however, a lower HBM withstand voltage can require additional ESD control measures.

EXAMPLE 3 If for a component a HBM withstand voltage of 50 V is assumed, the HBM withstand current is $I_{\text{HBM}} = 50 \text{ V} / 1500 \Omega = 33 \text{ mA}$.

7.2.2 Discharge of charged conductors

The risk of a component being damaged by contact to a charged conductor while at least one pin of the component is at a different potential (typically grounded) was previously thought to correlate to the "machine model" (MM) test. However, MM is no longer used for component ESD qualification due to severe deficiencies in repeatability and reproducibility. Therefore, MM qualification results are typically not available.

NOTE A discharge of a charged conductor to a floating device is modelled by CDM because it is the closest approximation.

- If HBM qualification is available, HBM thresholds divided by ten can act as a reasonable approach to correlate with a charged conductor's discharge into a component at a different potential. According to [6], the correlation between V_{HBM} and V_{MM} is in the range of 3:1 to 30:1. According to [7] (withdrawn) and [8], the MM withstand current is 1,75 A per 100 V.

EXAMPLE 1 If the HBM withstand voltage of a component is 500 V, the corresponding MM withstand voltage can be estimated to be $V_{\text{MM}} = V_{\text{HBM}} / 10 = 50 \text{ V}$, and the MM withstand current to be $I_{\text{MM}} = 1,75 \text{ A} \times (V_{\text{MM}} / 100 \text{ V}) = 875 \text{ mA}$.

- If the HBM robustness of the component is unknown, any of the following approaches can be adopted:
 - 35 V MM robustness against a discharge of a charged conductor can be used as a reasonable lower limit of ESDS that can be handled in an EPA according to IEC 61340-5-1. For most of the components, this value can be quite conservative, but still can be achieved rather easily in a process.

EXAMPLE 2 The maximum MM withstand current for a component with 35 V MM withstand voltage is then $I_{\text{MM}} = 1,75 \text{ A} \times (35 \text{ V} / 100 \text{ V}) = 613 \text{ mA}$.

- If the application does not tolerate any ESD-related failures, the assumed MM withstand voltage can be lowered; however, a lower MM withstand voltage can require additional ESD control precautions.

EXAMPLE 3 The maximum MM withstand current for a component with 10 V MM withstand voltage is then $I_{\text{MM}} = 1,75 \text{ A} \times (10 \text{ V} / 100 \text{ V}) = 175 \text{ mA}$.

7.2.3 Charged device model

The phenomenon of a charged component or a component in the presence of an electric field being discharged when contacted by a conductive item is referred to as a charged device model event. The present versions of this model are described in the standards IEC 60749-28:2022 [9] and ANSI/ESDA/JEDEC JS-002 [10]. For assessing the risk of damage in this CDM scenario, it is necessary to know the CDM robustness of the component.

- If the CDM robustness in terms of withstand current I_{CDM} of the component is known, the withstand current can be used and correlated directly to the discharge current in the process.

EXAMPLE 1 If the qualification withstand current I_{CDM} of the IC is 3,0 A, discharge currents of 3,0 A in the process should not damage the component.

- If only the CDM withstand voltage V_{CDM} is known, the CDM withstand current I_{CDM} can be estimated with the capacitance of the device in the CDM tester. There are two different approaches, a simplified approach based on two capacitance ranges and a more accurate approach based on three capacitance ranges:
 - For components with small capacitance ($< 10 \text{ pF}$), the CDM current correlates to the CDM voltage with $\sim 1,0 \text{ A}/100 \text{ V}$, which means $I_{\text{CDM}} = 1,0 \text{ A} \times (V_{\text{CDM}}/100 \text{ V})$. For components with larger capacitance ($\sim 50 \text{ pF}$), the correlation is $I_{\text{CDM}}/V_{\text{CDM}} = 2,0 \text{ A}/100 \text{ V}$, which means $I_{\text{CDM}} = 2,0 \text{ A} \times (V_{\text{CDM}}/100 \text{ V})$. The capacitance of the component in the CDM tester can be approximated from a comparison with the size of the modules used for the verification of CDM qualification testers.

EXAMPLE 2 For a large device (20 pF capacitance) with a CDM withstand voltage of 250 V, the CDM withstand current is $I_{\text{CDM}} = 2,0 \text{ A} \times (250 \text{ V}/100 \text{ V}) = 5,0 \text{ A}$.

- A more accurate approach with three capacitance ranges between 0,1 pF and 50 pF is based on recent work of the ESDA/JEDEC JWG CDM:

For a component capacitance C_{CDM} of $0,1 \text{ pF} < C_{\text{CDM}} \leq 1,0 \text{ pF}$:

$$I_{\text{CDM}} = \left[0,6 \text{ A} + \frac{C_{\text{CDM}} - 0,1 \text{ pF}}{0,9 \text{ pF}} \times 1,6 \text{ A} \right] \times \frac{V_{\text{CDM}}}{250 \text{ V}}$$

For a component capacitance C of $1,0 \text{ pF} < C_{\text{CDM}} \leq 10 \text{ pF}$:

$$I_{\text{CDM}} = \left[2,2 \text{ A} + \frac{C_{\text{CDM}} - 1,0 \text{ pF}}{9,0 \text{ pF}} \times 3,3 \text{ A} \right] \times \frac{V_{\text{CDM}}}{250 \text{ V}}$$

For a component capacitance $C_{\text{CDM}} > 10 \text{ pF}$:

$$I_{\text{CDM}} = \left[5,5 \text{ A} + \frac{C_{\text{CDM}} - 10 \text{ pF}}{40 \text{ pF}} \times 2,5 \text{ A} \right] \times \frac{V_{\text{CDM}}}{250 \text{ V}}$$

EXAMPLE 3 For a large device with 20 pF capacitance in the CDM qualification tester and a CDM withstand voltage of 250 V, the CDM withstand current is

$$I_{\text{CDM}} = \left[5,5 \text{ A} + \frac{20 \text{ pF} - 10 \text{ pF}}{40 \text{ pF}} \times 2,5 \text{ A} \right] \times \frac{250 \text{ V}}{250 \text{ V}} = 6,1 \text{ A}$$

- If the component's CDM robustness is unknown, any of the following approaches can be adopted:
 - If similar components with the same power supply concept, set of I/O cells, and the same die size and package have been qualified according to CDM, this qualification value can be used as a realistic approximation of the CDM robustness.
 - 200 V CDM withstand voltage (corresponds to 2,0 A to 4,0 A CDM current) can be used as a reasonable lower limit of ESDS that can be handled in an EPA according to IEC 61340-5-1. Experience has shown that a 100 V CDM robustness (corresponding to 1,0 A to 2,0 A CDM current) is sufficient to handle components in most of the processes without ESD damage; however, it can require additional ESD control techniques in the process.

7.3 ESD withstand currents of electronic assemblies

7.3.1 Discharge of charged personnel

For electronic assemblies/systems, in most cases, no HBM qualification is performed. However, as the current and energy of an HBM event do not change whether discharged to a single device (component) or an electronic assembly, the worst-case approximation is that all the discharge current is dissipated through one component. The withstand voltage of the entire system is then determined by the component with the lowest HBM withstand voltage.

For the HBM robustness of the single component, the same considerations as in 7.2.1 apply.

7.3.2 Discharge of charged conductors

For risks of electronic assemblies by charged conductors, the same considerations are valid as for HBM risk of electronic assemblies (7.3.1). As the discharge current and energy of a charged conductor does not change whether discharged to a component or an electronic assembly, the worst-case approximation is that all the discharge current is dissipated through one component. The withstand voltage of the entire system is then determined by the component with the lowest HBM withstand voltage.

For the robustness of the single component, the same considerations as in 7.2.2 apply.

Charged cables and the risk of a cable discharge event (CDE) can also be assessed as charged isolated conductors.

7.3.3 Discharge of boards/systems

The worst-case HBM risk for electronic systems can be correlated to the component's HBM withstand voltage. In contrast, for the discharge of a charged board (charged board event, CBE) or system or a board/system in an electric field, no easy correlation to any component qualification exists. The reason for this is that even if on a board, a component pin can be contacted directly. The charge stored on the board is typically significantly higher compared to the charge stored on a single component. Knowing the discharge peak current is required to establish any worst-case approximation. No qualification method exists yet for boards and electronic assemblies.

As a very simple worst-case approximation, the maximum allowed peak discharge current of a board (that is, the current flowing through the conductive item that contacts the board) can be estimated from the component's CDM threshold currents, see 7.2.3. As the charge stored on the board is larger than the charge stored on a single component, resulting in a wider full-width half maximum of the discharge current waveform and consequently more severe stress, a safety factor should be included. From experimental data, a safety factor of two seems to be a reasonable estimate [11]. For example, if all components on the board or in the system do not fail 3,0 A CDM current, very likely, a board discharge current of 1,5 A will not cause damage to the components on the board. This worst-case approximation requires that the discharge current in the process can be measured, which is rarely the case.

If the discharge current of the board cannot be measured, the only reasonable approach is to avoid "all" possible discharges or limit the charging of the board/system to an exceptionally low and safe value. From data in the literature (for example, see [12] and references therein), a worst-case approximation can be to limit the charging of the board/system to one-tenth of the minimum CDM robustness of all devices. For example, if the minimum CDM robustness of all components is known or assumed to be 200 V, then the charging of the board should not exceed 20 V.

Another option is to contact the ESDS with a material that limits the discharge current. See the assessment flows in 8.4 and 8.5.

7.4 Voltage sensitive devices

Some components such as MOSFETs and small value low voltage capacitors can be damaged if the voltage difference across part of the component, typically a dielectric material layer, exceeds a defined level.

Damage to a capacitive structure such as a MOSFET gate can occur if sufficient charge is introduced into the gate, causing the gate voltage to rise to the breakdown voltage level. The amount of charge Q_{br} required for breakdown can be estimated if the gate breakdown voltage V_{gbr} and gate capacitance C_g are known:

$$Q_{br} = C_g \times V_{gbr}$$

Small signal devices having small gate capacitance and low gate breakdown voltage are particularly susceptible to damage, especially when connected in very high resistance circuits. Possible damage sources can include conventional ESD sources.

The risk to voltage sensitive devices is not necessarily best evaluated using an HBM or CDM withstand voltage. Instead, it can be necessary to think in terms of an applied voltage or injected charge threshold for damage.

For a MOSFET gate, a withstand voltage of an ESD model with a known ESD source capacitance can be calculated from the gate capacitance and breakdown voltage (for example, see [13]). The initial charge Q_{ESD} in the HBM capacitance C_{ESD} at voltage V_{ESD} is

$$Q_{ESD} = C_{ESD} \times V_{ESD}$$

For example, during an HBM test, this charge would be shared with the gate capacitance C_g in parallel. The HBM charge required for breakdown is

$$C_{HBM} \times V_{HBM} = Q_{HBM} > (C_{HBM} + C_g) \times V_{gbr}$$

The susceptibility is not affected by the series resistance in the HBM circuit.

It has recently been demonstrated [14] that it can be possible to damage a voltage sensitive device in a circuit by charge injection or induction and hence voltage differences between circuit nodes connecting to the component, for example caused by changing external electrostatic fields. This risk is yet not well understood. The risk is increased if one of the circuit nodes is connected to ground.

8 ESD risk assessment flows

8.1 General considerations

Standards such as IEC 61340-5-1 give guidance on implementing an ESD control program for handling ESDS in EPAs. ESD failures can still happen even in well-equipped EPAs, as reported in many publications (see references in [15]). A detailed ESD risk assessment is needed for the various process steps to avoid failures coming from the production process. An ESD risk assessment should cover risks induced by charged personnel, ungrounded conductors, charged insulators, and charged ESDS.

Although automated processes dominate many production areas, manual process steps still exist, especially at process transition points and manual PCBA handling processes. Therefore,

assessing operator grounding and charging of personnel is necessary. Standards such as IEC 61340-4-5 [16] provide good guidance on measuring an operator's body voltage using footwear/flooring grounding. Without such an assessment, it is possible that ESD control items fail to function correctly together and are not effective.

Isolated conductors can charge and discharge into ESDS. Hence, it is also important to take precautions against isolated conductors when handling ESDS. These failures can be avoided by removing charges from all conductors, especially those in contact or close proximity with the ESDS. Following IEC 61340-5-1, the maximum voltage difference between an ESDS and a conductor shall not exceed 35 V to limit possible discharge currents between the conductor and the ESDS to an acceptable level.

Issues with CDM-type discharges are becoming more and more dominant. Many handling steps are now almost completely automated without interaction from personnel. A fact that imposes a high risk here is that many processes use insulators to aid in the process of producing a product or are part of the product itself. One basic idea of CDM protection is to control the charge on insulators, thereby avoiding charging and electrostatic fields wherever possible. This can be achieved by removing all nonessential insulators and controlling/reducing the charging of process required insulators to a safe level – including charging of both devices and printed circuit board assemblies (PCBAs).

The following subclauses describe this in more detail.

8.2 Manual handling steps

8.2.1 General considerations

Like automated systems, manual handling steps should be checked for charge generation and the possibility for direct discharge paths into ESDS. According to IEC 61340-5-1, charging is limited to an electrostatic voltage of 100 V on personnel in an EPA. Whether this value or any other value obtained in the process can cause damage to an ESDS handled by personnel should be evaluated.

The time to complete the steps being evaluated should be considered during the evaluation. If the time required for measurement is longer than the process, it is possible that critical discharging or charging can be missed.

8.2.2 Parameter limits for ESD risk assessment in manual handling steps

Four different parameters can be measured to assess the risk of an ESDS damaged by charged personnel. The results of the measurements can vary depending on the personnel and the grounding mechanisms. This variation should be considered in the assessment.

- a) Discharge current (time-dependent). The discharge peak current of charged personnel into ground can be related directly to the HBM withstand current of an ESDS (see 7.2.1 and 7.3.1). For a correlation, the decay time of the measured pulse should be below 170 ns. The decay time is the time interval between when the current is at maximum and when the pulse current is decayed to 36,8 % of the maximum. Typically, the HBM stress in a commercial HBM qualification tester is much more severe than the discharge of a human being charged to the same voltage [17] and does not need any additional margin. Therefore, the HBM withstand current I_{HBM} can be an approximation of the upper limit for the personnel's discharge peak current.

EXAMPLE 1 An IC with a component HBM current threshold $I_{\text{HBM}} = 1 \text{ A}$ should not be damaged by a discharge current of 1 A from personnel (or according to 7.2.1, by a discharge current of personnel charged to 1 500 V).

- b) Contact resistance of personnel. With a measured (possibly voltage dependent) contact resistance of personnel R_{contact} under ESD conditions (see Clause A.3), the maximum discharge current of personnel charged to a body voltage $V_{\text{personnel}}$, $I_{\text{personnel}} =$