PD IEC/TS 62647-3:2014

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Process management for avionics — Aerospace and defence electronic systems containing lead-free solder

Part 3: Performance testing for systems containing lead-free solder and finishes

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National foreword

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The UK participation in its preparation was entrusted to Technical Committee GEL/107, Process management for avionics.

A list of organizations represented on this committee can be obtained on request to its secretary.

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TECHNICAL SPECIFICATION

colour inside

Process management for avionics – Aerospace and defence electronic systems containing lead-free solder –
Part 3: Performance testing for systems containing lead-free solder and finishes

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

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PROCESS MANAGEMENT FOR AVIONICS – AEROSPACE AND DEFENCE ELECTRONIC SYSTEMS CONTAINING LEAD-FREE SOLDER –

Part 3: Performance testing for systems containing lead-free solder and finishes

FOREWORD

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- the required support cannot be obtained for the publication of an International Standard, despite repeated efforts, or
- the subject is still under technical development or where, for any other reason, there is the future but no immediate possibility of an agreement on an International Standard.

Technical specifications are subject to review within three years of publication to decide whether they can be transformed into International Standards.

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IEC/TS 62647-3, which is a technical specification, has been prepared by IEC technical committee 107: Process management for avionics.

The text of this technical specification is based on the following documents: IEC/PAS 62647-3 and GEIA-STD-0005-3.

This technical specification cancels and replaces IEC/PAS 62647-3, published in 2011. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

a) Terms and definition subclause changed in Clause 3.
b) Coherence with IEC/TS 62647-1, IEC/TS 62647-21 and IEC/TS 62647-22 definitions.
c) Introduction of “g-force” definition.
d) Reference to IEC 62647 documents when already published.
e) Harmonization of preconditioning data at Table B.1 level with regard to 5.3.3.

The text of this technical specification is based on the following documents:

Enquiry draft	Report on voting
107/213/DTS	107/233/RVC

Full information on the voting for the approval of this technical specification can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 62647 series, published under the general title *Process management for avionics – Aerospace and defence electronic systems containing lead-free solder*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- transformed into an International standard,
- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

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INTRODUCTION

The implementation of lead-free (Pb-free) interconnection technology into electronics has resulted in a variety of reactions by designers, manufacturers, and users. While the prime motivation for lead-free (Pb-free) technology was to address the social concern of improving the environment by limiting the amount of toxic and dangerous substances used in products, the ramifications of this initiative have provided a state of uncertainty regarding the performance – in this context, defined as operation and reliability, i.e. the expected life cycle of a product – of aerospace and defence systems. For over fifty years, tin-lead solder was the benchmark for electronics assembly and generations of research baselined its performance under a variety of operating conditions including the harsh settings of aerospace and defence equipment. However, with the integration of lead-free (Pb-free) technology, aerospace and defence companies are faced with questions as to whether these new materials will provide, as a minimum, the same degree of confidence during the life cycle of critical systems and products.

In evaluating performance, two approaches are used: analysis/modelling and test. This document addresses the latter, providing guidance and direction in the development and execution of performance tests for lead-free (Pb-free) electronic interconnections. The user of this document needs to be aware of the following: This document does not give answers as to how to perform a specific test. Products and systems applications vary immensely, so designers need to understand use conditions and the entire life cycle. Once this is understood, then this document can be used to give designers an understanding of how to develop a suitable test, e.g., ascertain the type of platform in which a product will be used, comprehending all the environmental effects on the platform, and learning why material characterization is key to deciding upon test parameters, etc.

Sound engineering knowledge and judgment will be required for the successful use of this document.

The global transition to lead-free (Pb-free) electronics has a significant impact on the electronics industry; it is especially disruptive to aerospace, defence and other industries that produce electronic equipment for high performance applications. These applications, hereinafter described as ADHP (Aerospace, Defence and High Performance), are characterized by severe or harsh operating environments, long service lifetimes, and high consequences of failure. In many cases, ADHP electronics need to be repairable at the soldered assembly level. Typically, ADHP industry production volumes may be low and, due to low market share, may not be able to resist the change to lead-free (Pb-free). Furthermore, the reliability tests conducted by suppliers of solder materials, components, and sub-assemblies cannot be assumed to assure reliability in ADHP applications. This document provides guidance (and in some cases direction) to designers, manufacturers, and maintainers of ADHP electronics in assessing performance of lead-free (Pb-free) interconnections.

Over the past several decades, electronics manufacturers have developed methods to conduct and interpret results from reliability tests for lead-bearing solder alloys. Since these alloys have been used almost universally in all segments of the electronics industry, and since a large body of data, knowledge, and experience has been assembled, the reliability tests for Pb-bearing solder alloys are well-understood and widely accepted.

When it became apparent that the use of Pb-bearing alloys would decline rapidly, programs were implemented to evaluate the reliability of the lead-free (Pb-free) replacement alloys. Those programs have generated a considerable database. To date, however, there is no reliability test method that is widely accepted in the ADHP industries. Reasons for this include:

a) No single lead-free (Pb-free) solder alloy has emerged as a replacement for lead-bearing alloys; instead, a number of alloys are being used in various segments of the electronics industry.

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b) The physical, chemical, and metallurgical properties of the various lead-free (Pb-free) replacement alloys vary significantly.

c) Due to the many sources of solder alloys used in electronic component termination materials or finishes, assembly processes, and repair processes, the potential number of combinations of alloy compositions is nearly unlimited. It is an enormous task to collect data for all these combinations.

d) The test methods developed by other segments: the IPC-9701A and IPC/JEDEC-9703 are directed toward shorter service lives and more benign environments. Also, there is still a question of suitable dwell times and acceleration factors. However, the intent of this document is to provide a means of coordinating the information from the IPC-9701A and IPC/JEDEC-9703 into a basic approach for ADHP suppliers.

e) The data from reliability tests that have been conducted are subject to a variety of interpretations.

In view of the above facts, it would be desirable for high-reliability users of lead-free (Pb-free) solder alloys to wait until a larger body of data has been collected, and methods for conducting reliability tests and interpreting the results have gained wide acceptance for high-reliability products. In the long run, this will indeed occur. However, the transition to lead-free (Pb-free) solder is well under way and there is an urgent need for a reliability test method, or set of methods, based on industry consensus. While acknowledging the uncertainties mentioned above, this document provides necessary information for designing and conducting performance tests for aerospace products. In addition, when developing test approaches, the material in question needs to be suitably characterized. Such material properties as ultimate tensile strength, yield strength, Poisson's ratio, creep rate, and stress relaxation have been shown to be key attributes in evaluating fatigue characteristics of lead-free (Pb-free) solders.

Because of the dynamic nature of the transition to lead-free (Pb-free) electronics, this and other similar documents are based on the best information and expertise available; its update will be considered as future knowledge and data are obtained.

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PROCESS MANAGEMENT FOR AVIONICS – AEROSPACE AND DEFENCE ELECTRONIC SYSTEMS CONTAINING LEAD-FREE SOLDER –

Part 3: Performance testing for systems containing lead-free solder and finishes

1 Scope

This part of the IEC 62647 series defines for circuit card assemblies (CCA):

– a default method for those companies that require a pre-defined approach, and
– a protocol for those companies that wish to develop their own test methods.

The intent of this document is not to prescribe a certain method, but to aid avionics/defence suppliers in satisfying the reliability and/or performance requirements of IEC/TS 62647-1 as well as support the expectations in IEC/TS 62647-21.

The default method (see Clause 5) is intended for use by electronic equipment manufacturers, repair facilities, or programs that, for a variety of reasons, may be unable to develop methods specific to their own products and applications. It should be used when little or no other information is available to define, conduct, and interpret results from reliability, qualification, or other tests for electronic equipment containing lead-free (Pb-free) solder. The default method is intended to be conservative, i.e., it is biased toward minimizing the risk to users of ADHP electronic equipment.

The protocol (see Clause 6) is intended for use by manufacturers or repair facilities that have the necessary resources to design and conduct reliability, qualification, or process development tests that are specific to their products, their operating conditions, and their applications. Users of the protocol will have the necessary knowledge, experience, and data to customize their own methods for designing, conducting, and interpreting results from the data. Key to developing a protocol is a firm understanding of all material properties for the lead-free (Pb-free) material in question as well as knowledge of package- and board-level attributes as described in 5.3.2. As an example, research has shown that the mechanisms for creep can be different between tin-lead and tin-silver-copper (SAC) solders. Understanding these mechanisms is key to determining critical test parameters such as dwell time for thermal cycling. The protocol portion of this document provides guidance on performing sufficient characterization of new materials in order to accurately define test parameters.

Use of the protocol is encouraged, since it is likely to yield more accurate results, and to be less expensive than the default method. The IEC/TS 62647-22 provides a comprehensive overview of those technical considerations necessary in implementing a test protocol.

This specification addresses the evaluation of failure mechanisms, through performance testing, expected in electronic products containing lead-free (Pb-free) solder. One failure mode, fatigue-failure through the solder-joint, is considered a primary failure mode in ADHP electronics and can be understood in terms of physics of failure and life-projections. Understanding all of the potential failure modes caused by lead-free (Pb-free) solder of ADHP electronics is a critical element in defining early field-failures/reliability issues. Grouping of different failure modes may result in incorrect and/or misleading test conclusions. Failure analysis efforts should be conducted to insure that individual failure modes are identified, thus enabling the correct application of reliability assessments and life-projection efforts.

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When properly used, the methods or protocol defined in this specification can be used along with the processes documented in compliance to the IPC-SM-785, to satisfy, at least in part, the reliability requirements of the IPC-SM-785 and JESD22-B110A.

Any portion of this document can be used to develop a lead-free (Pb-free) assembly test program, i.e., this document is tailorable and provides room for flexibility. For those situations in which results are used for reliability, verification, or qualification, stakeholder concurrence needs to be sought and documented so that expectations are understood and addressed.

This specification may be used for products in all stages of the transition to lead-free (Pb-free) solder, including:

- products that have been designed and qualified with traditional tin-lead electronic components, materials, and assembly processes, and are being re-qualified with use of lead-free (Pb-free) components;
- products with tin-lead designs transitioning to lead-free (Pb-free) solder; and
- products newly-designed with lead-free (Pb-free) solder.

For programs that were designed with tin-lead solder, and are currently not using any lead-free (Pb-free) solder, the traditional methods may be used. It is important, however, for those programs to have processes in place to maintain the tin-lead configuration including those outsourced or manufactured by subcontractors.

With respect to products as mentioned above, the methods presented in this document are intended to be applied at the level of assembly at which soldering occurs, i.e., circuit card assembly (CCA) level.

This document may be used by other high-performance and high-reliability industries, at their discretion.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC/TS 62647-22:2013, *Process management for avionics – Aerospace and defence electronic systems containing lead-free solder – Part 22: Technical guidelines*

IPC-9701A:2006, *Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments*

IPC-SM-785, *Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments*

JESD22-B110A, *Subassembly Mechanical Shock*

MIL-STD-810G:2008, *Environmental Engineering Considerations and Laboratory Tests*

3 Terms, definitions and abbreviations

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

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3.1.1
coupon
test sample representing a scaled-down or proportional version of an actual product or higher level test vehicle

3.1.2
CTE
coefficient of thermal expansion
degree of expansion of a material divided by the change in temperature

Note 1 to entry: PCB/PWB CTE (X-Y-axis) is measured in the direction in the plane of the piece part mounting surface and is used to quantify the stresses in the solder joint arising from the differences in CTE between the piece parts and the PCB/PWB during thermal cycling. CTE (Z-axis) is measured in the “thickness” direction and is typically used to quantify plated through hole stress.

[SOURCE: IEC/TS 62647-22:2013, 3.1.8]

3.1.3
g-force
force per unit mass that can be measured with an accelerometer and perceived as weight (with “g” from “gravitational”)

Note 1 to entry: Since such a force is perceived as a weight, any g-force can be described as a "weight per unit mass". g-forces, when multiplied by a mass upon which they act, are associated with a certain type of mechanical force in the correct sense of the term force, and this force produces compressive stress and tensile stress.

3.1.4
lead-free
Pb-free
less than 0,1 % by weight of lead (Pb) in accordance with reduction of hazardous substances(RoHS) guidelines

[SOURCE: IEC/TS 62647-1:2012, 3.8]

3.1.5
PCB
printed circuit board
PWB
printed wiring board
substrate using conductive pathways, tracks or signal traces etched from copper sheets laminated, and allowing to connect electrically un set of electronic components to realize a circuit card.

[SOURCE: IEC/TS 62647-21:2013, 3.1.10]

3.1.6
tin-lead
solder bearing the elements tin and lead, and corresponding to 63% by weight of tin and 37% by weight of lead unless otherwise specified

3.1.7
vehicle
test sample such as a populated circuit card assembly (CCA)

3.2 Abbreviations

ADHP	Aerospace, Defence and High Performance NOTE This refers to a generalized level of equipment used in harsh and stringent operating conditions.

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CCA	Circuit card assembly
JCAA	Joint Council of Aging Aircraft (organization within the US Department of Defence that has performed extensive lead-free solder reliability testing)
JG-PP or JGPP	Joint Group on Pollution Prevention (NASA group that began the lead-free solder testing)[1]
PSD	Power spectral density NOTE It describes how the power of a signal or time series is distributed with frequency.
RoHS	Restriction of Hazardous Substances NOTE The RoHS directive is a European directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment

4 Assumption

For the purposes of this document, if the element “lead” is implied, it will be stated either as Pb, as lead (Pb), or as tin-lead.

If a piece part terminal or termination “lead” is referred to, such as in a flat pack or a dual-inline package, the nomenclature lead/terminal or lead-terminal will be used.

5 Default test methods

5.1 General

Use of the default method shall be limited to CCAs. Test coupons may also be used provided the concerns listed in 5.3.2 are considered.

5.2 Test vehicles

5.2.1 Test vehicle type

Test vehicles used in testing of electronic systems containing lead-free solder shall consist of soldered assemblies that are representative of the materials and processes used in the assembly and/or repair procedures used by the ADHP electronics manufacturer or repair facility. Characterization and documentation of the test vehicle attributes (both design and manufacturing) is recommended. Test vehicle attribute documentation shall include, at a minimum, the following data:

- board type, material, size, finish, thickness, copper content
- piece-part material, package size, package type, termination finish
- assembly solder alloy
- assembly processes including fluxes and cleaners
- thermal management materials
- underfill and staking materials
- other mechanically attached structures

[1] JGPP Pb-free solder testing was completed with the support of JCAA.

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- environmental coatings
- repair history/process (including solder alloys)

The utilization of electrically functional assemblies/units or representative test vehicles is permitted provided full characterization of the electronic assembly materials, test vehicle configuration, and assembly processes are documented. IPC-9701A:2006, 4.2, contains additional guidance on the characterization and documentation for test vehicles.

Test coupons may be used but the user is cautioned that various attributes of concern can be different at coupon level, i.e., cool down rates, metallurgy, pitch, others. If the use of coupons is desired, the user shall perform an analysis to determine if such attribute differences exist. If differences are determined, the user shall mitigate associated risks. Be aware that results are based upon the processes used and that complete documentation of the processes is necessary if this document is being used to evaluate the processes.

5.2.2 Sample size

The number of test vehicles shall be based on a statistically based sample size and analysis plan. Accordingly, several options are available. IPC-9701A specifies a minimum number of 33 test samples. However, sample sizes can be smaller or larger depending upon usage conditions. Annex A provides additional insight into sample size selection.

5.3 Pre-conditioning by thermal aging method

5.3.1 General

Lead-free solder properties tend to change over time even under typical storage conditions. So test programs shall include some preconditioning exposure before the primary environments (e.g., temperature cycling, vibration, mechanical shock) to replicate these changes for the lifetime; IPC-9701A contains some guidance. Isothermal elevated temperature aging can accelerate these changes, such as grain growth, intermetallic compound growth, diffusion-driven voids, segregation, and oxidation. Such preconditioning can also help gain consistency among test articles by driving the grain structures to similar characteristics. The isothermal aging method may not cause changes representative of all particular application environments and processing conditions (curing bake, burn-in, environmental stress screening, field use and storage, etc.), so the test protocol and test result interpretation should account for this effect, and different time/temperature combinations may be required for different programs. In addition, the test protocol may need to include other preconditioning environments to assess all the effects pertinent to a particular application.

5.3.2 Thermal aging acceleration model

The default acceleration model which allows the tailoring of the basic isothermal aging preconditioning exposure follows the Arrhenius formulation:

$$AF = \exp\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\frac{E_a}{k} \qquad (1)$$

where

AF is the acceleration factor (dimensionless),

T_1 is the test temperature in K (in the default case, 100 °C, or 373,15 K),

T_2 is the application temperature,

E_a is the activation energy (eV), and

k is Boltzmann's constant (8,620 × $10^{-5)}$ eV/K.

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