

400Hz High Speed Static Transfer Switch

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ABSTRACT

The objective of this project was to replace electro-mechanical power line contactors with a Static Transfer Switch (STS) to improve the transfer of electrical power between aircraft generators and decrease required maintenance. The switch requirements include high reliability, lightweight, and high speed (less than 15mS) power transfer. An STS can shorten the bus transfer time to less than the "ride-through" of aircraft electronic loads and therefore have the ability to control and transfer electrical power while maintaining critical mission requirements.

The content of this paper and presentation will discuss the initial problem, the research and development approach, design, and initial testing of the STS.

INTRODUCTION

Aircraft continue to develop and place more emphasis on electronic systems. Military aircraft have mission critical electronic systems where even momentary failures can result in mission degradation or loss of aircraft. The US Navy sponsored this research under the SBIR program as existing component reliability has proven to be unacceptable and limits the aircraft power system to the older MIL-STD-704A_(F).

STS technology in the 60 Hz arena has been available for some time. Due to size and weight of products the technology has not transferred to the 400 Hz marketplace. A typical 60 Hz, 200 amp, STS weighs over 400 pounds, and is 34"W x 34"D x 76"H_(A). This program developed an STS that is nearly a direct form-fit-function of an existing mechanical double-throw contactor. STS design goals were, 260 amps, three-phase, double-throw, weight less than 15 pounds, and no larger than 5.5"W x 8.5"D x 8"H. Another goal was to provide this technology at approximately the same cost as the existing electro-mechanical contactors.

This project develops an ultra-compact STS (patent pending). The application of SCR technology to aircraft power systems decreases RF interference during switching operations as the SCR device naturally commutates only at zero current crossings. The developed device will transfer power in 3.0 mS (programmable), maintaining critical electronic loads. Future applications may add detection circuitry that monitors the power quality from each source and transfers critical loads prior to platform shutdown. This design could easily be adapted to other aircraft or military vehicles to prevent loss of power on the critical bus.

MAIN SECTION

The power semiconductor technology to be utilized was first determined. Then a variety of possible layout configurations were developed and evaluated on size, performance, and cost. Only designs presenting basically no changes to aircraft architecture would be considered, and, for reliability, the design could not be dependent on forced air-cooling from additional fans.

Major areas of design constraint included:

- Physical Size
- Mechanical Interface
- Electrical Performance
- Thermal Performance
- Cost

The above constraints had to be considered during each step of development in order that the end product meets all requirements. Further, to maximize market sales potential, the device should be as "universal" as possible to appeal to wide power applications.

SEMICONDUCTOR TECHNOLOGY SELECTION –

Conventional 60 Hz STS designs have existed for a number of years. These units typically use the Silicon Controlled Rectifier (SCR) as the base power component. The SCR offers several advantages, such as well-developed manufacturing techniques that provide a high quality part at low cost. They also have low voltage drop, extended ability to withstand surge currents, and always commutate (turns off) at a zero current crossing. This parameter is important, as it will offer greatly decreased transients (and electrical noise) to the aircraft power system. The solid-state base design eliminates moving parts and contacts that age and arc during operation. Thus, the device offers longer life, decreased service cost, and extremely fast switching speed. Two devices are required per pole. This technology is compared with others below.

- Insulated Gate Bipolar Transistor, IGBT. Low cost, fast switching speed, but higher voltage drop and the base-emitter junction cannot withstand 115 volts without additional diode protection. Two devices required per pole.
- Gate Turn-Off Thyristor, GTO. Higher cost than standard SCR, nearly doubled forward voltage drop, turn-off ability not required for this application. Two devices required per pole.
- Metal Oxide Semiconductor Field Effect Transistor, MOSFET. This device is extremely fast, easy to gate, but it has high voltage drop at the 208 volts operating level required. Two devices required per pole.
- Darlington Power Transistor. Old technology that has high forward voltage and requires a substantial base drive stem for conduction. Two devices required per pole.

As the heat generated by the STS is a direct function of forward voltage drop, the standard SCR offers the best performance of all the above technologies. Combining this with the natural zero-crossing turn-off characteristic, and lowest cost, results in the SCR as the best solution for this project.

Semiconductors are rated in Average Current, while most line currents are in Root-Mean-squared (RMS) amps. With sine-wave currents, the mathematical relationship is_(C):

$$I_{avg} = I_{rms} \times 90\%$$

As the SCR is not a bi-directional conduction device, two SCRs in opposing parallel are required to conduct AC current. Thus each SCR carries 50% of the current. Therefore, the rated current through a STS SCR conducting 260 Amps RMS is

$$I_{scr} = 260 \text{ Amps} \times 50\% \times 90\% = 117 \text{ Aavg}$$

The individual SCR heat generated is

$$\text{SCR Watts} = I_{avg} \times V_{forward}$$

Where $V_{forward}$ is the forward voltage of the SCR while conducting that average current. The $V_{forward}$ level can be found from SCR manufacturer's graphs, and is a non-linear function determined by SCR semiconductor chemistry and conducting area. Typically, the larger the SCR, the more conduction area, and thus less forward voltage loss. Heat removal from the SCRs is the most critical function. Here, two factors form the basis for evaluation:

- Heat Sink area
- Single or doubled sided SCR cooling

Hockey-puck type SCRs conduct power and heat from their two main faces. Each face is thermally connected to the device junction; thus, their internal thermal impedance is effectively doubled if they are cooled only on one surface. Figure 1 shows the typical thermal path of our STS layout.

The temperature rise ($^{\circ}\text{C}$) of each component is the thermal resistance times the wattage passing through the device. That is;

$$\Delta T (^{\circ}\text{C}) = \theta (^{\circ}\text{C/W}) \times P (\text{Watts})$$

Note in the figure that the electrical bus is included in this path. As the Heat Sink fins must be at frame potential, and the SCRs are cooled via their electrical contact surface, this path is required regardless of overall configuration.

PHYSICAL DEVELOPMENT APPROACH – The main consideration to all design considerations is the form-fit-function requirement of the base goal. A nearly limitless number of STS designs can be conceived if this parameter is ignored. To better meet this requirement and assure a feasible design, we must establish the important factors that each sub-component must meet. Some are detailed below:

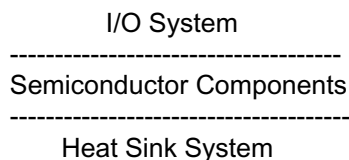
- Input/Output Electrical Parameters
 - Power System
 - Terminal Size
 - Terminal Locations
 - Control System
- Utilize same electrical switching commands as existing device: 28 VDC & 115 VAC, 400 Hz
- Auxiliary contacts must be the same quantity and electrical rating as existing device
- Semiconductor Parameters
 - Must meet base voltage & current requirements.
 - Must provide substantial overload/surge capability
 - Ideally should be capable of meeting higher voltage requirements for commercial marketability



- Heat Sink System
 - Supplies maximum surface area without restriction to airflow.
 - Should incorporate advanced design, such as corrugated fins (provide increased surface area).
 - Design based on 80°F air at 60 CFM

Combining the size constraints with the above component analysis it was determined that the STS could be broken into three logical “layers”. Each layer can be analyzed and designed to provide the layer function at the smallest utilization of space.

Basically, the general configuration of these layers becomes:



This is a logical order to the most compact design as each layer interfaces with the next. The power terminals of the upper layer connect to the SCRs of the center layer. The SCRs of the center layer connect directly to the heat removal system provided by the heat sink. But, the I/O System does not directly interface to the Heat Sink System. Thus, this logical analysis becomes the basis of further design development.

BRAINSTORMING POSSIBLE LAYOUTS - At this point in development various layouts that might meet project requirements were evaluated. Four possible designs were developed through the brainstorming exercise. Two of the designs meet the above logical layer layout. The third is a variation that adds a second power component level. The fourth design does not directly meet the logical layer configuration, and therefore would require some interference of the I/O section to the Heat Sink.

Figure 2 shows very basic design of a single layer SCR array. This layout meets the logical layer conception and utilizes SCRs that are 1.63” in diameter, 0.565” thick, rated 310 amps. The SCRs are Powerex_(D) model number C380PMX500. These SCRs are small enough to lay flat on the heat sink and still allow the package size to meet requirements, but electrical bus and insulation materials must separate them. Control electronics and I/O terminals would be located within the upper plane.

Figure 3 is a second variation on the logical layer design. This design uses larger SCRs. Each SCR is 2.28” in diameter, 1.060” thick, rated 620 amps and are Powerex model number C390MX500. The larger SCRs will have less voltage drop than above, and thus produce less heat. However, they cannot lay flat on the heat sink, as it would require the design to exceed

maximum length. Thus, the SCRs are arranged on “I” Bars. These I Bars conduct electrical power via collector busses (not shown) above the SCR body to the output terminals. The base of the I Bar transfers heat from the SCRs to the heat sink, and is electrically isolated by Aluminum Nitride (AlN) ceramic plates.

Figure 4 shows a variation of the design that does not quite meet the logical lay approach. Here, the heat sink is split into two sections, upper and lower. The upper heat sinks become the Input Terminals. A vertical rod through the center of each phase assembly would carry electrical current through the input heat sink plane, to output busses connected to output terminals. The advantage of this design is double sided cooling of the SCR. To provide space for the additional hardware the design would use the smaller SCRs.

Note that the upper heat sinks are much taller than the lower assembly. This design attempts to provide equal heat flow through each SCR face. The lower heat sink is common to all SCRs. However, the upper heat sinks are dedicated to only one pair of SCRs per phase. Thus, at any given switching configuration the design only utilizes 50% of the upper heat sink; and therefore its area is double of the lower heat sink. This results in a waste of space and weight in the design.

In Figure 5 we show a final design configuration. This design is also a variation on the logical layer concept. It uses two planes of SCRs connected to a common heat sink. The SCRs used are the smaller devices. This design allows for twice the number of SCRs, and thus decreases heat generation as each SCR only carries only 50% of load current. The non-linear Vforward function of the SCR results in less than 50% of the heat generated per SCR, and thus overall heat generated is decreased.

THERMAL PERFORMANCE ANALYSIS - Once a possible physical configuration is established its thermal performance can be estimated through basic equations. Since each design required several calculations, but each analysis is the same, a thermal calculation spreadsheet was developed. These spreadsheets are shown as Tables 1 through 4.

For each design, three operating cases were thermally evaluated. First, the normal operating point at 100% load and (aircraft supplied) forced ventilation. Second, an estimate of overload capacity is established by allowing the junction temperature to rise to maximum (about 150°C), while applying normal cooling air. The third case looks at the design if forced cooling (aircraft A/C system) air fails and the STS is cooled only by convection air through the Heat Sink. On the tables each column represents one of these cases. The input data is used to calculate a distinct junction temperature operating point for the first case. For the Overload and Convection columns, the load current is manually manipulated (trial-and-error) until the maximum junction

temperature is achieved. This is repeated for each design possible.

The spreadsheet uses Heat sink dimension data to estimate area. The thermal impedance of the SCR and the AIN electrical insulation was obtained from manufacturer data, and typical numbers supplied by Wakefield Engineering data estimated mount thermal impedance.

Input parameters were established by:

- Heat Sink Dimensions – Conception Drawings
- Number Mount Plates – Number of AIN Plates
- Irms – 100% Load, or Trial-and-Error to 150°C
- $V_f @ I_{av}$ – Data From Powerex Graphs
- θ_{hs} – Thermal Resistance of Heat Sink, Estimated From Wakefield Engineering Graphs
- θ_{AIN} – Value From Manufacturer
- #SCR per AIN – Conceptual Drawings
- SCRs /Phase – Conceptual Drawings
- T_{air} – Given From NAVSEA

Output data established by:

- Heat Sink Area – Calculation of Dimensions
- I_{ave} for V_f – 90% of Irms
- SCR Power Loss – $I_{av} \times V_f \times 50\%$
- Total Power Loss = # SCRs x SCR Power Loss
- ΔT_{jc} – SCR Power Loss x θ_{jc}
- ΔT_{mount} – $\theta_{mount} \times \text{No. Mount Faces}$
- ΔT_{AIN} – $\theta_{AIN} \times \text{Watts Transfer}$
- ΔT_{hs} – Total Power x θ_{hs}
- ΔT_a – $1.76 \times \text{Total Power} / \text{Airflow}$
- Junction Temp – Sum of all $\Delta T + T_{air}$

EVALUATION OF THERMAL ANALYSIS – The best design should provide the lowest Junction Temperature at 100% load, and also provide overload and convection capacity. Please refer to Tables 1 through 4 for the following.

100% Load Junction Temperature – The calculated data shows the following junction temperatures.

- Design of Figure 2 – 106.2 °C (Table 1)
- Design of Figure 3 – 100.3 °C (Table 2)
- Design of Figure 4 – 141.7 °C (Table 3)
- Design of Figure 5 – 114.6 °C (Table 4)

The above data shows two main results.

- Design of Figure 3 provides minimum temperature
- The two best designs were those that followed the logical layer design approach

Overload Capacity - The calculated data shows the following overload abilities.

- Design of Figure 2 – 345 Amps (Table 1)
- Design of Figure 3 – 408 Amps (Table 2)
- Design of Figure 4 – 297 Amps (Table 3)
- Design of Figure 5 – 338 Amps (Table 4)

The above data shows two main results.

- Design 3 provides the maximum overload capability
- The increased SCR size has more effect than using two smaller SCRs in parallel

Convection Cooled Capacity - The calculated data shows the following convection cooling capacities.

- Design of Figure 2 – 165 Amps (Table 1)
- Design of Figure 3 – 163 Amps (Table 2)
- Design of Figure 4 – 78 Amps (Table 3)
- Design of Figure 5 – 121 Amps (Table 4)

Designs of Figures 2 and 3 are best and basically have equal performance.

Considering all of the data, the design selected for further engineering development was that of Figure 2.

GENERAL DESIGN OF STS – Combining all of the above parameters resulted in development of a dense, compact, version of the aircraft STS. Photograph 1 shows the start of assembly of the developed STS. Note that the I Bars hold the SCRs just like that of Figure 2. An insulator plate separates phase SCRs. Note the use of plastic mounting bolts and the AIN plate.

Photograph 2 shows the STS after further assembly. Here, two phase insulator plates and all SCRs are installed. Note that Phase A Output Buss is located under the phase insulator, but the other output phase busses will be located higher, above the insulators. This layering of the busses provides sufficient conductor size in a very confined space.

Photograph 3 shows B Phase Buss installed and C Phase about to be installed. Note the Buss Spacer that will elevate B & C busses above Phase A Buss. The SCR gate leads will be routed to the PCB via holes in the insulator plates.

Photograph 4 shows the complete assembled STS. LEDs on the face provide clear indication of power and switching status. The entire device is attached to a mounting plate via four stainless steel straps. The mounting plate adapts the STS to fit the same mounting holes used by older technology components. The mounting plate can easily be adapted to fit other configurations.

DIGITAL CONTROL ELECTRONICS – The original electro-mechanical contactor had two coils to select the main contact position.

- To Ground Power coil – 115VAC, 400Hz
- To Generator Power, 28VDC

The contactors are mechanically interlocked so that only one source main contacts can close at a time, and the 28VDC command takes priority over the contact position. These command sources could also be utilized as a power supply source for the STS Printed Circuit Board (PCB).

In addition to the main contacts there are a variety of auxiliary contacts, each rated 115 VAC, 10 amps. The Ground Power side has six normally-closed contacts; the Generator side has 2 normally-closed and 2 normally-open contacts. These must be reproduced in the electronic STS to meet aircraft requirements.

The technical problem with using these command sources as a power supply source is allowable voltage range. Per MIL-STD-704 (worst-case application) these voltages can actually vary by the following.

- 28VDC Nominal: 16-40VDC
- 115VAC Nominal: 85-140VAC

A switching power supply is needed to cover a wide range of supply voltages without excessive heat production, and, since these two levels are quite different two supplies may be needed. However, upon reviewing the allocated space in the upper plane, only about 1.6 square inches is available for the total PCB. Thus, we quickly conclude that two supplies are not feasible.

One alternative was to use a miniature 400Hz transformer and rectifier to make 28VDC from the 115VAC. A supplier of small transformers was located. But, the transformer power ratings were only 50% of the 5 watts estimated to be required, and the transformer/rectifier/capacitor combination required nearly the same PCB area as a second switching power supply. Secondly, additional energy storage would be needed to provide a ride-through when transferring power sources.

The main problem here is the two different types of control power (115VAC & 28VDC). Pursuing alternatives, we looked to the power terminals. Both power sources provide the same AC voltages. Both have a MIL-STD-704 specified range of 147-242VAC. And, at least one source would be on before, during, and after a power transfer command.

The answer resulted in a very simple method of providing redundant source PCB power with minimal area required. Referring to Figure 6, two Integrated Circuit (IC) type full-wave-bridge (FWB) rectifiers are used to supply a common “universal” input switching power supply. The device selected is manufactured by Arch Electronics and can operate on 90-264 VAC, or 120-370 VDC, or combination thereof. As the unit is

rated both AC and DC, the high-ripple DC voltage provided by the two rectifiers is more than satisfactory. And the power supply requirements fall well within the MIL-STD-704 variations. The two rectifiers supply power to either source and are very small. 12 VDC was selected as the PCB control level as the use of CMOS IC's, rated from 5-18 VDC, was anticipated.

From Figure 6 we see that the input commands are passed through a scaling factor and then to a photo-optic isolation IC. The isolation IC input is rated for AC and DC. Basically, the device is a level sensing comparator. When the signal reaches an internal threshold, the isolated output is activated. The scaling circuit then becomes current limiting resistors of the value needed to trigger the output when minimum MIL-STD-704 command levels are detected. These two circuits provide a logic level DC Command (DCC), and an AC command (ACC).

Normal operation requires the aircraft to start all systems while on Ground Power. DCC passes through inverter #1 gate to form the signal DCC NOT. When this signal is combined with ACC in AND Logic #1 a base command to go to Ground Power Source is established.

However, this signal requires some additional permissions prior to firing power components. Just to the left of AND Logic 1, is a Start-UP Delay circuit. This circuit passes the PCB 12VDC power through a simple resistor-capacitor low pass circuit. The purpose of this circuit is to assure that all logic is disabled during initial power supply and circuit application. Without this small delay, possible miss-firings of power SCRs could occur. This delay is only about 200 mS.

Another circuit creates a digital time-delay of 3.0 mS, which is the time selected for power transfer from one source to the other. It provides sufficient time for all SCRs to naturally commutate. This switching sequence is shown in Figure 7, and is the heart of the STS device. This power transfer occurs sufficiently fast enough that electronic loads will not be affected. The two power sources do not necessarily have to be phase matched.

As shown in Figure 6, a programmable digital oscillator provides a 384 kHz digital signal. This signal is used for the base clock for both the 3.0 mS timer, and a stable gate firing source for the power semiconductors. Passing through a double flip-flop (provides a divide-by 4 function) the signal becomes a 96 kHz square-wave. This is the carrier provided to the high-frequency SCR gate drive circuits.

Upon start-up, the 12 bit binary counter will start at a random number and proceed to use the oscillator signal as a clock and count to a level of 1152. At that count, both the Q8 and Q11 outputs go high. This causes AND Logic 5 to go high, which is inverted by INV logic 2 to a zero state. This zero causes AND Logic 4 to stop passing the clock signal to the counter. Thus, the

counter is locked at that count until reset by another function. Regardless of the random state of the counter upon start-up, this whole sequence will take less than 11 mS. As this sequence has stabilized long before the 200 mS start-up delay of the previous circuit, it has no effect on operation other than to establish a base operating point.

As AND Logic 5 is now high, and the 200 mS start-up delay is complete (another high), AND Logic 6 will go high. AND Logic 2 then goes high, as both inputs are high. This activates the driver and energizes the Ground Power auxiliary relays on the PCB. This signal also enables AND Logic 3 to pass along the 96 kHz square-wave to the gate drives.

The drivers provide a 0/12 volt square wave to the gate drive transformers. These transformers are three-winding, 1:1:1, devices. The Primary is connected to the driver and a DC blocking capacitor. Each secondary is connected to a phase SCR via a resistor-schottky diode circuit. Phasing is arranged through the diodes such that the phase positive SCR gate is applied when the drive signal is +12 volts. And, the phase negative SCR gate is applied when the drive signal is 0 volts. If the drive signal remains at zero for over 3 uS, coupling to the secondary is lost and all SCRs are no longer gated. A gate resistor is provided to limit current to the gate junction.

When a command is received on the Generator Power source, it is scaled and processed similar to the Ground Power side. After the isolation IC is a circuit that creates a very narrow (0.20 uS) pulse each time the command position is changed. These pulses pass through an OR gate to the reset function on the binary counter. When this occurs, the counter is reset, AND Logic 5 goes low, AND Logic 6 goes low, and all SCR gate signals are disabled. This is the start of the 3.0 mS transfer period.

Just as in the mechanical design, the command to Generator Power (DCC) takes priority over the Ground Power section (ACC). INV Logic 1 output goes low, de-energizing the Ground Power SCRs and auxiliary relays. The counter counts to 1152 and stops. Note that:

$$0.003 \text{ Sec} \times 384,000 \text{ Pulses/Sec} = 1152 \text{ Pulses}$$

AND Logic 5 and 6 both return to a 1 state, enabling SCRs. But now AND Logic 1 is low, so the Ground Power SCRs remain off. AND Logic 7 is high, energizing the driver and auxiliary relays for the Generator Power source. Like the other side, the 96 kHz square-wave is used to activate the gate drivers of this source. Thus, power is transferred from Ground Power to Generator Power with a 3.0 mS "off" period.

Return to Ground Power is accomplished in similar manner. Removal of the DCC signal triggers another pulse to reset the binary counter. The 3.0 mS period

starts again. At the end of this period the system returns to the Ground Power.

Note that when operating on either source that a gate signal is constantly applied to the SCR, even when negatively biased. This allows for a simple design while also assuring SCR turn-on at the earliest possible positive-biased operating point. This feature eliminates the typical "electrical noise" generated by SCR switching in a phase-modulated circuit.

An LED is provided on each source. An illuminated LED denotes which side is connected to the output. The Source LEDs are actually connected in series with the relay coils. A shunt resistor limits current through the LED to rated value. This conserves the 420-mA current of the supply by using the same current to energize the LED and relays.

Just as the STS package utilizes dense packaging, the PCB is very compact. Figure 8 shows how the PCB fits within the upper plane of the STS design. Note that the PCB utilizes even the small cavities between power terminals. A 0.20" space is allowed on left and right edges to allow space for the SCR gate leads. The PCB is a four-layer design.

Not shown are interface wires, which must be soldered to the PCB during assembly. 24 wires are pre-soldered to the PCB prior to installation into the top cavity. These wires carry the commands and auxiliary signals to the aircraft; a short cable terminates in a standard aircraft connector. No changes to aircraft control wiring are required to update the aircraft with the new STS.

Gate leads from each SCR are routed through holes in the G-11 fiberglass assembly. During external construction the PCB is fitted with miniature ring stand-offs at each gate wire termination. The PCB is inserted into the Top and bolted in place. Then the gate leads are looped and soldered to these stand-offs. This is necessary as aligning 24 SCR wires simultaneously as the PCB is inserted would be nearly impossible. The stand-offs allow termination above the PCB after installation in the STS, and the entire cavity is then filled with epoxy, which will stabilize the entire assembly from vibration damage.

DEVELOPMENT PROGRAM – The key to a successful program was following a development program that proceeded in steps. Each step must be completed before the next step will proceed. This is similar to construction; first the foundation, then the structure, then the roof, etc. And, like a building, a general plan must be completed before starting construction. The work described above forms the foundation of the development effort. It provides baseline restrictions on size and capacities that establish the parameters of further design. Some of the basic steps and periods proposed were^(E).