

4H-SiC VJFET Based Normally-off Cascode Switches for 300°C Electronic Applications

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ABSTRACT

Vertical-Junction-Field-Effect-Transistors (VJFETs) are currently the most mature SiC devices for high power/temperature switching. High-voltage VJFETs are typically designed normally-on to ensure voltage control operation at high current-gain. However, to exploit the high voltage/temperature capabilities of VJFETs in a normally-off high-current voltage-controlled switch, high-voltage normally-on and low-voltage normally-off VJFETs were connected in the cascode configuration. In this paper, we review the high temperature DC characteristics of VJFETs and 1200 V normally-off cascode switches. The measured parameter shifts in the 25°C to 300°C temperature range are in excellent agreement with theory, confirming fabrication of robust SiC VJFETs and cascode switches.

INTRODUCTION

Silicon carbide (SiC) is ideally suited for power conditioning applications due to its high temperature capability, its high thermal conductivity, and its high critical field strength. For power devices, the tenfold increase in critical field strength of SiC allows high voltage blocking layers to be fabricated significantly thinner and more highly doped than those of comparable Si devices. This reduces device on-state resistance and the associated conduction and switching losses, while maintaining the same high voltage blocking capability. In addition, the wide band gap and excellent thermal conductivity of SiC allow operation at high temperatures where conventional Si devices fail. Circuit designers are attracted by the high-voltage and high-temperature capabilities of SiC power devices and would like to deploy them as direct replacements of power silicon MOSFETs and IGBTs. These silicon power switches are normally-off, e.g., they block their specified voltage at zero gate bias which ensures safety in case of failure.

Presently, several SiC devices are being developed for the lucrative 600 V (1200 V rating) power switching market. SiC MOS based devices show promise as

normally-off power switches but suffer from low MOS mobility and native oxide reliability issues [1]. Furthermore, several temperature dependant factors result in a decrease of the SiC MOSFET threshold voltage with temperature. This may lead to unwanted MOSFET turn on at temperatures over 200°C [2].

The SiC bipolar junction transistor is another normally-off power switching candidate. However, as with all SiC bipolar devices, its long term performance deteriorates due to forward bias voltage degradation [3]. Also, the BJT is a current controlled device that can require substantial base drive current [4].

SiC VJFETs are promising candidates for high power/temperature switching as they only use *pn* junctions as a current control mechanism in the active device area, where the high electric fields occur, and can therefore fully exploit the high temperature properties of SiC in a gate voltage controlled switching device. An important consideration in the operation of power VJFETs is maintaining high current-gain voltage-control capability by biasing the gate below its built-in potential. If the gate voltage exceeds its built-in potential value, significant hole injection occurs into the channel and the VJFET operates in bipolar mode. Under this biasing condition, the VJFET can potentially behave like a bipolar transistor with its current gain decreasing as the gate voltage increases in excess of its built-in potential value. In addition, operating the gate in bipolar mode at very low drain voltages can lead to the expansion of stacking faults, which can cause forward voltage degradation in majority carrier devices, thereby compromising long term reliability [5]. Consequently, high voltage VJFETs operating at high current-gain need be normally-on (depletion mode) devices. Nevertheless, VJFET based all-SiC high power/temperature normally-off switches can be implemented by combining a high-voltage normally-on (depletion mode) VJFET with a low-voltage normally-off (enhancement mode) VJFET in the cascode configuration.

In this paper we show that a normally-off SiC vertical channel JFET is impractical for 1200-V power switching

applications. We subsequently introduce the normally-off 1200-V all-SiC VJFET based cascode switch, analyze its operation, and review its high temperature DC characteristics.

SiC VERTICAL-CHANNEL JFET STRUCTURE

A cross sectional schematic of a normally-on high-voltage p^+ ion-implanted 4H-SiC vertical-channel JFET is shown in Figure 1. The channel layer is doped to low 10^{16} cm^{-3} , and the drift layer is doped to mid 10^{15} cm^{-3} . To ensure >1200 V blocking, a 12 μm drift layer thickness is used. In the on-state, majority carriers (electrons) flow vertically from source to drain. To control the current through the device the gates are subjected to a voltage, which adjusts the width of the depletion regions between the p -type gates in the n -type channel.

In normally-off VJFETs, the p^+ implant depletion regions overlap at 0 V gate bias. As the normally-off VJFET need only block low voltages in cascode switching operation, its drift layer is approximately 2.5 μm to minimize on-state resistance and losses.

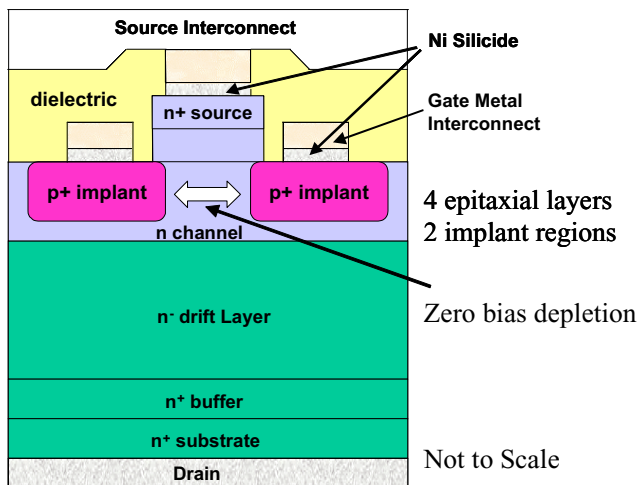


Figure 1. Simplified cross-sectional schematic of a normally-on ion-implanted SiC VJFET. The layer dimensions are not to scale.

To ensure high-voltage operation with minimum associated on-state resistance, a robust, self-aligned, multiple floating guard-ring edge termination was implemented. The high-voltage VJFETs (12 μm drift layer doped at mid 10^{15} cm^{-3}) exhibit breakdown voltages of up to 2022 V, which corresponds to 93% of the calculated 4H-SiC material limit [6]. The inherent simplicity of the vertical-channel JFET design and guard-ring edge termination has enabled seven photolithographic level fabrication with no epitaxial regrowth and with a single masked ion-implantation event [7]. As a result, VJFETs of the design presented in Fig. 1 have been manufactured at high-yields and with excellent wafer parameter uniformity [8-9].

FEASIBILITY OF A 1200 V NORMALLY-OFF VERTICAL CHANNEL JFET

To assess the feasibility of a normally-off 1200 V power switch, a vertical-channel JFET that blocks 1300 V at a gate bias of 0 V and at a drain current density of 1 mA/cm^2 was fabricated. Its blocking voltage characteristics appear in Figure 2. Gate biases were applied in the 0.5 V to 2.5 V range to confirm VJFET gate functionality. Positive values of gate bias reduce the extent of the gate depletion regions in the n -doped channel, thereby reducing blocking voltage capability. At $V_{gs} = 0 \text{ V}$ (normally-off) the VJFET blocks 1300 V. This blocking voltage is reduced to 880 V and 160 V at positive gate biases of +1 V and +2 V, respectively.

On-state drain current measurements were performed on the 1300 V normally-off VJFET and are presented in Figure 3. At a gate bias of 2.5 V, the specific on-state resistance is prohibitively high at $23 \text{ m}\Omega \text{ cm}^2$. A low specific on-state resistance of $5 \text{ m}\Omega \text{ cm}^2$ is measured at a gate bias of 3 V.

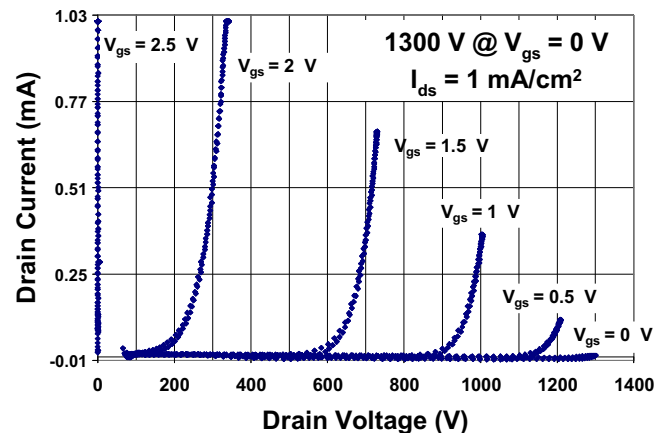


Figure 2. Blocking voltage characteristics versus gate bias for a 1300-V VJFET. The device is normally-off to 1300 V, e.g., it blocks 1300 V at zero gate-to-source bias ($V_{gs} = 0 \text{ V}$).

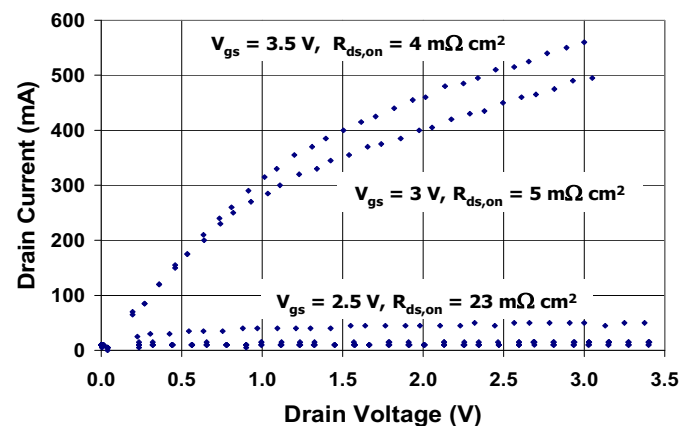


Figure 3. On-state drain current versus drain voltage characteristics of a 1300 V normally-off VJFET, at a gate-to-source bias range of 0 to 3 V, in steps of 0.5 V. At $V_{gs} = 2.5 \text{ V}$, which is below the built-in potential of the gate-to-source junction, the on-state resistance is prohibitively high at $23 \text{ m}\Omega \text{ cm}^2$.

As pointed out in Section 1, an important consideration in the operation of VJFETs in power conditioning circuits is maintaining high current-gain voltage-control capability by biasing the gate below its built-in potential. For VJFET epitaxial doping levels relevant to power switching applications, the built-in gate potential is approximately 2.7 V as illustrated in Figure 4 for the 1300 V normally-off vertical-channel JFET. This value is in good agreement with power VJFET gate built-in potentials reported by other groups [2, 10].

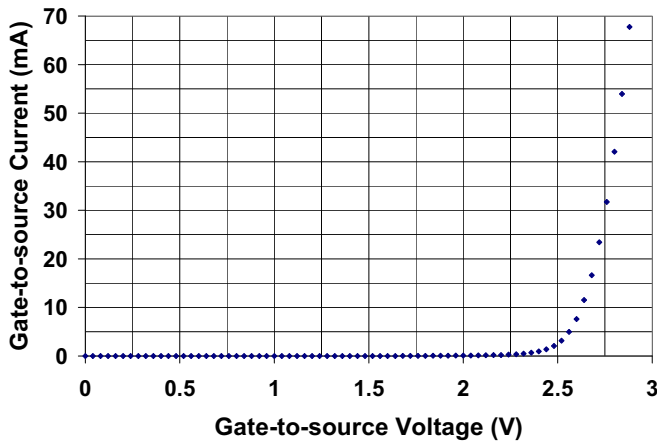


Figure 4. Forward gate-to-source voltage characteristics of the 1300 V normally-off VJFET. The built-in potential of the junction is approximately 2.7 V.

It is obvious from Figures 3 and 4 that 1300 V normally-off VJFET operation at low on-state resistance ($5 \text{ m}\Omega \text{ cm}^2$) requires a gate bias (3 V) in excess of the junction's built-in potential. Thus, a $\sim 1200 \text{ V}$ normally-off vertical-channel JFET is not practical for power conditioning applications. To further illustrate this point, the drain and gate currents of the 1300 V normally-off VJFET were simultaneously measured as a function of drain voltage, Figure 5.

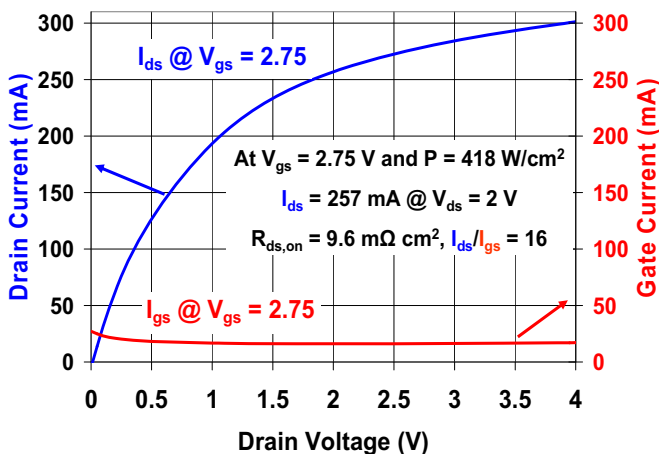


Figure 5. Drain and gate currents versus drain voltage for a 1300 V normally-off VJFET at a gate bias of $V_{gs} = 2.75 \text{ V}$. The specific on-state resistance is $9.6 \text{ m}\Omega \text{ cm}^2$ and the current gain is $I_{ds}/I_{gs} = 16$.

The gate voltage was set at 2.75 V, which lowers on-state resistance to an acceptable $9.6 \text{ m}\Omega \text{ cm}^2$ from its

$23 \text{ m}\Omega \text{ cm}^2$ value at $V_{gs} = 2.5 \text{ V}$. A low current gain of $I_{ds}/I_{gs} = 16$ is measured at this gate bias of $V_{gs} = 2.75 \text{ V}$, for a drain voltage of $V_{ds} = 2 \text{ V}$ and a drain current of $I_{ds} = 0.257 \text{ A}$ (power density of 418 W/cm^2). Consequently, reducing on-state resistance by biasing the gate above its built-in potential lowers current gain to levels impractical for efficient power switching operation.

ALL-SiC NORMALLY-OFF CASCODE SWITCH

To satisfy the circuit designer requirement for normally-off power switching, high-voltage normally-on and low-voltage normally-off VJFETs were connected in the cascode configuration. This creates a power switch with control specifications similar to those of silicon MOSFETs and IGBTs [11]. A schematic of the cascode switch and its constituent VJFETs are shown in Figure 6.

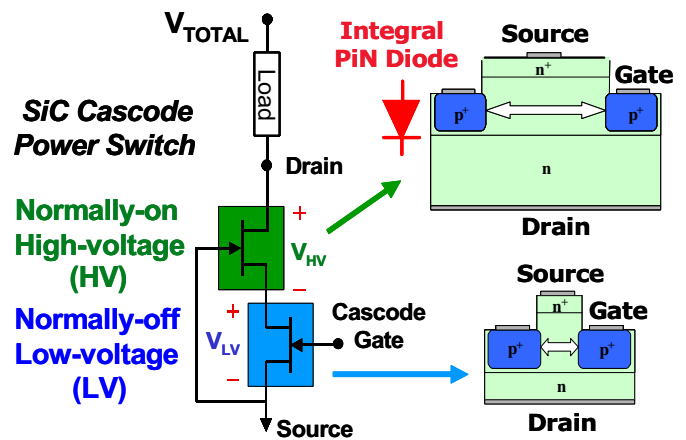


Figure 6. Schematic of Northrop Grumman's all-SiC power switch consisting of high-voltage normally-on and low-voltage normally-off VJFETs connected in the cascode configuration.

In the cascode configuration and with the low-voltage VJFET being biased in the on state, the high-voltage and low-voltage VJFETs operate in series, with the gate-to-source junction of the high-voltage SiC VJFET automatically biased at a voltage value equal to the negative of the drain-to-source voltage drop across the low-voltage VJFET. Because of this negative bias on the high-voltage VJFET's gate, care must be taken to minimize the voltage drop of the low-voltage JFET during the on-state. In the off state, the low-voltage VJFET's drain-to-source blocking voltage provides the necessary negative gate bias to pinch off the high-voltage VJFET. After the high-voltage VJFET is pinched-off, further increase in reverse voltage at the drain of the cascode is supported by the high-voltage VJFET.

The VJFET based all-SiC switches are voltage-driven, and have exhibited excellent power switching characteristics including low on-resistance, high speed, and low switching losses [12]. A typical blocking curve