

Systems to Silicon: A Complete System Approach to Power Semiconductor Selection for Environmentally Friendly Vehicles

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Charles Sullivan, Robert J. Campbell and Tanto Sugiarto
Delphi Corp.

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ABSTRACT

A complete system approach to power semiconductor analysis and selection is set forth in this paper. In order to address design overkill, a suitable power profile across the desired drive schedule is obtained through vehicle simulation in lieu of worse case operating conditions. The representative profile is then applied to detailed models of the inverter, power device, and power device thermal stack-up in order to predict worse case, silicon junction temperature rise. The simulation stream includes a closed silicon thermal loop that leads to more accurate power loss and junction temperature calculations. The models are combined and exercised in a single platform for ease of integration and fast simulation. Herein, the methods will be applied to a working example of an inverter for motor drives, and analytical results will be reviewed.

INTRODUCTION

As the market for hybrids and fuel cell vehicles continues to grow, the utilization of power electronics is also expanding. Power electronics systems for the green market primarily include, but are not limited to, DC-DC converters, chargers, and inverters for motor drives. High voltage and high current power semiconductors are critical components therein and are major contributors to the cost of power electronics systems for environmentally friendly vehicles.

The selection of power semiconductor devices for green technologies is a crucial step in the design of power electronics systems. It is imperative that the power semiconductor solution is optimized for price, functionality, and reliability. Packaging constraints for manufacturability and thermal integrity are vital considerations. Often the choice of power semiconductor devices is based on prior art

and previous converter design iterations. However this approach is arguably heuristic and iterative in nature. Emphasis is placed on thermal characterization of previous design iterations, wherein analysis is extrapolated to new worse-case power loss requirements. This may lead to design overkill with excess thermal capability and added cost.

Herein is set forth a practical method of assessing junction temperature rise across a drive cycle for power semiconductor devices. Historically this type of analysis has invoked some form of Finite Element Analysis. Such an approach requires hours and sometimes days for completion. As detailed in this paper, a single simulation platform, Matlab Simulink, is utilized to bring all system components together, yielding fast simulation and quick design iteration analysis. The paper is organized as follows: First, an overview of the analytical approach is reviewed, followed by brief a description of each principle component. A more detailed review of applying frequency domain derived transfer functions for thermal modeling is provided, followed by a discussion on power silicon characterization and test. The various strategies and components are then pulled together in a working example, highlighting the flexibility and speed associated with this approach.

SYSTEMS TO SILICON APPROACH

The primary goal for this study is to predict maximum junction temperatures for the inverter power silicon devices across the desired operating profile. The desired operating profile may represent a typical vehicular driving schedule of interest or may represent a continuously applied set of worse case operating current and voltage conditions. The focus for this paper will be the former, wherein the system approach to estimating junction temperatures across the desired drive profile will be developed.



In order to assess junction temperature rise, losses for the power semiconductor devices must be established. This power vs. time profile is then applied to the power device's thermal model in order to calculate or simulate thermal response. Construction of realistic power profiles is necessary in order to avoid over-design of excessive thermal capacity or capability with added cost. The power profile for the power device is derived primarily from the utilization of the inverter and machine combination across the targeted vehicular driving schedule. Particularly, the contribution of the power electronics system toward vehicle propulsion and energy capture across the drive profile will yield a characteristic pattern of inverter current and voltage vs. time. Temperature dependent device parameters also influence device power loss, junction temperature rise, and in turn device parameter characteristics. The analysis described herein takes temperature dependence into consideration by actively modeling the effects of temperature on device loss-related parameters.

In summary, the process of estimating power silicon junction temperature rise over a drive cycle comprises the follow steps:

- Construction of accurate vehicle model, including accurate propulsion system component models
- Vehicle simulation across the targeted schedule to obtain realistic profiles of inverter input voltage and machine torque vs. time.
- Reverse mapping of machine performance to obtain profile of machine phase current vs. time.
- Application of inverter model to obtain power semiconductor switch and diode utilization.
- Application of power semiconductor models to obtain profile of device power vs. time.
- Application of power profile to obtain estimation of junction temperature vs. time; temperature is fed iteratively back into power semiconductor model for junction temperature compensation.
- model for junction temperature compensation.

SYSTEMS TO SILICON MODELING STRUCTURE

The principle components in the Systems to Silicon approach are the vehicle model, the inverter electrical device model, and the power device mechanical stackup (thermal) model, as shown in the analysis block diagram of [Fig. 1](#).

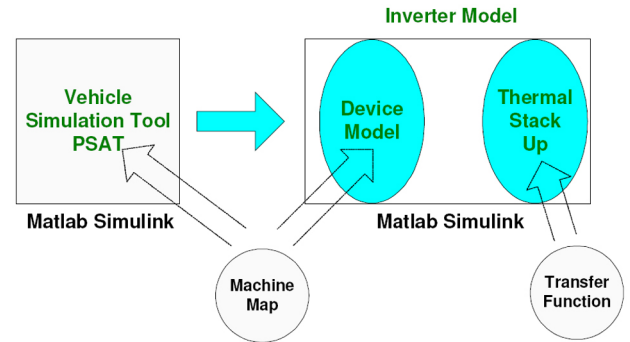


Fig. 1. Sys-to-Si Analysis

Vehicle Modeling and Drive Cycle Analysis

Vehicle simulation is performed using the Powertrain System Analysis Toolkit, or PSAT, developed by Argonne National Labs for Hybrid Electric Vehicle simulation. The tool comes available with a number of vehicle configurations and powertrain component options that one might commonly find in the HEV market. The user can customize the vehicle parameters, engine type and size, powertrain configuration (conventional, parallel hybrid, series hybrid and split architectures), mechanical and electrical accessory loads, and drive cycles. Vehicle parameters such as mass, tire size, and aerodynamic drag coefficient can be tailored for small, mid-size, full-size, truck, and commercial vehicles. The tool is Matlab Simulink based. The Simulink component and control modules are accessible and can be modified to further customize components and hybrid controls. The tool offers a number of standard US, European and Asian drive cycles.

The system model is not overly stiff; however the vehicle equations of motion represent true vehicle dynamics based on vehicle mass and applied wheel torque. Components are constructed to model specific steady state operating conditions but are applied in continuous fashion at each simulation interval. Simulation then yields a series of steady state operating conditions for each component, strung back to back without component dynamic modeling. This is acceptable however, as the time constant of the power device thermal transfer function appears as a low pass filter to the higher frequencies associated with actual component dynamics. Furthermore, the change in applied power is naturally limited by the time constants associated with the propulsion machine's stator and rotor. So it is assumed that power is constant between PSAT output samples, applied in stair step fashion. Accordingly, from the perspective of the thermal model, inverter device current is also assumed to be non-varying between discrete samples.

PSAT is flexible and reconfigurable, but care must be taken to construct accurate component models in order to extract a

legitimate machine power profile. As described briefly in subsequent sections, phase currents are extracted from the machine power profile, and the inverter model is then applied in order to estimate device power loss averaged across inverter PWM switching cycles. Phase currents, inverter input voltages, and thus device average power are assumed constant between each output sample. Inputs to the PSAT vehicle model include vehicle and component parameters, a machine operating and efficiency map, and a drive cycle of choice; the output from PSAT is a profile of machine power vs. time.

Machine Performance Mapping

An accurate machine model is a vital part of the complete system. The machine is represented with capability curves and efficiency maps across the expected range of operating conditions. These curves are pre-generated uniquely for each machine candidate using Matlab script files based on accurate behavioral models incorporating non-linear and magnetic saturation effects. As such, time simulation yields a string of steady state machine operating points. It should be noted that the inverter is not specifically modeled in this system approach, but rather the machine efficiency maps are scaled appropriately by expected inverter efficiencies across the range of operating conditions.

The machine model inputs for this system are torque demand from the HEV controller, machine rotor speed as determined from vehicle and or engine speed via the transmission configuration, and inverter bus voltage. The machine model then calculates constraints based on allowable dc input power and maximum shaft output power and returns applied shaft torque and associated dc power.

Upon completion of system simulation, the machine map is inversely applied to the resultant string of machine operating conditions during post processing to obtain phase current, inverter device modulation index, and inverter power factor profiles across the drive schedule in order to calculate power semiconductor device power.

Inverter Device Model

Using input profiles of bus voltage, phase current (I), modulation index (MI), and power factor (pf) along with switching frequency (fsw), power switch (i.e. IGBT, MOSFET) and power diode losses are calculated. Specifically, switch and diode conduction losses are derived from calibrated functions, $F(I, I_2, MI, pf)$, using temperature calibrated device parameters (i.e. saturation voltage V_{sat} , diode forward voltage drop V_f). Likewise, power device and diode switching losses are derived from simple, calibrated functions, $F_{sw}(f_{sw}, I, \text{bus voltage})$ using temperature calibrated device parameters (i.e. IGBT turn-on energy E_{on} , IGBT turn-off energy E_{off} , and diode reverse recovery energy Err).

Junction temperature (T_j) is a critical component for accurate device parameterization and modeling. Particularly, E_{on} , E_{off} , Err , V_{sat} , and V_f require careful characterization, yielding precision 2nd and 3rd order parameter equations with coefficients that vary appropriately with temperature, current, and voltage. A more detailed treatment of the power semiconductor characterization approach is given below in POWER SILICON CHARACTERIZATION. This process yields temperature compensated, device power loss that will be subsequently applied to the power semiconductor thermal stack-up model for estimating junction temperature. At each time step, junction temperature T_j is fed back into the empirically derived parameter curve-fit equations to model device parameter temperature sensitivity. Data point interpolation is used to enhance accuracy if the parameter curves are well behaved and accurately characterized.

Inverter Model Thermal Stack-Up

The thermal stack-up for each power device is modeled in the time domain with a frequency-domain derived transfer function obtained via FEA (finite element analysis). A more detailed description of this approach and a discussion of the benefits therein are given below in FREQUENCY DOMAIN DERIVED THERMAL TRANSFER FUNCTION. The transfer function block accepts power from the inverter device model and outputs device junction temperature; e.g. from the power loss values calculated for the current time-step, the thermal interface model is used to calculate the resulting T_j increase or decrease. This T_j value is then fed back in order to adjust temperature-dependent device parameters for power calculations during subsequent time steps. In this way the intended goal of T_j prediction across a drive cycle is achieved, enhanced for accuracy and proper convergence through implementation of junction temperature feedback for proper scaling of temperature-dependent parameterization.

Overall System Data Flow Diagram

The flow of data between major components for the Systems-to-Si approach depicted in [Fig. 1](#) is shown below in [Fig. 2](#). Without further description, the various component inputs and outputs as set forth in the previous sections are identified [Fig. 2](#).

POWER SILICON CHARACTERIZATION

A vital element for accurate power loss estimation is to know exactly how the power semiconductor devices react over a range of voltages, currents, switching rates (di/dt 's and dv/dt 's), temperatures, and gate drive conditions. This list of variables could require a tremendous amount of characterization testing to occur so some simplifications are necessary. The parameters of interest for the IGBT include

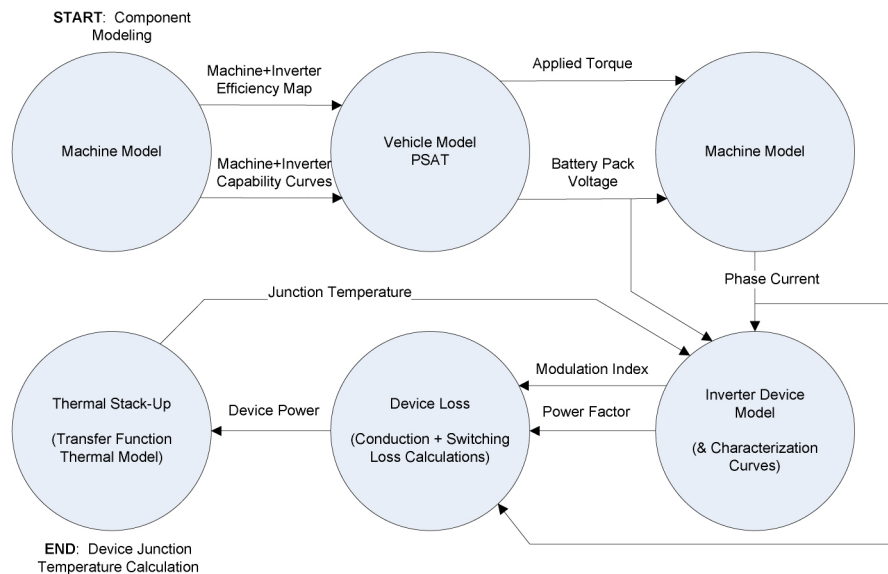


Fig.2. Sys-to-Si Analysis

turn on energy (E_{on}), turn off energy (E_{off}), and collect to emitter saturation voltage (V_{sat}). The parameters of interest for the diode include reverse recovery energy (E_{rr}) and forward voltage drop (V_f). In general, all IGBT parameters may be replaced with their corresponding MOSFET parameters for this analysis.

In general, each application has a unique operating voltage and current range. However, if the semiconductor characterization envelop is wide enough, most applications can be covered. It is recommended to select at least four voltage and current characterization points each in order to capture any non-linearities or unusual behaviors that may affect the accuracy of the power loss simulation. Most power stages are designed with a specific current switching rate in mind (di/dt). The di/dt rate is usually bounded on the low side by excessive switching losses and on the high side by overshoots caused by parasitic inductances or EMI generation. Designers have a target di/dt in mind that is deemed to be the optimal for most designs. The semiconductor devices should be characterized at this optimum di/dt rate with the option of gathering data at rates half and twice as fast. The gate drive circuitry should be designed to allow these optimal di/dt rates to be achieved by changing resistor values. The last variable of interest is junction temperature (T_j). In most power semiconductor device technologies, the loss parameters are sensitive to T_j . Some parameters may have a positive temperature coefficient and some have a negative temperature coefficient. If one makes an assumption that the loss parameters do not change over temperature, large errors in the power loss simulation will occur. Therefore, it is recommended that loss parameters be characterized at a minimum of three junction temperatures. These temperatures can be 25°C, the highest coolant (for liquid systems) or ambient (for air systems)

temperature, and the highest allowed operating junction temperature. Having loss parameters at these three temperatures will result in accurate efficiency modeling over various drive cycles. Worse case T_j analysis can also be determined.

Before the loss parameters can be measured, they must have agreed upon definitions. Proposals and justifications for each major loss parameter are discussed below.

V_{sat} and V_f

The on-state conduction losses for the IGBT and Diode should be measured carefully on semi-automated test equipment that uses current pulses in order to avoid self heating of the junction during characterization. The characterization can be performed with the nominal gate drive voltage level. Adjustments for various gate drive voltage levels can be made at a latter time during worse case analysis. It is important to insure that the current levels adequately cover the entire operating range with some over ranging at the top end. The worse case T_j will usually occur at the highest current level and the most sensitive system level efficiency points will usually occur at low current levels. While a linear curve fit is usually adequate for most modeling, care must be taken to insure that the curve fit is accurate down to the current level where efficiency measurements are critical. If a linear model will not suffice, a two piece linear model or a polynomial curve fit may be necessary. V_{sat} and V_f curves should be generated for the various T_j levels described above.

Turn off Losses

Fig. 3 below illustrates the proposed definition for the turn off loss, E_{off} .