

A New Policy for COTS Selection: Overcome the DSM Reliability Challenge

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ABSTRACT

Up to now, the reliability achieved by COTS components was largely sufficient for avionics, in terms of failure rate as well as time to failure. With the implementation of new and more integrated technologies (90 nm node, 65 nm and below), the question has arisen of the impact of the new technologies on reliability. It has been stated that the lifetime of these new technologies might decrease. The drift is expected to be technology dependent: integration, technology node, materials, elementary structure choices and process play a key role. Figures have been published, which give smaller lifetime than the 30 years generally required for avionics. This would of course impact not only the reliability, but also the maintenance of COTS-based avionics. Hence a new policy should be defined for the whole COTS supply chain.

Faced with these impending risks, different methodologies have been developed [1], [2]. As far as EADS is concerned, we launched a study based on a Physics-of-Failure approach to assess the risks linked to the use of these technologies. Reliability may only be assessed if the end-user describes his mission profile, in which the COTS will be deployed. This is not enough: the COTS technology should be known in detail to choose the relevant parameters for the degradation models of the failure mechanisms, which are both possible and relevant in this usage environment.

This paper presents the methodology with relevant simulation and experiments, supported by an application case.

INTRODUCTION

The electronics COTS components used in avionics so far were reliable enough in terms of failure rate as well as time to failure. However, the implementation of new and more integrated technologies (technology node 90 nm, 65 nm and below) raised some questions whether this will still be the case [3]. The impact may be on failure rate (for the random failure mechanisms) and / or on time-to-failure (for the wear-out failure mechanisms).

As shown on [Figure 1](#), the lifetime of these new technologies might decrease. In average, the smaller the technology node, the shorter the lifetime is. As exhibit, figures are smaller than the 30 years lifetime generally required for avionic applications. This would of course impact not only the reliability, but also the maintenance of COTS-based avionics.

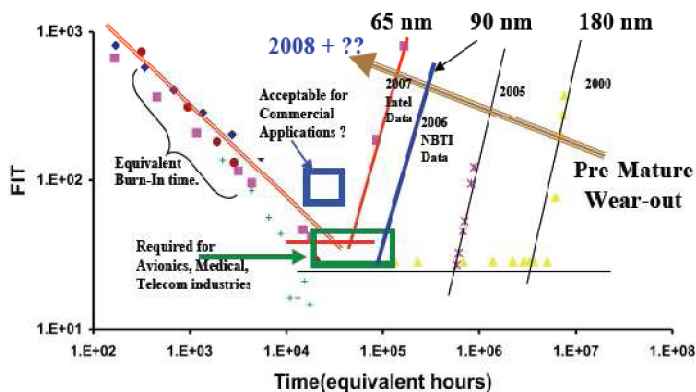


Figure 1. Reliability bath curves plotted for nodes 180, 90 and 65 nm [4]

Different methodologies have been developed to manage this reliability risk. A study based on a Physics-of-Failure approach to assess the risks linked to the use of these technologies has been performed by EADS according to potential impact on avionics. To assess the reliability, end-user has to describe his mission profile and more precisely specific mission profile for the COTS that will be used. In order to choose the relevant parameters for the degradation models of the failure mechanisms, which are both possible and relevant in this usage environment, the COTS technology must be known in detail.

The first part of the presentation will detail the risk analysis that EADS IW proposes on DSM (Deep Sub Micron) components, based on the above three pillars: the mission profile, the description of technology nodes and the most relevant failure mechanisms. The expected lifetime in different usage profiles have been simulated. The dependence of lifetime on technology nodes will be presented and discussed, and the most relevant failure mechanisms will be highlighted.

One of the difficult tasks in testing such VLSI is the choice of the acceleration means. The more relevant acceleration factors are frequency and temperature. Voltage is not relevant, because embedded converters protect the most sensitive transistors from the power voltage. Frequency is highly relevant, because it discriminates between two important failure mechanisms: HCI and NBTI. Temperature is another challenge, because one must apply a temperature on components and avoid testing the supporting board in the same time. The second part of the presentation will highlight the innovation that has been specifically developed to apply locally the minimum and maximum temperature. The detail the test bench that has been specifically defined and put in place to accelerate the failure mechanisms of interest will be described in this part.

Finally, the experimental points will be compared to the simulations. In order to do that, acceleration factors should be

derived. The acceleration factors are calculated based not only on bibliographical data and mission profile, but also on a detailed description and understanding of the technology nodes and the underlying process dependences through the use of the main parameters. The comparison is a proof of the relevance of the methodology that should now be further improved, to become more industrial. A short prospect for future developments will also be given in the paper.

RISK ANALYSIS

We propose a methodology specially adapted for end users. In the field of component selection, end users generally want to evaluate the potential reliability risks in mission before choosing a component. This task becomes harder and harder due to the wide range of technologies available on the market and, above all, owing to the lack of field returns in application. The particularity of our approach is to consider the impact of technology and environment on component lifetime. For that purpose, a list of the most relevant failure mechanisms is set up at silicon level. Then, the associated degradation laws and parameters are selected according to the component technology and mission stresses. Next, mean-time-to-failure (MTTF) are computed for each failure mechanism and compared to the lifetime requirement of the application.

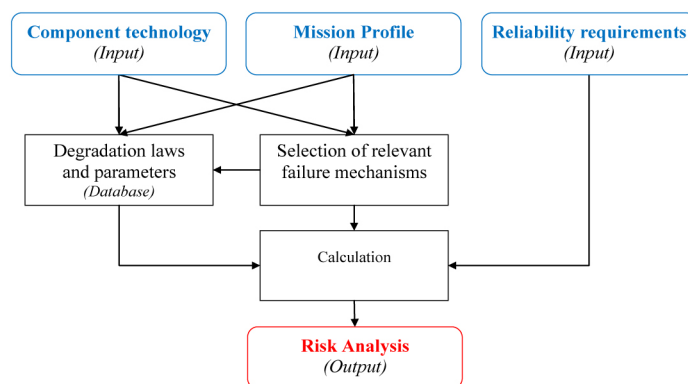


Figure 2. Risk Analysis methodology of Deep Sub Micron components

1. COMPONENT TECHNOLOGY

The first step of the methodology is to collect pieces of information related to the technology of the component. If some data are provided in qualification reports, many of them are missing. To go through, we have to proceed to some reverse engineering at silicon level. The aim is to set up a component identity card of the Back End of the Line (BEOL) and Front End of the line (FEOL) levels. Basically, the required parameters are:

- The generation node (half pitch parameter),
- Number of metallic layers, materials and dimensions of metallization and interconnects,



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- Material and dimensions of transistor,
- Substrate type (silicon on insulator or massive bulk).

The chosen component to test the methodology is a 90 nm SRAM. A construction analysis has been performed at both BEOL and FEOL levels, in order to extract the component technology and the material used (see figures 3 and 4). At BEOL level, the integrated circuit has been designed with 2 layers of metallization isolated thanks to SiO₂ interlayer oxides. The metal-2 (M2) and metal-1 (M1) layers have been manufactured with 2 layers of aluminum covered with 55 nm of titanium barrier layer. The local connexion mainly used for bias distribution and head-to-tail connection of inverters in 6T cell, is made of tungsten. The half pitch of 90 nm measured at M1 level confirms the technological node of 90 nm for this component. Concerning the FEOL, the memory cell is composed of 6 MOS-based transistors, *i.e.* 2 NMOS of access (N₅ and N₆ in Figure 4), 2 head-to-tail inverters with 2 pull up PMOS (P₃ and P₄) and 2 pull-down NMOS (N₁ and N₂). For the transistors designed in the inverters, the drawn gate-length is 90 nm and gate is in poly-Si. The SiON gate oxide gives an equivalent oxide thickness (EOT) of 2.3 nm.

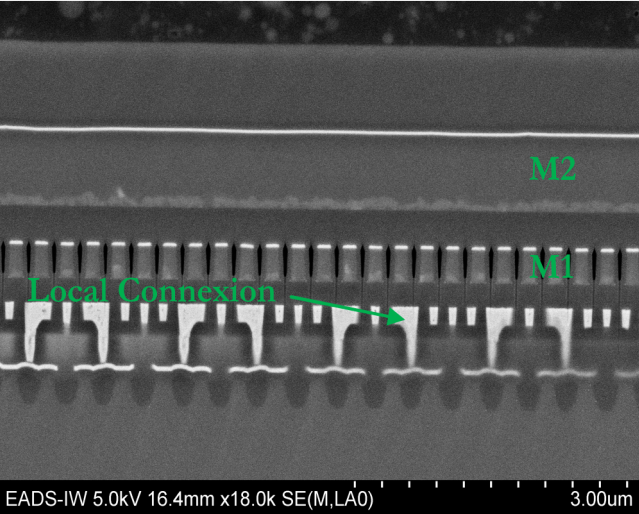


Figure 3. Cross-section of the 90 nm SRAM

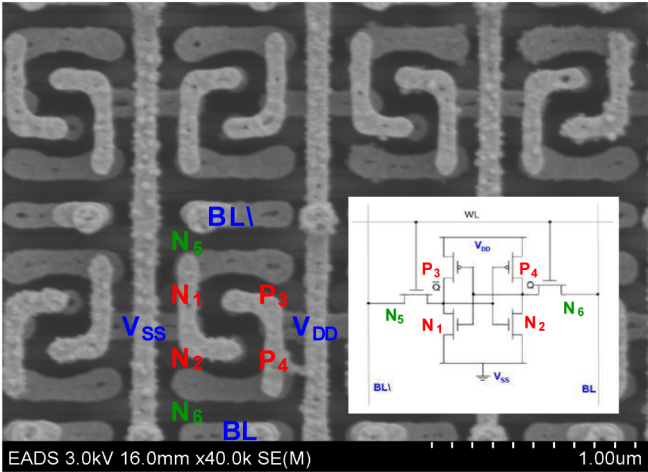


Figure 4. Overview of the transistor level of the 6T cells, with the corresponding electrical scheme

2. MISSION PROFILE DESCRIPTION

The next step is to get access to the condition of use, the environment and external factors that may induce a component functional failure. For this work, we consider that the SRAM is assembled in a computer located in an avionics bay of middle range aircraft. The functioning mission profile of the computer is indicated in Table 1. For this application, 3 flights a day are considered with 2 layovers of 2 hours each (see figure 5). The plane is operated 350 days a year with a duration functioning goal of 30 years. We assume that the 6T-cell is biased when the computer is turned ON, that is representing a worst case comparing to real conditions of solicitation.

Many external stresses may coexist in aeronautics: vibration, thermal cycling, fog salt and radiations. That is why the field is considered as harsh environment. Nevertheless, in addition to the electric stress, temperature seems to be the most critical ageing factor at die level. For this application, the computer temperature ranges from 15°C to 30°C in mission. Besides, the power dissipation for this SRAM is around 25°C. Hence, the junction temperature in mission as described in Figure 5 is going from 40°C to 55°C. With these considerations, the memory cell is biased in mission for 165 900 h at 40°C and during 42 000 hours at 55°C. Those data will be used in simulation afterwards.

Table 1. Function mission profile

	Mission profile	
State of computer	Computer OFF	Computer ON
Frequency of use	4.2 hours a day	19.8 hours a day
	350 days a year	
	30 years	