

High Current (>1000A), High Temperature (>200°C) Silicon Carbide Trench MOSFET (TMOS) Power Modules for High Performance Systems

Brice R. McPherson, Robert Shaw, Jared Hornberger, Alex Lostetter, Roberto Schupbach, Brad Reese and Ty McNutt
Arkansas Power Electronics International

Takukazu Otsuka, Yuki Nakano and Takashi Nakamura
Rohm Co., Ltd.

ABSTRACT

The demands for high-performance power electronics systems are rapidly surpassing the power density, efficiency, and reliability limitations defined by the intrinsic properties of silicon (Si) based semiconductors. The advantages of silicon carbide (SiC) are well known, including high temperature operation, high voltage blocking capability, high speed switching, and high energy efficiency. These advantages, however, are severely limited by conventional power packages, particularly at temperatures higher than 175°C and >100 kHz switching speeds. Here, APEI, Inc. presents the design process and testing data of its newly developed high performance HT-2000 SiC power module for extreme environment systems and applications. This advanced power module, targeted for high performance commercial and industrial systems such as hybrid electric vehicles or renewable energy applications, implements a novel low parasitic packaging approach that enables high switching frequencies in excess of 100 kHz. High temperature functionality offers system level gains in power density (reducing heat sink volume and mass), and allows service in high ambient temperatures, such as under the hood of a vehicle. The power module contains sixteen state-of-the art 900V SiC Trench MOSFET devices developed by ROHM Co., Ltd, and features an ultra-low on resistance (~1.5 mOhm per switch position), extremely fast switching speeds (in the 10s of nanoseconds), and low switching energies. High current (>1500A) and high temperature (up to 200°C) curve tracing results will be discussed, including on-state characteristics, on-resistance vs. drain current, reverse and gate leakage, and high speed switching curves.

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INTRODUCTION

Wide band gap materials, such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are ideal for next generation power devices, offering superior performance in comparison to traditional Silicon (Si) based switches. In particular, substantially higher voltage breakdown strengths allow devices to be fabricated with blocking layers up to an order of magnitude thinner, directly reducing channel resistances and increasing switching speed. SiC based devices, in particular, are a maturing technology with a growing selection of power components (diodes, MOSFETs, JFETs, and BJTs) available on the commercial market from a diversity of vendors [1][2][3]. SiC has a thermal conductivity ~3x higher than Si and

GaN, can theoretically operate at temperatures up to 600°C (compared to ~150°C for Si), and can be formed into vertical channel device structures to minimize on-resistances.

While the intrinsic features of SiC combined with advanced device design and fabrication techniques have created power switches with unprecedented levels of performance, their true potential is drastically hindered by conventional power packages, materials, attaches, and layout techniques. In order to unlock the revolutionary performances promised by SiC, the power packaging, gate drive, bussing, heat removal, and control systems must be specifically designed around high temperature wide band gap technology. With these tools, a system level designer may significantly increase the efficiency and reduce the weight and volume of

the entire power conversion system (motor drives, inverters, battery chargers, etc.). This includes a reduction of the power module itself, reduced size or complexity of the heat removal system (heat sink, cold plate, etc.), decreased passive filtering and magnetics (due to high frequency switching), and placement in high ambient environments (such as under the hood of a vehicle) without the need for bulky thermal isolation. There are numerous applications which may take advantage of these features, notably including commercial and military vehicular motor drives, avionics systems, solar and wind grid tie inverters, down hole geological exploration electronics, and power supplies for satellite systems.

With this mindset, APEI, Inc. has developed the HT-2000, a high temperature high performance power module expressly designed to embrace the benefits and challenges of SiC power devices. The HT-2000 is high temperature (up to 250°C), high current (100->1000A, depending on device type, performance, topology, and cooling method), and low inductance (allowing for high frequency switching). It is designed to be adaptable to a variety of performance requirements, capable of paralleling a large number of devices (or any switch type) with a proprietary layout technique which provides equal current sharing and simultaneous switching events.

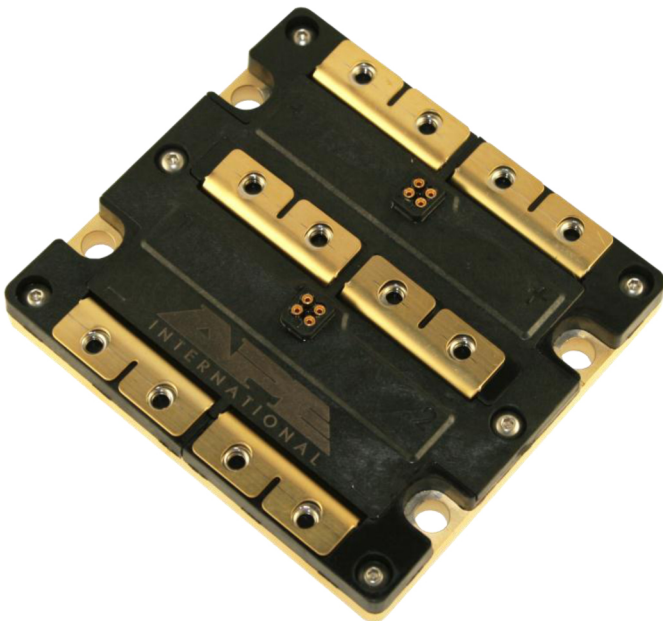


Figure 1. The HT-2000 power module developed for advanced wide band gap power electronics.

These power modules are rated to 1200V, are operational at very high currents, offer a low thermal resistance ranging from 0.12 to 0.17°C/W (depending on the size and number of devices paralleled internally), can perform at temperatures in excess of 250°C, and are designed to house various SiC devices, including MOSFETs, JFETs, or BJTs. It is configurable as either a half or full bridge converter. It weighs just over 130 grams with a volume of 67cm³ (offering

a $\sim 3\times$ mass reduction, $\sim 2.6\times$ volume reduction when compared with similarly rated state of the art Si Trench IGBT based systems).

This discussion begins with an overview of the newly developed SiC double trench MOSFET produced by Rohm, Ltd., followed by an examination of the package design process and key highlights of the HT-2000 power module, and concluded with relevant high temperature (up to 200°C) characterization and high current (up to 1500A) testing of the HT-2000 module populated with sixteen TMOS devices.

BODY

Trench MOSFET Overview

In a standard vertical power MOSFET, the gate structure is planar. This introduces a region where the current must travel laterally before it may move vertically through the channel. As a result, this path produces an internal normally-on JFET region in the structure, which contributes to the overall on-resistance. In Si switches, a technique to circumvent this is to etch trenches in the material (U and V shaped, for example), forming vertical gates which reduces the channel resistance and eliminates the parasitic JFET in the structure. This technique, while effective, introduces a gate oxide reliability issue when high voltages are applied. The corners of the gate trenches are sharp and act as a concentration point for the electric field, and may generate a breakdown if there is a flaw in the oxide. Si has the luxury of a well-developed and reliable gate oxide obtained from decades of research and production, and the ease of etching and processing characteristic of the technology. While the reliability of oxide on SiC has come a long way in the past decade, there are still many issues present under high electrical bias.

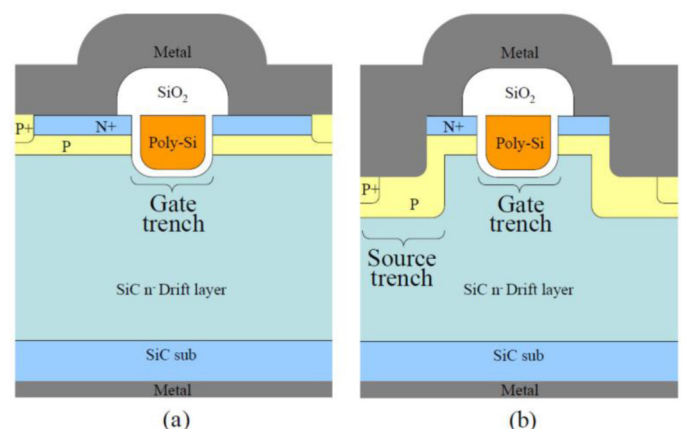


Figure 2. Schematic cross section of (a) a conventional single-trench design and (b) ROHM Ltd.'s double trench structure.

To circumvent this issue, Rohm, Ltd. has developed a novel double-trench device design for their SiC MOSFETs [4]. Figure 2 displays a conventional trench MOSFET

structure (left), and the new double trench design on the right. The key difference is the addition of source trenches around the periphery of the gate trenches. The source trenches act to “buffer” the electric field at the gate (Figure 3), reducing the electric stress at the trench corners and correspondingly improving the reliability of the trench structure.

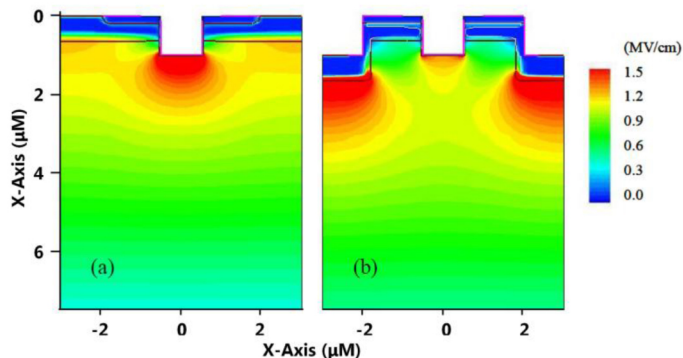


Figure 3. Electric field distribution of the device cross section while blocking for (a) a single trench structure and (b) the double trench device for $V_{DS}=600V$ and $V_{GS}=0V$.

The double trench technique, when applied to SiC, substantially reduces the on-resistance of the device. On-resistance is one of the most critical metrics for a power device, ultimately determining the maximum current the device can carry. The double trench MOSFET devices in production by Rohm, Ltd. offer a truly breakthrough performance and retain the numerous benefits of MOSFET type devices for power, including: normally-off operation, straightforward voltage control and drive, and high speed switching.

HT-2000 Design

Power packaging challenges

The benefits of SiC as a power electronic device are striking; however, to fully capitalize on these advantages, new approaches to the requisite packaging, gate drive, and system level design are imperative. Package limitations are often encountered when driving up the current density (whether by increasing the power for a given footprint or reducing the footprint for a particular power level) and increasing switching speeds due to parasitic impedances in the lead frames and interconnects. Power density and peak temperature are proportional; an increase in one will generate a rise in the other. As a direct result, increasing the operational temperature in power electronics packages is a dominating factor for the next generation of high power density power electronics modules.

Extreme temperature power packaging is an enormous challenge. As the operating temperature rises, traditional packages become incapable of reliably withstanding the exposure. Accordingly, the utilization of high temperature

capable materials, attach processes, minimization of coefficient of thermal expansion (CTE) differences, and forming high current interconnections must be the foundation of any such system. APEI, Inc. has embraced this challenge, aggressively developing extreme environment packaging solutions specifically for SiC and other wide band gap semiconductors. Power systems operating at junction temperatures ranging from 200 to 300°C [5] and extreme environment sensor systems in a 450°C ambient [6] have been demonstrated by APEI, Inc. engineers.

In addition to temperature, parasitic impedances are a pervasive issue in electronic packages, notably for power where current paths are longer and multiple devices may be arranged in parallel. Current sharing during transitional events is a critical issue for large arrays of paralleled devices. In [5], APEI, Inc. engineers demonstrated the benefits of matched power device layouts, performing a study comparing different methods to arrange six devices in parallel. Figure 4 (left) displays the turn-on current values for each device in a linear arrangement and (right) for a more symmetrical ‘forked’ arrangement with pairs of matched current lengths.

As shown, a linear layout of devices results in non-simultaneous switching events, in which the paralleled switches turn on in a cascading fashion, resulting in enormous current spikes and localized heating. By forking the layout and creating matched pairs of devices, the current path length to the furthest device is halved, and the burden is shared by two switches. This considerably reduces switching loss and thermal loading on the devices. Figure 4 is a salient example of the enormous benefits that can be achieved if the magnitudes and distribution of impedances are carefully scrutinized. Further improvements can be made by reducing the length of the current paths by cutting the package height, and improving the effective cross section of the die topside interconnects by paralleling many wire bonds or using a wire bondless style of contact.

HT-2000 design

Power electronic systems are exceptionally diverse, with a wide range of applications, power levels, and environmental conditions complicating the selection of an appropriate packaged module. As such, configuration flexibility is paramount. The HT-2000 power package was devised from the ground-up to be device neutral; the internal interconnection and layouts are compatible or adaptable with most currently or soon to be available SiC devices from a variety of vendors. Newly available devices may rapidly be implemented in these housings with an adjustment to the assembly hardware. It is capable of junction temperatures ranging from 200-250°C, voltages up to 1200V, and currents ranging from 100 to >1000A (depending on the size, type, topology, and number of devices inside).

A novel interconnection scheme is employed which allows arrangement as either a half bridge or full bridge configuration through external bussing. Figure 5 illustrates this approach. There are six external power connectors, two