

CAN FD Network Design Hints and Recommendations

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ABSTRACT

The CAN FD protocol internationally standardized in ISO 11898-1:2015 just describes how to implement it into silicon. The ISO 11898-2:2016 standard specifies the physical media attachment (PMA) sub-layer of the CAN (FD) physical layer. The design of CAN FD networks is not in the scope of these standards. In general, the physical layer design of CAN FD networks requires more attention compared with Classical CAN networks. First recommendations have been developed. Different standardization bodies have already specified or are in the process of specifying higher-layer protocols, for example ISO for on-board diagnostic, ASAM for calibration, etc.

CITATION: Zeltwanger, H., "CAN FD Network Design Hints and Recommendations," *SAE Int. J. Passeng. Cars – Electron. Electr. Syst.* 9(1):2016, doi:10.4271/2016-01-0060.

INTRODUCTION

The CAN FD protocol is an extension of the well-known (Classical) CAN data link layer. The main benefits are a higher throughput and longer data frames with up to 64 byte. One part of the CAN data frame is transmitted optionally with higher bit-rate exceeding the former limitation of 1 Mbit/s. Designing CAN FD networks has some impacts on the physical layer design as well as the software architecture as known from the Classical CAN approach.

THE CAN FD PROTOCOL AND ITS IMPACTS ON THE PHYSICAL LAYER

The CAN FD protocol introduces a second bit-rate to be used in the data phase, when just one node is transmitting bits. All other nodes in the network are receivers. This means, it is not necessary to be synchronized. In this phase there is no in-bit time sampling required as in the arbitration phase, when several nodes are transmitting identifier bits or the ACK (acknowledge) bit. This means, the bit-rate is not dependent on the network length. The network and transceiver propagation delays are not more relevant. The bit-time setting for the data-phase is similar to the arbitration phase. The user needs to configure the time-quantum, the SYNC segment and the sample-point. ISO 11898-1:2015 provides just a framework for the bit-time settings, e.g. to use the same oscillator frequency in all nodes. In order to keep the quantization error as small as possible, it is recommended to use an equal time-quantum length for both bit-rates. ISO 11898-1 contains some formulas to calculate the maximum allowed oscillator frequency tolerance at a given data-phase bit-rate. When the ratio of data-phase bit-rate and arbitration bit-rate is low (e.g. 6:1) the Classical CAN oscillator tolerance is sufficient. For higher ratios, the tolerance needs to be calculated using the referenced formulas.

And, there are some other additional transceiver values to be considered. The bit-width variations, caused by the network topology and the transceiver features are relevant. The bit-width variation is determined by the interface between the CAN controller (often integrated in the micro-controller) and the CAN transceiver, the CAN transceiver itself (asymmetry of transmitting and receiving), and the reflections depending on the chosen network topology and the impedance of the selected components (e.g. cable and connectors, etc.).

Edition 2016 of the ISO 11898-2 standard (merging the legacy ISO 11898-2, -5, and -6 standards) specifies the transceiver characteristics. There are three new parameters of interest: the loop-delay from TxD to RxD, the Tx delay, and the Rx delay. The transceiver loop-delay is the time between receiving the bit at TxD and transmitting it at RxD from the viewpoint of the transceiver. The recessive-to-dominant edge is measured at 30 percent and the dominant-to-recessive edge at 70 percent. The symmetry for both delays is important for the transmitting node. The most critical situation is the recessive bit after five dominants. If the transceiver is very asymmetric, the recessive bit-time is shortened or expanded in relation to the nominal bit-time. Therefore the ISO 11898-2:2016 standard specifies the minimum and maximum values for recessive bits as shown in [Table 1](#). The values are given for a network load on the bus-lines (CAN_H and CAN_L) of 60 Ω and 100 pF.

Table 1. Loop-delay symmetry (source: ISO 11898-2:2016)

Bit rate (data-phase)	$t_{BH(RXD)}$ min	$t_{BH(RXD)}$ max	t_{bit} (nominal)
1 Mbit/s	n. a.	n. a.	1000 ns
2 Mbit/s	400 ns	550 ns	500 ns
5 Mbit/s	120 ns	220 ns	200 ns

The allowed transmitter supply voltage tolerance, the network load, and temperature effects cause this asymmetry. In order to reduce the emission the transmitter controls the slew-rate of the falling and rising edge to the lowest value possible at a given bit-rate. Table 2 shows the specified values as given in ISO 11898-2:2016 for a network load on the bus-lines (CAN_H and CAN_L) of 60 Ω and 100 pF.

Table 2. Transceiver Tx delay symmetry (source ISO 11898-2:2016)

Bit rate (data-phase)	$t_{\text{Bit(Bus) min}}$	$t_{\text{Bit(Bus) max}}$	$t_{\text{bit (nominal)}}$
1 Mbit/s	n.a.	n.a.	1000 ns
2 Mbit/s	435 ns	530 ns	500 ns
5 Mbit/s	155 ns	210 ns	200 ns

The transceiver Rx delay depends on production dispersion, temperature variation, receiver thresholds, supply voltage variation, and the slew rate. The delay is a calculated value as given in Table 3. The $\Delta t_{\text{Rec(min)}}$ value shortens the recessive bit-length and $\Delta t_{\text{Rec(max)}}$ lengthens the recessive bit-length.

Table 3. Transceiver Rx delay symmetry

Bit rate (data-phase)	$\Delta t_{\text{Rec (min)}}$	$\Delta t_{\text{Rec (max)}}$	$t_{\text{bit (nominal)}}$
1 Mbit/s	n.a.	n.a.	1000 ns
2 Mbit/s	-65 ns	40 ns	500 ns
5 Mbit/s	-45 ns	15 ns	200 ns

Figure 1 shows the impacts between the TxD signal of the transmitting node, the V_{diff} differential bus voltage, and the possible recessive bit-time duration at the RxD pin of the receiving node. The rising edges can jitter, and the falling edges are stable.

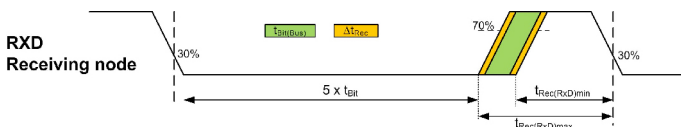


Figure 1. Jitter of the rising edge at a receiving node's RxD pin (source: CiA 601-1)

The range marked in green is the variation of the transmitter and the range marked in yellow is the variation of the receiver. To calculate the worst-case scenario, both parameters are added [2].

CAN FD nodes with configured data-phase bit-rate of 1 or 2 Mbit/s should use transceiver chips compliant to ISO 11898-2:2016 qualified for 2 Mbit/s. Nodes using a data-phase bit-rate of 5 Mbit/s should implement transceivers qualified for 5 Mbit/s as specified in ISO 11898-2:2016 or for higher bit-rates (not yet standardized in ISO 11898-2:2016).

CAN FD NODE DESIGN RECOMMENDATIONS

Besides using CAN transceivers compliant with ISO 11898-2:2016, the CiA 601-1 specification gives further hints and recommendations on the design of CAN FD connectable electronic control units (ECU). Figure 2 shows a typical communication network with a transmitting node, a receiving node and the wire in between. The symmetry of the RxD signal on the receiving node is defined by the symmetry performance of the transmitting and receiving node. To guarantee a robust communication between two or more nodes in a network, the transceiver Tx delay symmetry of the transmitting node and the transceiver Rx delay symmetry of the receiving node shall be very accurate. The loop-delay symmetry cannot cover this in total. It could be that one ECU in the network has a transceiver with a very symmetric transmitter part and an asymmetric receiver part. The behavior of a transceiver from another supplier may behave vice versa. Therefore, in CiA 601-1 additional parameters are defined for the transmitter and receiver symmetry.

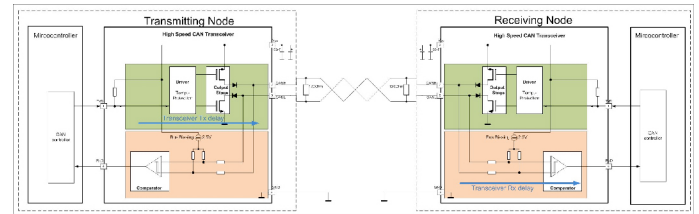


Figure 2. Important delays in a CAN FD network (source: CiA 601-1)

Table 4 provides the resulting min and max values for the recessive bit length seen by a receiving node. They are valid for a 60- Ω and 100-pF busload. The following effects are not considered in this part of the document, but in the CiA 601-4 specification (not yet released): the behavior of the network itself such as ringing or additional propagation delay of the dominant to recessive transition, and clock tolerances.

Table 4. Recessive bit-time at the receiving node's RxD pin (source: CiA 601-1)

Bit-rate (data phase)	$t_{\text{Rec(RxD) (min)}}$	$t_{\text{Rec(RxD) (max)}}$	$t_{\text{bit (nominal)}}$
1 Mbit/s	n.a.	n.a.	1000 ns
2 Mbit/s	370 ns	570 ns	500 ns
5 Mbit/s	110 ns	225 ns	200 ns

The sample-point of the data-phase bit-rate is independent of the arbitration point-rate sample-point. The setting depends on the transmitting node delay (TD). The TD is the delay from the CAN controller's transmit flip-flop (FF) to its receive flip-flop. This means, when the CAN controller sends a bit, this bit appears at the CAN controller's input after TD. This TD is the sum of the following delays:

- Propagation delay from CAN controller Tx-FF output to TxD micro-controller port,
- Propagation delay from TxD micro-controller port to TxD transceiver port,