

Solder Void Modeling and Its Influence on Thermal Characteristics of MOSFETs in Automotive Electronics Module

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ABSTRACT

Current generation automobiles are controlled by electronic modules for performing various functions. These electronic modules have numerous semiconductor devices mounted on printed circuit boards. Solders are generally used as thermal interface material between surface mount devices and printed circuit boards (PCB) for efficient heat transfer. In the manufacturing stage, voids are formed in solders during reflow process due to outgassing phenomenon. The presence of these voids in solder for power packages with exposed pads impedes heat flow and can increase the device temperature. Therefore it is imperative to understand the effect of solder voids on thermal characteristics of semiconductor devices. But the solder void pattern will vary drastically during mass manufacturing. Replicating the exact solder void pattern and doing detail simulation to predict the device temperature for each manufactured module is not practical. Hence different numerical models are studied for the solder, by using single and distributed void patterns matching the percentage void fraction. The numerical studies indicated that distributed void pattern captures the void behavior well compared to single void model. For the MOSFET (Metal-Oxide-Semiconductor-Field-Effect-Transistor) device under study, it is observed that the void percentage up to 20% has negligible impact on device temperature for its maximum rated power. The temperature rise because of increase in void percentage (from 20% to 50%) for different power ratings of MOSFET is discussed in the paper. A risk rating chart is also provided as guideline for solder void rejection.

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INTRODUCTION

Solder voids are gas occlusions that form in solder joints during the soldering process. The voids are caused by the amount of outgassing flux that gets entrapped inside the solder joint during reflow. Voiding is one of the major reliability concerns when solder is used as the thermal interface material. The use of lead (Pb)-free solders has increased concerns emanating from solder voids due to its poor solderability. Studies indicate that in certain Pb-free solders the occurrence of voids can be in excess of 50% of solder volume [1, 2]. The presence of voids in solders reduces the effective area available for heat transfer. This subsequently results in an increase in thermal resistance and rise in chip junction temperature that can lead to temperature related failure mechanisms.

The void formation during manufacturing is almost inevitable due to following circumstances which are impossible to control:-

- Entrapment of gas bubbles formed by reactions among material and fluxes during reflow soldering process
- Poor wetting of solder due to contaminated or defective back side metallization of silicon die or heat spreader
- Solder-alloy fatigue due to cyclic thermo-mechanical stresses experienced during device operation

Solder voids can be classified generally in three ways (there are six groups) as listed below:-

1. Solder wetting point of view
 - Shallow voids (partially wetted)
 - Deep voids (completely not wetted voids)
2. Void Configuration
 - Distributed small voids
 - Large coalesced voids
3. Void Location
 - Corner/edge
 - Centre of the STIM

The various void types have different level of impact on the thermal performance of electronics packaging. The precise thermal behavior evaluation is essential for these different types of void patterns.

LITERATURE SURVEY

An extensive literature survey was carried out to understand the previous works done on solder void modeling. The surveys also aided in understanding the general trend of the void percentage level normally observed in solder joints. Three dimensional finite element modeling was explored by Chang et al. [3] to investigate the effect of

solder void size and location on thermal resistance of power devices. The study suggested that chip temperature and thermal resistance increase with increase in void percentage. Thermal resistance has increased to 6.5% and 27.2% for void percentage of 20% and 79% respectively. Fleischer et al. [4] used experimental and numerical methods to predict the relation between void geometry and package resistance. Thermal resistance has increased to 30% with 73% of random voids. But for contiguous voids of 73%, thermal resistance increased up to 200%. Two dimensional FEA is used by Zhu [5] to study thermal impact of voids on power device. The chip area is around 0.5mm x 0.5mm having power dissipation of 1W. Thermal impedance variation with different classes of voids and void percentage is also highlighted in his work. The result indicated that impact on thermal resistance is greater for larger, coalesced and edge voids compared to small distributed voids. Biswal et al. [6] assessed the impact of solder voids on the silicon die temperature during transient operations of a high power automotive electronic module. The solder voids were modeled explicitly using ANSYS®. It is shown that there is profound impact of solder voids on the silicon die temperature depending on the size and void fraction. But the void distribution seems to have negligible impact on the die temperature. Katsis et al. [7] demonstrated that operation of power semiconductor devices induces thermal stresses resulting in void growth. Commercially available TO-247 style MOSFETs were power cycled, imaged and thermally analyzed to generate a correlation between void percentage and thermal impedance. The void percentage has increased from 10% to 35% for 4000 cycles. Liu Chen et al. [8], performed analysis using ANSYS® to model D²PAK package and calculated 'R_{jc}' for different types of randomly distributed voids using statistical approach. Four different void configurations viz. upper voids, middle voids, bottom voids and through thickness voids are analyzed. The increase in thermal resistance was highest at around 67% for through thickness voids. The upper voids, middle voids and bottom voids experienced the increase in resistance of 62%, 60% and 56% respectively.

The literature survey indicated that void size, void location and void percentage cannot be generalized for all devices and it can vary drastically for the same device during mass manufacturing. The void distribution seems to have less impact on the rise in chip temperature. This means that explicitly modeling the voids may not be essential to capture the real effects. Most of the solder void studies done are in the die-attach regions. It was also noted that through thickness voids has maximum thermal resistance compared to upper voids, middle voids and bottom voids. Hence the current study is focused on solder between the device and the PCB interface regions for through thickness voids. In the present work, different numerical models are attempted to study the void impact by using single and equally distributed void patterns matching the percentage void fraction to replace the time consuming explicit void modeling.

SOLDER VOIDS IN MOSFET

The studies are performed on a MOSFET device (power package with exposed pad) that is very commonly used in automotive electronic modules. The MOSFET has resistance junction to case of

2°C /W and its allowable maximum power dissipation for the present application can vary up to 12W. MOSFET X-ray image with 20% void fraction is shown in [figure 1](#).

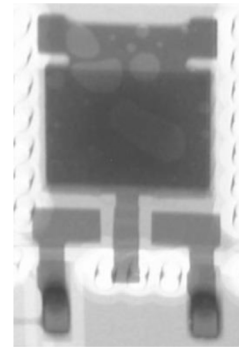


Figure 1. X-ray image of MOSFET

For the present study void percentage range is chosen based on the the solder X-ray images taken for a series of MOSFET. X-ray images indicated that the maximum solder void percentage is around 50% with different sizes of voids. [Figure 2a](#) and [2b](#) shows the solder voids extracted from the X-ray images for 20% and 50% void percentage. For each percentage of voids, two different configurations that are commonly found are chosen. One configuration is corresponding to small distributed voids and other one is large coalesced voids. In the smaller voids, the diameter of voids varies from 0.05mm to 1mm and for bigger voids the sizes greater than 1mm diameter is present.

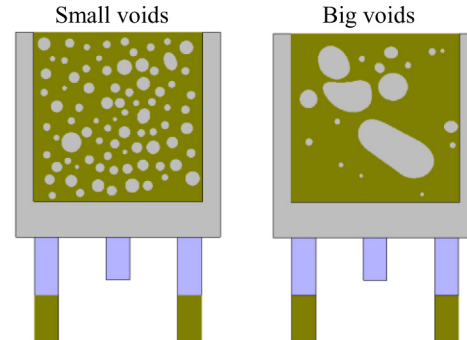


Figure 2a. Solder with around 20% void percentage

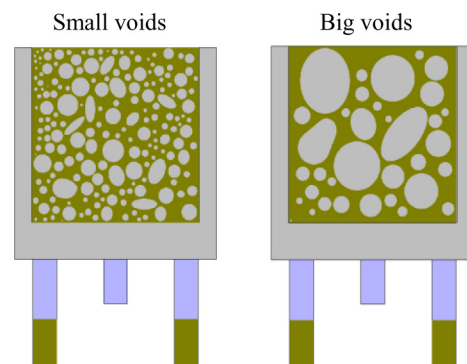


Figure 2b. Solder with around 50% void percentage

BASLINE THERMAL MODEL

Initially to understand the effect of solder void on MOSFET temperatures, steady state thermal analysis is carried out using commercial CAE software package FloTHERM® without solder voids. The thermal model used for simulation is shown in [figure 3](#). This model is used as baseline to compare the temperature increase due to void presence. The internal construction of MOSFET thermal model is shown in [figure 4](#). The baseline thermal model consists of MOSFET mounted at center of PCB of dimension 60mm x 60mm surrounded by ambient air. The solder thickness considered in simulation is 0.1mm. MOSFET device has 22 thermal via underneath the device. Thermal via effect is taken in analysis by appropriately calculating the orthotropic properties. The thermal model developed captured all three modes of heat transfer viz. conduction, convection and radiation. To account for radiation appropriate emissivity properties are applied to the components. PCB and Encapsulant emissivity is assumed to be 0.8. The dimensions of the different components of the thermal model are given in [table 1](#). The thermal conductivity material properties used are given in [table 2](#).

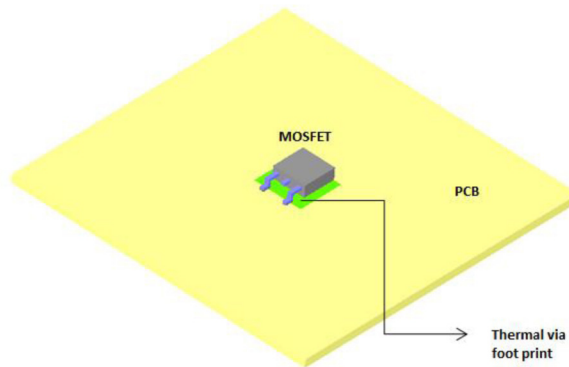


Figure 3. Thermal Model with MOSFET mounted in PCB

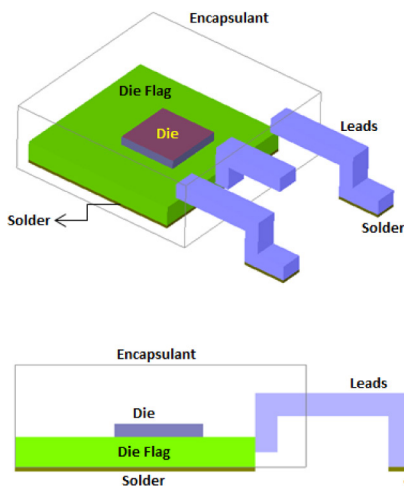


Figure 4. Internal construction of MOSFET thermal model

Table 1. Dimensions of FloTHERM® model

Component	Dimension
PCB	60.0mm x 60.0mm x 1.60mm
Encapsulant	6.54mm x 6.54mm x 2.29mm
Die flag	5.40mm x 5.40mm x 0.67mm
Die	2.00mm x 2.00mm x 0.30mm
Thermal via	8.86mm x 9.42mm x 1.60mm
Solder in FET-PCB interface	5.40mm x 5.40mm x 0.10mm
Solder in Leads	1.52mm x 0.76mm x 0.10mm

Table 2. Thermal conductivity properties

Component	Thermal Conductivity, W/ m K
PCB	In-plane: 61.5 ; Out-Plane: 0.38
Encapsulant	0.65
Die flag	301.5
Die	117.5
Thermal via	In-plane: 61.5 ; Out-Plane: 6.54
Solder in FET-PCB interface	38
Leads	385

The thermal contours of baseline model with 6W power dissipation for 25°C ambient temperature is shown in [figure 5](#).

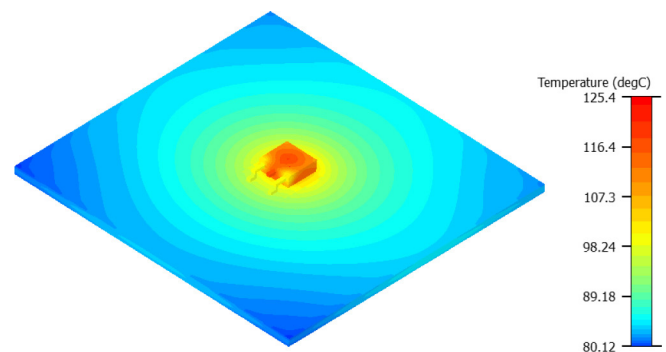


Figure 5. Baseline model thermal contours

DETAIL SOLDER VOID MODEL

From the X-ray images of the solder, it is found that in general, void percentage can vary to a maximum of around 50%. In a detailed solder void model, the voids are explicitly modeled replicating the X-ray images. Thermal analysis is carried out for two different void percentages 20% and 50%. For each solder void percentage, studies are carried out for two void configurations viz. small and big. The void configurations studied are shown in [figure 2a](#) and [2b](#). Thermal studies are carried out using model shown in [figure 3](#). [Table 3](#) provides the consolidated summary of MOSFET temperature rise over ambient for varying power dissipation values (2W to 12W). The simulation results indicated that 20% solder void does not have significant temperature raise compared to that of 'No void' situation