



AEROSPACE STANDARD

AS47643™

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Verification Methods for MIL-STD-1760E Aircraft Station Interfaces

RATIONALE

MIL-STD-1760 has now reached Revision E and has introduced changes to the interface standard such that an updated version of the SAE verification standard is essential.

FOREWORD

This SAE Aerospace Standard (AS) is a document for validating aircraft station compliance with the interface requirements of MIL-STD-1760E. This document was prepared by the SAE AS-1B, MIL-STD-1760 User Task Group to provide industry guidelines to the U.S. Government's MIL-STD-1760E. This document was prepared to minimize unnecessary or undesirable variations in Aircraft Station Interface verification against MIL-STD-1760E. For verification of aircraft designed to MIL-STD-1760A Notice 2 AS4764 Issued 1995-04 applies. For verification of aircraft designed to MIL-STD-1760B Notice 3 AS47641 Issued 1999-08 applies.

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TABLE OF CONTENTS

1.	SCOPE.....	4
1.1	Purpose.....	4
1.2	Application.....	4
1.3	Tailoring.....	4
1.4	Limitations.....	4
1.5	Identification System.....	4
2.	REFERENCES.....	5
2.1	Applicable Documents.....	5
2.1.1	SAE Publications.....	5
2.1.2	U.S. Government Publications.....	5
2.1.3	NATO Publications.....	5
2.2	Abbreviations and Acronyms.....	6
2.3	Definitions.....	8
3.	GENERAL REQUIREMENTS.....	8
3.1	Introduction.....	8
3.2	Verification Techniques.....	8
3.2.1	Test.....	8
3.2.2	Analysis.....	9
3.2.3	Inspection.....	9
3.3	Tailoring.....	9
3.4	Test Conditions.....	9
3.5	Measuring Equipment.....	9
3.5.1	Equipment Type.....	9
3.5.2	Equipment Accuracy.....	11
3.6	Operation of an ASI Under Test.....	11
3.7	Test Data.....	11
4.	DETAILED REQUIREMENTS.....	11
4.1	Introduction.....	11
4.2	High Bandwidth (HBW).....	12
4.2.1	General Requirement.....	12
4.2.2	Special Considerations.....	13
4.3	MIL-STD-1553 (MUX) Data.....	13
4.3.1	General Requirements.....	13
4.3.2	Special Considerations.....	15
4.4	Low Bandwidth (LBW).....	15
4.4.1	General Requirement.....	15
4.4.2	Special Considerations.....	15
4.5	Release (REL) Consent.....	16
4.5.1	General Requirement.....	16
4.5.2	Special Considerations.....	16
4.6	Interlock (INL).....	17
4.6.1	General Requirement.....	17
4.6.2	Special Considerations.....	17
4.7	Address (ADR).....	17
4.7.1	General Requirements.....	17
4.7.2	Special Considerations.....	18
4.8	Structure Ground (GND).....	18
4.8.1	General Requirement.....	18
4.8.2	Special Considerations.....	19
4.9	28 VDCP.....	19
4.9.1	General Requirement.....	19
4.9.2	Special Considerations.....	20
4.10	115 V/200 VACP.....	21
4.10.1	General Requirement.....	21
4.10.2	Special Considerations.....	22

4.11	270 VDCP	22
4.11.1	General Requirement	22
4.11.2	Special Considerations	23
4.12	Fiber Optics	24
4.12.1	General Requirement	24
4.12.2	Special Considerations	24
4.13	Initialization Procedures	24
4.13.1	General Requirement	24
4.13.2	Special Considerations	25
4.14	Connector Intermateability	25
4.14.1	General Requirement	25
4.14.2	Special Considerations	26
4.15	Umbilical Cables	26
4.15.1	General Requirement	26
4.15.2	Special Considerations	27
4.16	Fiber Channel Interface (FCI)	28
4.16.1	General Requirements	28
4.16.2	Special Considerations	28
5.	NOTES	28
5.1	Guidelines for Verification Plan Development	28
5.1.1	Introduction	28
5.2	Test Sequence	29
5.3	Revision Indicator	29
APPENDIX A	VERIFICATION METHODS	30
TABLE 1	HIGH BANDWIDTH VERIFICATION MATRIX	12
TABLE 2	MIL-STD-1553 DATA BUS INTERFACE VERIFICATION TEST COMPLIANCE MATRIX	14
TABLE 3	LOW BANDWIDTH VERIFICATION MATRIX	15
TABLE 4	RELEASE CONSENT VERIFICATION MATRIX	16
TABLE 5	INTERLOCK VERIFICATION MATRIX	17
TABLE 6	ADDRESS VERIFICATION MATRIX	18
TABLE 7	STRUCTURE GROUND VERIFICATION MATRIX	19
TABLE 8	28 VDC POWER VERIFICATION MATRIX	20
TABLE 9	115 V/200 VAC POWER VERIFICATION MATRIX	21
TABLE 10	270 VDC POWER VERIFICATION MATRIX	23
TABLE 11	FIBER OPTIC VERIFICATION MATRIX	24
TABLE 12	INITIALIZATION VERIFICATION MATRIX	25
TABLE 13	CONNECTOR INTERMATEABILITY VERIFICATION MATRIX	26
TABLE 14	UMBILICAL VERIFICATION MATRIX	27
TABLE 15	FIBER CHANNEL INTERFACE VERIFICATION TEST COMPLIANCE MATRIX	28

1. SCOPE

This document establishes techniques for validating that an Aircraft Station Interface (ASI) complies with the interface requirements delineated in MIL-STD-1760 Revision E.

1.1 Purpose

The purpose of this document is to provide methods for validating that an aircraft's store electrical interface complies with the aircraft station interface (ASI) requirements of MIL-STD-1760. This document provides a modular, independent set of methods for each of the requirements in MIL-STD-1760 that applies to aircraft requirements. For verification of aircraft designed to MIL-STD-1760A, AS4764 applies. For verification of aircraft designed to MIL-STD-1760B, AS47641 applies. For verification of aircraft designed to MIL-STD-1760C, AS47642A applies.

1.2 Application

The methods herein apply to initial verification of an aircraft design to the requirements of MIL-STD-1760 and are expected to be conducted as part of aircraft design verification (as opposed to qualification test, quality conformance test, flight line test, etc.). The methods contained in this document are sufficient to cover the Class I interface. Aircraft with Class II ASIs will use the appropriate subset of these Class I methods.

1.3 Tailoring

The methods contained herein are general methods for conducting ASI verification and, as such, do not provide detailed procedures for these methods. It is intended that detailed procedures for verification of a specific ASI will be covered by tailored test plans and procedures prepared specifically for that aircraft. These tailored test procedures would, for example, address those peculiar commands required to step through sufficient operations and states to demonstrate compliance with the particular aircraft/store electrical interconnection system (AEIS) requirement under test.

1.4 Limitations

The methods contained herein are based on MIL-STD-1760E. In addition, this document addresses testing compliance of an aircraft to MIL-STD-1760 based on the assumption that all tests are conducted at the aircraft's ASI connector and measurements of performance occur only at this ASI.

1.5 Identification System

The test methods contained in this document are designated by an alphanumeric identification scheme. Each method is identified by a three alphabetical character combination followed by a three-digit number. The meaning of the first three individual letters is:

- a. HBW: High Bandwidth Interface
- b. MUX: Digital Multiplex Data Interface
- c. LBW: Low Bandwidth Interface
- d. REL: Release Consent Interface
- e. INL: Interlock Interface
- f. ADR: Address Interface
- g. GND: Structure Ground
- h. 28 V: 28 VDC Power Interface
- i. ACP: 115 V/200 VAC Power Interface

- j. HVP: 270 VDC Power Interface
- k. FOC: Fiber Optic Channel
- l. INT: Initialization
- m. CON: ASI Connector
- n. UMB: Umbilical Cable
- o. FCI: Fiber Channel Interface

The three numbers following the letter code is a sequentially assigned number such that numbers 101 through 199 are for ASI requirements and 201 through 299 are reserved for mission store interface (MSI) requirements. When applicable, the letter following this three-digit number is the test method revision letter. For example, HBW101 represents the original version of the first test requirement (TR) for the ASI HBW interface while HBW101A represents the first revision of that requirement.

2. REFERENCES

2.1 Applicable Documents

The following publications form a part of this document to the extent specified herein. The latest issue of SAE publications shall apply. The applicable issue of other publications shall be the issue in effect on the date of the purchase order. In the event of conflict between the text of this document and references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

ISO 10012:2003 Measurement Management Systems – Req. for measurement process and measuring equipment

2.1.1 SAE Publications

Available from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096-0001, Tel: 877-606-7323 (inside USA and Canada) or +1 724-776-4970 (outside USA), www.sae.org.

AS4113 Verification Test Plan for the Digital Time Division Command/Response Multiplex Data Bus, Bus Controllers

2.1.2 U.S. Government Publications

Copies of these documents are available online at <http://quicksearch.dla.mil>.

MIL-C-38999 Connectors Electrical, Circular, Miniature, High Density, Quick Disconnect

MIL-STD-704 Electric Power, Aircraft, Characteristics and Utilization of MIL-STD-1498

MIL-STD-1553 Digital Time Division Command/Response Multiplex Data Bus

MIL-STD-1560 Insert Arrangements for MIL-C-38999 and MIL-C-27599 Electrical Circular Connectors

MIL-STD-1760E Aircraft/Store Electrical Interconnection System

2.1.3 NATO Publications

Available from the Document Automation and Production Service (DAPS), Building 4/D, 700 Robbins Avenue, Philadelphia, PA 19111-5094, Tel: 215-697-6257, <http://assist.daps.dla.mil/quicksearch/>.

STANAG 3350 AVS Analogue Video Standard for Aircraft Applications

2.2 Abbreviations and Acronyms

AC	Alternating Current
ACP	Alternating Current Power
ADR	Address
AEIS	Aircraft/Store Electrical Interconnection System
AS	Aerospace Standard
ASD	Avionics Systems Division
ASI	Aircraft Station Interface
AUX	Auxiliary
BC	Bus Controller
COM	Communication
CON	Connector
CSSI	Carriage Store Station Interface
dB	Decibel
dBm	Decibels above 1 mW
DC	Direct Current
DCP	Direct Current Power
DoDISS	Department of Defense Index of Specifications
EIA	Electronic Industries Association
FOC	Fiber Optic Channel
GHz	Gigahertz
GND	Ground
HB	High Bandwidth
HBW	High Bandwidth
HVP	High Voltage Power
Hz	Hertz
ICD	Interface Control Document
INL	Interlock
INT	Initialization

kHz	Kilohertz
LB	Low Bandwidth
LBW	Low Bandwidth
mA	Milliamp
MHz	Megahertz
MIL	Military
ms	Millisecond
MSG	Message
MSI	Mission Store Interface
MUX	Multiplex
N/A	Not Applicable
P-P	Peak-to-Peak
REL	Release
RNASP	Routing Network Aircraft System Port
RT	Remote Terminal
RMS	Root Mean Squared
STANAG	Standardization Agreement
STD	Standard
TDP	Technical Data Package
TR	Test Requirement
TRMS	True Root Mean Squared
UUT	Unit Under Test
V	Volts
VSWR	Voltage Standing Wave Ratio

2.3 Definitions

2.3.1 AEIS TERMS

Terminology peculiar to the AEIS is defined in MIL-STD-1760.

2.3.2 UNIT UNDER TEST (UUT)

The UUT is defined as the “production configuration aircraft” undergoing verification tests. The test point for all electrical tests is the ASI.

2.3.3 VERIFICATION

Verification is defined as the process whereby the final design of an AEIS is evaluated to determine its compliance with the requirements imposed by MIL-STD-1760. This compliance evaluation is accomplished using a combination of techniques including tests, analysis, and inspections. This verification is conducted to determine that the design complies with MIL-STD-1760 under nominal ambient conditions. While this verification may be part of an aircraft's qualification test (if specified in the aircraft's system specification), it is not necessarily intended to be conducted under all aircraft environmental and operational conditions and, as such, does not specifically “qualify” the aircraft to its system specification/interface control document (ICD) requirements.

The addition of a new column, titled “Shall Statement”, in each of the fourteen (14) Verification Tables, clearly identifies the requirement to be validated. The numbers in the column are directly linked to the corresponding “shall” statement in the order that it appears in the MIL-STD-1760 paragraph. For example, In Table 6 Address Verification Matrix, MIL-STD-1760 paragraph 5.1.6, the first two (2) shall statements, as they appear on 1760, are validated using test method ADR101 while the third (3) shall statement is validated using test method ADR102. In this way, the requirement is easily identified, traceable to MIL-STD-1760 and therefore must be followed or adhered to (tested) to verify overall system compliance to MIL-STD-1760.

3. GENERAL REQUIREMENTS

3.1 Introduction

As part of an aircraft's qualification to its system specification requirements, the AEIS design shall be validated against the requirements of MIL-STD-1760. The specific verification effort for a given ASI will be defined in a test plan prepared for the AEIS. The methods defined in this document provide guidance for the preparation of the test plans by delineating the pertinent requirements in MIL-STD-1760 and verification methodology. For those requirements that can be validated by test or analysis, this document also provides test techniques. Section 4, herein, presents verification details associated with each requirement in MIL-STD-1760.

3.2 Verification Techniques

Verification of a design to the requirements of MIL-STD-1760 can be accomplished through the use of a number of techniques. A general listing of these techniques includes:

- a. Test
- b. Analysis
- c. Inspection

3.2.1 Test

Tests are those methodologies that measure characteristics or performance under specified conditions. Tests also include techniques that “demonstrate” operation of circuitry or system performance.

3.2.2 Analysis

Analyses are those methodologies that verify design compliance with the designated requirements of MIL-STD-1760 without performance of verification test or inspection. These methodologies will primarily be based on technical evaluation of aircraft design documentation such as drawings, parts lists, software listings, etc.

3.2.3 Inspection

Inspections are visual examinations and other nondestructive investigations of hardware and materials to determine compliance with the physical requirements of MIL-STD-1760.

3.3 Tailoring

The implementation of an AEIS could be unique for each type of aircraft. Therefore, the test techniques presented in this document are written in general terms to avoid addressing aircraft unique operating details that would be required if detailed test techniques were presented. As a result, the procedures for validating an ASI will need to be defined by a custom "Test Plan" tailored specifically for the AEIS. This custom test plan would address specific test setups, test equipment, and those operating procedures required to exercise the ASI under test. These are a set of minimal verification requirements that can be added to but not subtracted from as that would mean that the AEIS may not meet the requirements of the "Standard".

3.4 Test Conditions

Except as specified in the detailed AEIS test plan, verification tests are expected to be conducted under the following ambient conditions:

- a. Temperature: Room ambient
- b. Altitude: Normal ground
- c. Vibration: None
- d. Humidity: Room ambient up to 90% relative humidity (noncondensing)
- e. Power supply:
 - AC: 115 VAC RMS $\pm$ 3.0 VAC RMS, 400 Hz $\pm$ 7 Hz
 - DC: 27.5 VDC $\pm$ 2.0 VDC

3.5 Measuring Equipment

This section addresses the test equipment used in the test methods contained in this document.

3.5.1 Equipment Type

The detailed test plan prepared for a specific AEIS will identify the specific equipment (by manufacturer and part number or by characteristics) that is to be used in each of the tests. The following is a list of generic equipment types required for testing an ASI:

- a. HBW Interfaces:
 - 1. Sinusoid Signal Generator capable of 1.3 V P-P at 20 MHz with $\pm$ 2.0 V offset
 - 2. Function/Arbitrary Waveform Generator capable of 3.5 Vpp, 20 Hz to 20 MHz with a $\pm$ 2.0 VDC offset
 - 3. Network Analyzer 20 Hz to 200 MHz both 50 and 75 Ω capability
 - 4. Spectrum Analyzer with high persistence display 20 Hz to 200 MHz, 50 and 75 Ω capability

5. Oscilloscope with storage facility
 6. Power Meter capable of measuring -55 dBm
 7. Adapters Cables, Impedance Matching Attenuators and Test Loads of 50 and 75 Ω
- b. Digital MUX Data Interface:
1. MIL-STD-1553 data bus tester
 2. Impedance analyzer
 3. Oscilloscope with storage facility
 4. TRMS differential voltmeter
- c. Low Bandwidth Interface:
1. Audio Spectrum Analyzer covering a frequency range from 150 Hz to 50 kHz with variable voltage output up to 12 V P-P with selectable output and input impedances.
 2. Test loads of 30, 50, 60, 75, and 600 Ω .
 3. Ohmmeter (continuity test).
 4. Digital voltmeters with a signal measurement bandwidth of greater than DC to 10 kHz.
 5. Second order Butterworth low pass filter (12 dB/octave roll-off) with a cut-off frequency of 8 kHz.
 6. Oscilloscope with storage facility.
- d. Discrete Interfaces (REL Consent, INL, ADR, and Structure GND):
1. Digital Volt Ammeter
 2. Oscilloscope with storage facility
 3. DC Power supply
 4. AC Power Supply
 5. Resistor Decade Box
- e. 28 VDCP Interface:
1. Digital Volt-Ammeter
 2. Oscilloscope with storage facility
 3. DC Power supply
- f. 115 V/200 VACP Interface:
1. Digital Volt-Ammeter
 2. Oscilloscope with storage facility

- 3. ACP (400 Hz) supply
- 4. Power factor meter
- g. 270 VDCP Interface:
 - 1. N/A
- h. Fiber Optic Interface:
 - 1. N/A
- i. Initialization, Connector Intermateability, Umbilical Cable Interface:
 - 1. None Required

3.5.2 Equipment Accuracy

The accuracy of instruments and test equipment used to control or monitor the test parameters shall be verified and shall satisfy the requirements of ISO-10012:2003 to the satisfaction of the procuring activity. All instruments and test equipment used in conducting the tests specified herein shall:

- a. Conform to laboratory standards whose calibration is traceable to the prime standards at the National Bureau of Standards.
- b. Have an accuracy of at least $\frac{1}{4}$ tolerance on the requirement to be measured. For example, if a variable has a tolerance of $\pm 10\%$, the test equipment shall have a measurement tolerance of $\pm 2.5\%$ or better. In the event of conflict between this accuracy and requirement for accuracy in any one of the test methods of this document, the latter should govern.
- c. Measurements made to satisfy open-ended maximum or minimum requirements shall be accurate within 5% of the requirements to be satisfied.

3.6 Operation of an ASI Under Test

The detailed test plan shall include those AEIS peculiar operational requirements necessary to sequence the ASI through the applicable states and modes. These peculiar requirements include such items as: timelines, commands to a store, status and responses from a store, and high and low bandwidth signal sources or loads. Actual or simulated signal inputs (and loads) required to activate, utilize, or operate all AEIS functions may be used during testing.

3.7 Test Data

Test data shall include complete identification of all test equipment and accessories. The data shall include the actual test setup, test sequence used, and ambient conditions. The test record shall contain a signature and date for certification of the test data by the test engineer.

4. DETAILED REQUIREMENTS

4.1 Introduction

Detailed verification methods are given in Appendix A of this document. The paragraphs below present information relative to each of the ASIs.

4.2 High Bandwidth (HBW)

4.2.1 General Requirement

The High Bandwidth (HBW) interfaces of the ASI are to be validated against the requirements of MIL-STD-1760 through a combination of test, analysis, and inspection methods. The HBW verification matrix is presented in Table 1.

Table 1 - High bandwidth verification matrix

MIL-STD-1760 Paragraph	Title	Shall Statement	Verification Technique 1	Verification Technique 2	Verification Technique 3	Method Reference
4.3	Primary Interface Signal Set	1 2 3	- X X	X X X	- X -	HBW101 HBW107-HBW121 HBW102
4.3.1	High Bandwidth Interfaces	1 2 3 4, 6 5	X X - X -	X X - X X	- - - - X	HBW101 HBW103, HBW109, N/A HBW107-HBW121 HBW101
4.3.1.1	Type A Signal Requirements	1, 2	X	-	-	HBW103
4.3.1.1a		1, 2, 3	X	-	-	HBW104
4.3.1.1b		1	X	-	-	HBW105
4.3.1.1c		1	X	-	-	HBW105
4.3.1.2	Type B Signal Requirements	1	-	-	-	N/A
4.3.1.3	Signal Assignment	1	-	X	-	HBW106
4.3.1.3a		1	-	X	-	HBW106
4.3.1.3b		1	-	X	-	HBW106
4.3.1.3c		1, 2	-	X	-	HBW106
5.1	Aircraft Requirements	1	-	X	-	HBW107-HBW121
5.1.1	Aircraft HB Interfaces	1, 2 3	X	X X	- -	HBW107 HBW109-HBW114
5.1.1.1	Minimum Transfer Capacity	1	X	X	-	HBW108
5.1.1.2.1	Type A Return Loss	1, 2	X	-	-	HBW109
5.1.1.2.2	Type A Transient Response	1, 2	X	-	-	HBW110
Figure 5b		1-6	X	-	-	HBW110
Figure 6b		1-5	X	-	-	HBW110
5.1.1.2.3	Type A Insertion Gain	1	X	-	-	HBW111
5.1.1.2.4	Type A Representative Pulse Delay	1, 2, 3	X	X	-	HBW112
5.1.1.2.5	Type A Equalization	1, 2, 3	X	-	-	HBW113
5.1.1.2.6	Type A Dynamic Range	1	X	-	-	HBW114
5.1.1.2.7	Type A Signal Path DC Offset	1	X	-	-	HBW115
5.1.1.2.8	Type A Noise Requirements	1	X	-	-	HBW116-HBW121
5.1.1.2.8.1	Type A Random Noise	1	X	-	-	HBW116
5.1.1.2.8.2	Type A Periodic Noise	1, 2, 3	X	-	-	HBW117
5.1.1.2.8.3	Type A Impulse Noise	1	X	-	-	HBW118
5.1.1.2.8.4	Type A Stimulated Noise	1	X	-	-	HBW119
5.1.1.2.8.5	Type A Common Mode Noise	1	X	-	-	HBW120
5.1.1.4	Ground Reference	1, 2, 3	X	-	-	HBW121
NOTE: Verification Techniques: 1. Test 2. Analysis 3. Inspection						

4.2.2 Special Considerations

The following special considerations apply to the three different verification techniques.

4.2.2.1 Test Techniques

Test of the aircraft's compliance to the HBW interface requirements concerns the effect of the ASI mating connector on the test results. Some of the critical electrical characteristics (such as Return Loss) of the interface can be significantly affected by the ASI connector performance. Likewise, the test results can be significantly affected by calibration methods associated with the test setup. An example case is measuring the Return Loss of the aircraft at the ASI. Typical methods for calibrating a network analyzer create an "opportunity" to cancel the effects of the ASI mating connector on the Return Loss measurement by considering the ASI mating connector as part of the test cable.

MIL-STD-1760 paragraphs 4.3.1 and 4.3.1.2 contain "Shall" statements for the Type B signal. However, there is no applicable test method for this requirement as Type B signals have not yet been adequately defined in the standard.

4.2.2.2 Analysis Techniques

The analysis effort associated with the HB interface is essentially limited to determining compliance by analysis of the aircraft's ICD or system specification, as applicable. In some instances analysis of specific test results is also required.

4.2.2.3 Inspection Techniques

The inspection effort associated with the HB interface is essentially limited to confirming that the aircraft HB interfaces include a signal connection and signal return (shield) connection. This compliance can be determined by analysis of the aircraft's ICD or system specification, as applicable.

4.2.2.4 Revisions and Notices

None.

4.3 MIL-STD-1553 (MUX) Data

4.3.1 General Requirements

The MIL-STD-1553 data interface of the ASI is to be validated against the requirements of MIL-STD-1760 through a combination of test, analysis, and inspection methods. The digital MUX data verification matrix is presented in Table 2.

Table 2 - MIL-STD-1553 data bus interface verification test compliance matrix

MIL-STD-1760 Paragraph	Title	Shall Statement	Verification Technique 1	Verification Technique 2	Verification Technique 3	Method Reference
4.3	Primary Interface Signal Set	1-3	X	X	X	MUX101-MUX119
4.3.2.1	MIL-STD-1553 Data Bus Interface	1, 2	-	-	X	MUX101-MUX119
5.1.2	Aircraft MIL-STD-1553 Data Bus Interface	1, 2			X	MUX101-MUX119
5.1.2.1a	Functional Characteristics	1, 2	-	X	-	MUX102
5.1.2.1b		1, 2		X		MUX103
5.1.2.1c		1		X		MUX104
5.1.2.1d		1		X		MUX102
5.1.2.1e		1		X		MUX104, MUX109-MUX119
C.4.2.2.4	Nuclear Weapon Control	1, 2, 3	-	X	-	MUX104
C.4.2.2.5	Nuclear Weapon Monitor	1, 2, 3		X		MUX104
5.1.2.2	Electrical Characteristics	1	X			MUX105-MUX108
5.1.2.2.1	Output Characteristics	1	X	-	-	MUX105
		3	X			MUX106
5.1.2.2.2	Input Characteristics	1	X		-	MUX107
5.1.2.2.3	Shield Grounding	1	X	-	-	MUX108
C.4.1	Logical Interface (Communication Rules)	1, 2, 3	-	X	-	MUX109
C.4.1.1.3.1.5	Logical Interface (Transmit Vector Word)	1, 2, 3	-	X	-	MUX11
C.4.1.1.3.1.6	Logical Interface (Synchronize with Data Word)	1, 2	-	X	-	MUX111
C.4.1.1.3.2	Logical Interface (Prohibited Mode Commands)	1	-	X	-	MUX112
C.4.1.2.3	Logical Interface (Subsystem Flag BIT)	1, 2, 3	-	X	-	MUX113
C.4.1.5.2 ?	Logical Interface (Checksum Requirement and Algorithm)	1	-	X	-	MUX114
C.4.1.5.3	Logical Interface (Execution Time)	1	-	X	-	MUX115
C.4.1.5.5	Logical Interface (Request Servicing)	1-4	-	X	-	MUX116
C.4.2.1	Logical Interface (Base Message Data Format)	1-3	-	X	-	MUX117
C.4.2.1.1		1, 2		X		
C.4.2.1.2				X		
C.4.2.2.1	Logical Interface (Store Control)	1	-	X	-	MUX118
C.4.2.2.2	Logical Interface (Store Monitor)	1	-	X	-	MUX119
NOTE: Verification Techniques: 1. Test 2. Analysis 3. Inspection						

4.3.2 Special Considerations

The following special considerations apply to the three different verification techniques.

4.3.2.1 Test Techniques

Test of the aircraft's compliance to the digital MUX data interface requirements concerns the effect of the mating test cable (between the test equipment and the aircraft) on the test results. Some of the critical electrical characteristic (such as input impedance) measurements can be significantly affected by the test cable characteristics. The test cable should use quality components and be as short in length as practical to minimize test cable effects on the test results.

4.4 Low Bandwidth (LBW)

4.4.1 General Requirement

The low bandwidth (LBW) interface of the ASI is to be validated against the requirements of MIL-STD-1760 through a combination of test, analysis, and inspection methods. The LBW verification matrix is presented in Table 3.

Table 3 - Low bandwidth verification matrix

MIL-STD-1760 Paragraph	Title	Shall Statement	Verification Technique 1	Verification Technique 2	Verification Technique 3	Method Reference
4.3	Primary Interface Signal Set	1-3	X	X	X	LBW101-LBW111
4.3.3	Low bandwidth interface	1, 2, 3, 4	- X	X X -	- - -	LBW101 LBW102 LBW104
4.3.3.1	LB signal requirements	1, 2, 3, 4	X X	- -	- -	LBW103 LBW106
4.3.3.2	Signal assignment	1, 2	- -	X -	- X	LBW102 LBW112
5.1.3	Aircraft LB interface	1, 2	-	X	-	LBW102
5.1.3.1	Minimum transfer capacity	1, 2	-	X	-	LBW102
5.1.3.2	Input/output impedance	1, 2	X	-	-	LBW104
5.1.3.3	Insertion gain	1	X	-	-	LBW107
5.1.3.4	Equalization requirements	1, 2	X	-	-	LBW107
5.1.3.5	Signal path dc offset	1	X	-	-	LBW108
5.1.3.6	Noise	-	N/A	N/A	N/A	-
5.1.3.6.1	Periodic random noise	1, 2, 3	X	X	-	LBW109
5.1.3.6.2	Impulse noise	1, 2	X	X	-	LBW110
5.1.3.6.3	Stimulated noise	1	X	X	-	LBW111
5.1.3.6.4	Common mode noise	1, 2	X	-	-	LBW108
5.1.3.7	Ground reference	1, 2, 3	- X	X -	- -	LBW101 LBW105
NOTE: Verification Techniques: 1. Test 2. Analysis 3. Inspection						

4.4.2 Special Considerations

The following special considerations apply to the three different verification techniques.

4.4.2.1 Test Techniques

Test of the aircraft's compliance to the LBW interface requirements concerns signal level, impedance, signal quality, and frequency range.

4.4.2.2 Analysis Techniques

The analysis effort associated with the LB interface is essentially limited to determining compliance by analysis of the aircraft's ICD or system specification, as applicable. In some instances analysis of specific test results is also required.

4.4.2.3 Inspection Techniques

The inspection effort associated with the LB interface is essentially limited to confirming that if the aircraft uses the interface for only those applications identified in the standard; i.e., tones or voice grade audio. This compliance can be determined by analysis of the aircraft's ICD or system specification, as applicable.

4.5 Release (REL) Consent

4.5.1 General Requirement

The Release Consent (REL) interface of the ASI is to be validated against the requirements of MIL-STD-1760 through a combination of test, analysis, and inspection methods. The Release Consent verification matrix is presented in Table 4.

Table 4 - Release consent verification matrix

MIL-STD-1760 Paragraph	Title	Shall Statement	Verification Technique 1	Verification Technique 2	Verification Technique 3	Method Reference
4.3	Primary Interface Signal Set	1, 2, 3	X	X	X	REL101-REL107
4.3.4	Release Consent Interface	1, 2	-	X	-	REL101
5.1.4	Aircraft Release Consent Interface	1, 2, 3 4, 5	- X	X X	- -	REL101 REL102
5.1.4.1 5.1.4a 5.1.4b	Voltage Level	1 2	X X	- -	- -	REL103 REL103
5.1.4.2	Current Level	1, 2	X	-	-	REL103
5.1.4.3	Stabilization Time	1	X	-	-	REL104
5.1.4.4	Enable Lead Time	1	-	X	-	REL105
5.1.4.5	Inhibit Delay	1	-	X	-	REL106
5.1.4.6	Ground Reference	1	-	X	-	REL107
5.1.4.7	Duration of Application	1	-	X	-	REL108
NOTE: Verification Techniques: 1. Test 2. Analysis 3. Inspection						

4.5.2 Special Considerations

The following special considerations apply to the three different verification techniques.

4.5.2.1 Test Techniques

Test of the aircraft's compliance to the Release Consent interface requirements concerns the electrical isolation to all other ASIs.

4.5.2.2 Analysis Techniques

The analysis effort associated with the Release Consent interface is essentially limited to confirming that the aircraft uses the interface for only those applications identified in the standard. This compliance can be determined by analysis of the aircraft's ICD or system specification, as applicable.

4.5.2.3 Inspection Techniques

The Release Consent interface has no inspection requirements.

4.5.2.4 Revisions and Notices

None.

4.6 Interlock (INL)

4.6.1 General Requirement

The Interlock (INL) interface of the ASI and Auxiliary ASI are to be validated against the requirements of MIL-STD-1760 through a combination of test, analysis, and inspection methods. The INL verification matrix is presented in Table 5.

Table 5 - Interlock verification matrix

MIL-STD-1760 Paragraph	Title	Shall Statement	Verification Technique 1	Verification Technique 2	Verification Technique 3	Method Reference
4.3	Primary Interface Signal Set	1, 2, 3	X	X		INL101-INL104
4.3.5	Primary Interlock Interface	1, 3		X		INL101
4.4	Auxiliary Power Interface Signal Set	1, 2		X		INL101
4.4.2	Auxiliary Interlock Interface	1, 3		X		INL101
5.1.5	Aircraft Interlock Interface	1		X		INL101
5.1.5a	Open Circuit Voltage	2	X			INL102
5.1.5b	Excitation Current	2	X			INL103
5.1.5c	Impedance Detection Threshold	1, 2	X			INL104
NOTE: Verification Techniques: 1. Test 2. Analysis 3. Inspection						

4.6.2 Special Considerations

The following special considerations apply to the three different verification techniques.

4.6.2.1 Test Techniques

Test of the aircraft's compliance to the Interlock interface requirements concern measurements required to evaluate impedances at specific voltage, current, and frequency levels.

4.6.2.2 Analysis Techniques

The analysis effort associated with the Interlock interface is essentially limited to confirming that the aircraft uses the interface for the application identified in the standard. This compliance can be determined by analysis of the aircraft's ICD or system specification, as applicable.

4.6.2.3 Inspection Techniques

The Interlock interface has no inspection requirements.

4.6.2.4 Revisions and Notices

MIL-STD-704 contains several revision and notices that may impact the verification criteria.

4.7 Address (ADR)

4.7.1 General Requirements

The address (ADR) interface of the ASI is to be validated against the requirements of MIL-STD-1760 through a combination of test, analysis, and inspection methods. The ADR verification matrix is presented in Table 6.

Table 6 - Address verification matrix

MIL-STD-1760 Paragraph		Shall Statement	Verification Technique 1	Verification Technique 2	Verification Technique 3	Method Reference
4.3	Primary Interface Signal Set	1, 2, 3	X	X	-	ADR101-DR109
4.3.6	Address Interface	1, 2	-	X	-	ADR101
5.1.6	Aircraft Address Interface	1, 2 3	- -	X X	- -	ADR101 ADR102
5.1.6.1	Address Assignment	2	-	X	-	ADR103
5.1.6.1a		3	-	X	-	ADR104
5.1.6.1b		1, 4	X	-	-	ADR105
5.1.6.2, 5.1.6.2a, 5.1.6.2b	Address Signal	1	X	-	-	ADR106
5.1.6.3, 5.1.6.3a, 5.1.6.3b	Logic Thresholds	1-4	X	-	-	ADR107
5.1.6.4	Response Characteristics	1, 2	X	-	-	ADR108
5.1.6.5	Address Isolation	1, 2	X	-	-	ADR109
NOTE: Verification Techniques: 1. Test 2. Analysis 3. Inspection						

4.7.2 Special Considerations

The following special considerations apply to the three different verification techniques.

4.7.2.1 Test Techniques

Test of the ASIs' compliance to the ADR interface requirements concerns the ability to determine if a unique address has been assigned to each ASI and tests for address stability, response times, thresholds, response characteristics, and isolation.

4.7.2.2 Analysis Techniques

The analysis effort associated with the ADR interface is essentially limited to confirming that the ASI uses the interface for only those applications identified in the standard. This compliance can be determined by analysis of the aircraft's ICD or system specification, as applicable.

4.7.2.3 Inspection Techniques

The ADR interface has no inspection requirements.

4.7.2.4 Revisions and Notices

None.

4.8 Structure Ground (GND)

4.8.1 General Requirement

The Structure Ground interface of the ASI is to be validated against the requirements of MIL-STD-1760 through a combination of test, analysis, and inspection methods. The Structure Ground verification matrix is presented in Table 7.

Table 7 - Structure ground verification matrix

MIL-STD-1760 Paragraph	Title	Shall Statement	Verification Technique 1	Verification Technique 2	Verification Technique 3	Method Reference
4.3	Primary Interface Signal Set	1-3	X	X		GND101
4.3.7	Primary Structure Ground	1-3	-	X	-	GND101
4.4.3	Auxiliary Structure Ground	1-3	-	X	-	GND101
5.1.7	Aircraft Structure Ground	1, 2	X	X	-	GND101
NOTE: Verification Techniques: 1. Test 2. Analysis 3. Inspection						

4.8.2 Special Considerations

The following special considerations apply to the three different verification techniques.

4.8.2.1 Test Techniques

The measurements required for the Structure Ground interfaces are current and voltage measurements between the Structure Ground interface contact and the aircraft conductive structure.

4.8.2.2 Analysis Techniques

The analysis aspects of the Structure Ground interface deal with fault analysis. The aircraft design should be evaluated to determine its ability to safely conduct the fault currents that could occur due to internal faults of power sources to vehicle structure. The path resistance shall be low enough that when conducting fault currents, the voltage developed is of safe magnitude. The analysis should confirm, by evaluation of the aircraft's ICD, fabrication drawings and other technical documentation, that the ASI is not relying on the existence of structure ground to complete a ground path for any interface power or signal function.

4.8.2.3 Inspection Techniques

The structure GND interface has no inspection requirements.

4.8.2.4 Revisions and Notices

None.

4.9 28 VDCP

4.9.1 General Requirement

The 28 VDCP interface of the ASI is to be validated against the requirements of MIL-STD-1760 through a combination of test, analysis, and inspection methods. The 28 VDCP verification matrix is presented in Table 8.

Table 8 - 28 VDC power verification matrix

MIL-STD-1760 Paragraph	Title	Shall Statement	Verification Technique 1	Verification Technique 2	Verification Technique 3	Method Reference
4.3	Primary Interface Signal Set	1-3	X	X		28V101-28V109
4.3.8	Primary Power	1 2, 4 3 5*	- - N/A N/A	X X N/A N/A	- - N/A N/A	28V102 28V101 (28 VDC only) - -
4.4.1	Auxiliary Power	1 2, 4 3 5*	- - N/A N/A	X X N/A N/A	- - N/A N/A	28V102 28V101 (28 VDC only) - -
5.1.8	Aircraft 28 VDC Power Interface	1-3	-	X	-	28V101
5.1.8.1	Independent Control	1	-	-	X	28V102
5.1.8.2	Voltage Level	1-4	X	X	-	28V103
5.1.8.3.1	Current Capacity Primary Signal Set	1, 2	X	X	-	28V104
5.1.8.3.2	Current Capacity Auxiliary Power Signal Set	1	X	X	-	28V105
5.1.8.3.3	Simultaneous Current	-	N/A	N/A	N/A	-
5.1.8.4	Overcurrent Protection	1	X	X	-	28V106
5.1.8.5	Off-State Leakage Current	1, 2	X	-	-	28V107
5.1.8.6	Stabilization Time	1	X	-	-	28V108
5.1.8.7	Ground Reference	1	-	-	X	28V101
5.1.8.8	Power Application	1, 2	-	X	-	28V109
NOTE: Verification Techniques: 1. Test 2. Analysis 3. Inspection * Shall for 'not to be used for discrete functions' is not considered to be relevant to ASIs.						

4.9.2 Special Considerations

The following special considerations apply to the three different verification techniques.

4.9.2.1 Test Techniques

Test of the ASI's compliance to the 28 VDCP interface requirements concerns the total 28 VDC continuous current provided simultaneously through both the primary and AUX interfaces at any Class IA or IIA ASI. This current need not exceed 30 A unless testing over current protection requirements.

4.9.2.2 Analysis Techniques

The analysis effort associated with the 28 VDCP interface is essentially limited to confirming that the ASI is "compatible" with MIL-STD-704. This compliance may be determined by analysis of the aircraft's ICD, fabrication drawings and other technical documentation that defines the design.

The abnormal operation voltage limits are to be validated by analysis only due to practical difficulties of arranging for the aircraft to work in an abnormal mode.

4.9.2.3 Inspection Techniques

The 28 VDCP interface has no inspection requirements.

4.9.2.4 Revisions and Notices

MIL-STD-704 contains several revisions, notices, and amendments that may impact the verification criteria.

NOTE: The requirement in Section 4 of MIL-STD-1760 that the power interface is not to be used for discrete functions is considered not relevant to ASIs and is therefore not addressed in this document.

The soft requirement for simultaneous current is validated by the independent control analysis and maximum current capability tests for the Primary and Auxiliary; i.e., combination need not exceed 30 A.

4.10 115 V/200 VACP

4.10.1 General Requirement

The 115 V/200 VACP interface of the ASI is to be validated against the requirements of MIL-STD-1760E through a combination of test, analysis, and inspection methods. The 115 V/200 VACP verification matrix is presented in Table 9.

Table 9 - 115 V/200 VAC power verification matrix

MIL-STD-1760 Paragraph	Title	Shall Statement	Verification Technique 1	Verification Technique 2	Verification Technique 3	Method Reference
4.3	Primary Interface Signal Set	1-3	X	X		ACP101-ACP112
4.3.8	Primary Power	1 2, 4 3 5*	- - N/A N/A	X X N/A N/A	- - N/A N/A	ACP102 ACP101 (115 VAC only) - -
4.4.1	Auxiliary Power	1 2, 4 3 5*	- - N/A N/A	X X N/A N/A	- - N/A N/A	ACP102 ACP101 (115 VAC only) - -
5.1.9	115 V/200 VAC Power Interface	1-3	-	X	-	ACP101
5.1.9.1	Independent Control and Deadfacing	1-3	-	X	-	ACP102
5.1.9.2	Voltage Level	1-3	X	X	-	ACP103
5.1.9.3.1	Current Capacity Primary Signal Set	1	X	X	-	ACP104
5.1.9.3.2	Current Capacity Auxiliary Power Signal Set	1	X	X	-	ACP105
5.1.9.3.3	Simultaneous Current	-	N/A	N/A	N/A	-
5.1.9.4	Overcurrent Protection	1	X	X	-	ACP106
5.1.9.5	Off-state Leakage Current	1, 2	X	-	-	ACP107
5.1.9.6	Stabilization Time	1	X	-	-	ACP108
5.1.9.7	Phase Rotation	1 1	X X	- -	- -	ACP109 ACP110
5.1.9.8	Load Power Factor	1	-	X	-	ACP111
5.1.9.9	Phase Power Unbalance	1	-	X	-	ACP112
5.1.9.10	Ground Reference	1	-	X	-	ACP101
5.1.9.11	Power Application	-	N/A	N/A	N/A	-

NOTE: Verification Techniques:

1. Test
2. Analysis
3. Inspection

* Shall for 'not to be used for discrete functions' is not considered to be relevant to ASIs.

4.10.2 Special Considerations

The following special considerations apply to the three different verification techniques.

4.10.2.1 Test Techniques

Test of the ASI's compliance to the 115 V/200 VACP interface requirements concerns the total 115 VAC continuous current provided simultaneously through both primary and AUX interfaces at any Class IA or IIA ASI. This current need not exceed 30 A per phase unless testing over current requirements.

4.10.2.2 Analysis Techniques

The analysis effort associated with the 115 V/200 VACP interface is essentially limited to confirming that the ASI is "compatible" with MIL-STD-704. This compliance can be determined by analysis of the aircraft's ICD, fabrication drawings, and other technical documentation that defines the ASI design.

The abnormal operation voltage limits are to be validated by analysis only due to practical difficulties of arranging for the aircraft to work in an abnormal mode.

4.10.2.3 Inspection Techniques

The 115 V/200 VACP interface has no inspection requirements.

4.10.2.4 Revisions and Notices

MIL-STD-704 contains several revisions, notices, and amendments that may impact the verification criteria.

NOTE: The requirement in Section 4 of MIL-STD-1760 that the power interface is not to be used for discrete functions is considered not relevant to ASIs and is therefore not addressed in this document.

The soft requirement for simultaneous current is validated by the independent control analysis and maximum current capability tests for the Primary and Auxiliary; i.e., combination need not exceed 30 A.

The Power Application requirement is considered to be applicable to stores and not addressed here.

4.11 270 VDCP

4.11.1 General Requirement

The 270 VDC high voltage power (HVP) interface of the ASI is to be validated against the requirements of MIL-STD-1760E through a combination of test, analysis, and inspection methods. The 270 VDCP verification matrix is presented in Table 10.

Table 10 - 270 VDC power verification matrix

MIL-STD-1760 Paragraph	Title	Shall Statement	Verification Technique 1	Verification Technique 2	Verification Technique 3	Method Reference
4.3	Primary Interface Signal Set	1, 2, 3	-	X	-	HVP101
4.3.8	Primary Power Interface	1, 3, 4, 5	-	X	-	HVP101
4.4	Auxiliary Power Interface Signal Set Interface	1, 2	-	X	-	HVP101
4.4.1	Auxiliary Power	1, 3, 4, 5	-	X	-	HVP101
5.1.10	Aircraft 270VDC Power Interface	1, 2	-	X	-	HVP101
5.1.10.1	Independent Control and Dead Facing	1, 2, 3	-	X	-	HVP102
5.1.10.2	Voltage Level	1, 2, 3	X	X	-	HVP103
5.1.10.3	Current Capacity:	-	-	-	-	-
5.1.10.3.1	Primary Signal Set	1	X	X	-	HVP104
5.1.10.3.2	Auxiliary Power Signal Set	1	X	X	-	HVP105
5.1.10.3.3	Simultaneous Current	-	-	-	-	-
5.1.10.4	Overcurrent Protection	1	X	X	-	HVP106
5.1.10.5	Off-state Leakage Current	1, 2	X	-	-	HVP107
5.1.10.6	Stabilization Time	1	X	-	-	HVP108
5.1.10.7	Ground Reference	1	-	X	-	HVP101
5.1.10.8	Power Application	-	-	-	-	-
NOTE: Verification Techniques: 1. Test 2. Analysis 3. Inspection						

4.11.2 Special Considerations

The following special considerations apply to the three different verification techniques.

4.11.2.1 Test Techniques

Test of the ASI's compliance to the 270 VDCP interface requirements concerns the total 270 VDC continuous current provided simultaneously through both the primary and AUX interfaces at any Class IA or IIA ASI. This current need not exceed 30 A unless testing over current requirements.

4.11.2.2 Analysis Techniques

The analysis effort associated with the 270 VDCP interface is essentially limited to confirming that the ASI is "compatible" with MIL-STD-704. This compliance may be determined by analysis of the aircraft's ICD, fabrication drawings and other technical documentation that defines the design.

The abnormal operation voltage limits are to be validated by analysis only due to practical difficulties of arranging for the aircraft to work in an abnormal mode.

4.11.2.3 Inspection Techniques

The 270 VDCP interface has no inspection requirements.

4.11.2.4 Revisions and Notices

MIL-STD-704 contains several revisions, notices, and amendments that may impact the verification criteria.

NOTE: The requirement in Section 4 of MIL-STD-1760 that the power interface is not to be used for discrete functions is considered not relevant to ASIs and is therefore not addressed in this document.

The soft requirement for simultaneous current is validated by the independent control analysis and maximum current capability tests for the Primary and Auxiliary; i.e., combination need not exceed 30 A.

4.12 Fiber Optics

4.12.1 General Requirement

The fiber optic (FOC) interface of the ASI is to be validated against the requirements of MIL-STD-1760 through a combination of test, analysis, and inspection methods. The FOC verification matrix is presented in Table 11.

Table 11 - Fiber optic verification matrix

MIL-STD-1760 Paragraph	Title	Shall Statement	Verification Technique 1	Verification Technique 2	Verification Technique 3	Method Reference
4.3	Primary Interface Signal Set	1, 2, 3		X	X	FOC101
4.3.9	Fiber Optics Interfaces	1		X	X	FOC101
5.1.11	Fiber Optic Interface	1, 2, 3	-	X	X	FOC101
NOTE: Verification Techniques: 1. Test 2. Analysis 3. Inspection						

4.12.2 Special Considerations

The following special considerations apply to the three different verification techniques.

4.12.2.1 Test Techniques

There are no FOC interface tests required for ASI verification since the FOC interface requirement is limited to reserving cavities in the connectors.

4.12.2.2 Analysis Techniques

The analysis effort associated with the FOC interface is limited to confirming, by inspection, that the ASI does not use the connector cavities that are reserved for FOC applications. This compliance can be determined by analysis of the aircraft's ICD, fabrication drawings, and other technical documentation that defines the aircraft design.

4.12.2.3 Inspection Techniques

The inspection requirement associated with the ASI's FOC interface deals with confirming that the ASI connector contains plugged contact cavities for the two reserved FOC channels.

4.13 Initialization Procedures

4.13.1 General Requirement

The power-up initialization performance of the ASI is to be validated against the requirements of MIL-STD-1760 through a combination of test, analysis, and inspection methods. The initialization verification matrix is presented in Table 12.

Table 12 - Initialization verification matrix

MIL-STD-1760 Paragraph	Title	Shall Statement	Verification Technique 1	Verification Technique 2	Verification Technique 3	Method Reference
4.3	Primary Interface	1-3	-	X	-	INT101-INT104
5.1.12	Signal Set Initialization	1	-	X	-	INT101
5.1.12.1	Pre-initialization Conditions	1	-	X	-	INT102
5.1.12.1a		1	-	X	-	
5.1.12.1b		1	-	X	-	
5.1.12.1c		1	-	X	-	
5.1.12.2	Power Application	1, 2	-	X	-	INT103
5.1.12.3	First Response	1, 2, 3	-	X	-	INT104
NOTE: Verification Techniques: 1. Test 2. Analysis 3. Inspection						

4.13.2 Special Considerations

The following special considerations apply to the three different verification techniques.

4.13.2.1 Test Techniques

Test of the ASI's compliance to the power-up initialization process concerns operational limitations that may exist with the aircraft. Conducting these tests will generally require several cycles of power turn-on and turn-off to evaluate the various test cases. The detailed test plan for the specific aircraft ASI under test should identify any power cycling limitations.

4.13.2.2 Analysis Techniques

A number of ASI initialization requirements in MIL-STD-1760 are defined as aspects associated with being compatible with various interface operational conditions. For example, paragraph 5.1.12.1, MIL-STD-1760E, states that Release Consent interface shall be in the inhibit state prior to store power-up. These compatibility requirements shall be validated by analysis.

This verification will be based on evaluation of associated aircraft technical documentation such as ICDs, drawings, software listings, etc.

4.13.2.3 Inspection Techniques

There are no inspection requirements associated with the power-up initialization process verification.

4.14 Connector Intermateability

4.14.1 General Requirement

Connector (CON) intermateability characteristics of the ASI are to be validated against the requirements of MIL-STD-1760 through a combination of test, analysis, and inspection methods. The CON intermateability verification matrix is presented in Table 13.

Table 13 - Connector intermateability verification matrix

MIL-STD-1760 Paragraph	Title	Shall Statement	Verification Technique 1	Verification Technique 2	Verification Technique 3	Method Reference
4.3	Primary Interface Signal Set	1-3		X	X	CON101, CON102
4.5	Interface connectors	1, 2	-	X	X	CON101
5.6.1a, 5.6.1b, 5.6.1f, 5.6.1g	Primary interface connectors	1-4, 13, 14	-	X	X	CON101
5.6.2a, 5.6.2b, 5.6.2c, 5.6.2d	Auxiliary power interface connector	1 - 4	-	X	X	CON101
5.6.3, 5.6.4	Connector receptacle, Plugged cavities	1	-	X	X	CON101
5.6.7.1a, 5.6.7.1b, 5.6.7.1c, 5.6.7.1d	ASI and CSSI	1	-	-	X	CON102
NOTE: Verification Techniques: 1. Test 2. Analysis 3. Inspection						

4.14.2 Special Considerations

The following special considerations apply to the three different verification techniques.

4.14.2.1 Test Techniques

There are no CON intermateability tests required for ASI verification.

4.14.2.2 Analysis Techniques

The analysis effort associated with CON intermateability is limited to confirming that the aircraft uses the correct connector type, insert, and contact assignments. This compliance can be determined by analysis of the aircraft's ICD, fabrication drawings, and other technical documentation that defines the ASI design.

4.14.2.3 Inspection Techniques

The inspection requirements associated with the ASI connector characteristics consist of visual verification of connector orientations.

4.14.2.4 Revisions and Notices

MIL-STD-1560, MIL-C-38999, and MIL-C-39029 contain several revisions, notices, and amendments that may impact the verification criteria.

4.15 Umbilical Cables

4.15.1 General Requirement

Umbilical (UMB) characteristics are to be validated against the requirements of MIL-STD-1760 through a combination of analysis, and inspection methods. The UMB cable verification matrix is presented in Table 14.

Table 14 - Umbilical verification matrix

MIL-STD-1760 Paragraph	Title	Shall Statement	Verification Technique 1	Verification Technique 2	Verification Technique 3	Method Reference
4.3	Primary Interface Signal Set	1-3	-	X	X	UMB101-UMB103
5.4	Umbilical Cable Requirements	1	-	-	X	UMB101
5.4.1	Primary Umbilical HB Interfaces	1	-	-	X	UMB102
		2	-	-	X	UMB103
5.4.2	Primary Umbilical Data Bus Interface	1	-	-	X	UMB102
		2	-	-	X	UMB103
5.4.3	Primary Umbilical LB Interface	1	-	-	X	UMB102
		2	-	-	X	UMB103
5.4.4	Primary Umbilical Release Consent Interface	1	-	-	X	UMB102
5.4.5	Umbilical Interlock Interface	1	-	-	X	UMB102
5.4.6	Primary Umbilical Address Interface	1	-	-	X	UMB102
5.4.7	Umbilical Structure Ground	1, 2	-	-	X	UMB102
5.4.8	Umbilical 28 VDC Power Interface	1, 2	-	-	X	UMB102
5.4.9	Umbilical 115 VAC Power Interface	1, 2	-	-	X	UMB102
5.4.10	Umbilical 270 VDC Power Interface	1	-	-	X	UMB101
5.4.11	Primary Umbilical Fiber Optic Interface	1	-	-	X	UMB101
5.4.12	Umbilical Gross Shield	1	-	-	X	UMB101
		2	-	-	X	UMB103
5.6.5	Umbilical Primary Interface Connectors	1-4	-	X	X	UMB101
5.6.5	Umbilical Auxiliary Interface Connectors	1-4	-	X	X	UMB101
5.6.7.3	Umbilical Cable	1, 2	-	-	X	UMB101
NOTE: Verification Techniques: 1. Test 2. Analysis 3. Inspection						

4.15.2 Special Considerations

The following special considerations apply to the different verification techniques.

4.15.2.1 Test Techniques

The analysis effort associated with umbilical cables is limited to confirming that the aircraft uses the correct connector type, insert, contact types, and cables types that meet the requirements, and that the umbilical production test documentation and reports confirm compliance with the isolation and bonding requirements across the environment the umbilical is expected to operate in. This compliance can be determined by analysis of the aircraft's ICD, fabrication drawings, and other technical documentation that defines the Umbilical design.

4.15.2.2 Analysis Techniques

The inspection requirements associated with the umbilical characteristics consist of visual verification of connector orientation, and if desired, identification of contact types.

4.15.2.3 Inspection Techniques

MIL-STD-1560, MIL-C-38999, and MIL-C-39029 contain several revisions, notices, and amendments that may impact the verification criteria.

4.16 Fiber Channel Interface (FCI)

4.16.1 General Requirements

The Fiber Channel interface of the ASI is to be validated against the requirements of MIL-STD-1760 through a combination of test, analysis, and inspection methods. The FCI verification matrix is presented in Table 15.

Table 15 - Fiber channel interface verification test compliance matrix

MIL-STD-1760 Paragraph	Title	Shall Statement	Verification Technique 1	Verification Technique 2	Verification Technique 3	Method Reference
4.3	Primary Interface Signal Set	1-3	X	X	X	FCI101
4.3.2.2	Fiber Channel Interface	1, 2	-	-	X	FCI101
5.1.13	Aircraft Fiber Channel Interface	1, 2, 3.4.5			X	FC101 & See AS6089, AS6260
D.4.1	Communication Rules	1, 2, 3	X	X	X	AS6089
D.4.2.1	Base Message Data Format	1	X	X	X	AS6089
D.4.2.2.1	Store Control	1	X	X	X	AS6089
D.4.2.2.2	Store Monitor	1	X	X	X	AS6089
D.4.2.2.3	Store Description	1	X	X	X	AS6089
D.4.2.2.4	Aircraft Description	1	X	X	X	AS6089
D.4.2.3	Mass Data Transfer Messages	1	X	X	X	AS6089
D.4.2.4	Protocol for Time Tagging	1, 2, 3	X	X	X	AS6089
D.4.2.4.1a	Time Tag Reference Time	1, 2, 3, 4, 5	X	X	X	AS6089
D.4.2.4.2a	Aircraft System Time at Reset	1, 2, 3, 4	X	X	X	AS6089
D.4.2.4.3a	Receive Time Tag	1, 2	X	X	X	AS6089
D.4.2.4.4a	Transmit Time Tag	1, 2	X	X	X	AS6089
NOTE: Verification Techniques: 1. Test 2. Analysis 3. Inspection						

4.16.2 Special Considerations

The following special considerations apply to the three different verification techniques.

4.16.2.1 Test, Analysis, and Inspection Techniques

Test, Analysis, and Inspection of the aircraft's compliance to the Fiber Channel interface are to be performed IAW the verification methods in AS6089 (for AS5653 Network Controller) and AS6260 (for AS5653 Physical Layer).

5. NOTES

5.1 Guidelines for Verification Plan Development

5.1.1 Introduction

A custom verification plan should be written specifically for each ASI to be validated. The development of the test plan requires that ASI data items be available. These data items should include, but not be limited to, an aircraft ICD, wiring diagram, system segment specification, and data document. With the necessary data items available, a review of the verification methods in Appendix A should be performed to identify the test, analysis, and inspection techniques necessary for verification. Once the required techniques have been identified, a specific verification plan can then be written for each test method.

5.2 Test Sequence

Careful consideration must be given to the test sequences for each ASI. All operational safety requirements of the aircraft must be identified. Additionally, all operational restrictions of the aircraft must be known. In general, analysis methods will be performed prior to electrical tests on the aircraft. Power limitations of some aircraft may preclude prolonged operation or repetitive cycling of operation power. The initial tests on the ASI should verify the physical interface. All unused pins should be checked, if not plugged, for proper impedance characteristics. The connector should be checked for intermateability, the structure GND interface should be checked, and INL continuity and isolation should be tested. MIL-STD-1553 control signals, such as, the ADR interface, INL, and REL consent tests should be performed. After these tests have been completed, ACP and DCP interfaces should be checked. The final sets of tests should check those portions of the LB and HB interface that have been implemented. Once the required testing has been completed, the aircraft should be returned to a known state and power should be removed.

5.3 Revision Indicator

A change bar (I) located in the left margin is for the convenience of the user in locating areas where technical revisions, not editorial changes, have been made to the previous issue of this document. An (R) symbol to the left of the document title indicates a complete revision of the document, including technical revisions. Change bars and (R) are not used in original publications, nor in documents that contain editorial changes only.

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APPENDIX A - VERIFICATION METHODS

METHOD: HBW101

PARAMETER: Primary Interface Signal Set, High Bandwidth Interfaces

MIL-STD-1760E PARAGRAPH: 4.3, 4.3.1

PURPOSE: This method verifies that the RNASP HB interfaces required in the primary interface signal set are present and that each HB interface has a signal connection and a signal return (shield) connection.

PARAMETER TYPE: ☒ ELECTRICAL ☐ PROTOCOL ☐ PHYSICAL
VERIFICATION TECHNIQUE: ☐ TEST ☒ ANALYSIS ☐ INSPECTION

VERIFICATION CRITERIA: The aircraft is considered to have passed if the required HB1 and HB3 signals are present and supported by the RNASP and if each HB interface has a signal connection and a signal return (shield) connection.

APPARATUS: N/A

VERIFICATION METHOD: Evaluate the aircraft's TDP to verify that the HB interfaces are supported per the primary interface signal set requirements and that each interface contains a signal connection and a signal return.

NOTES: N/A

METHOD: HBW102

PARAMETER: Primary Interface Signal Set

MIL-STD-1760E PARAGRAPH: 4.3

PURPOSE: This method verifies that an RNASP is not damaged by the removal of any termination from any HB interface.

PARAMETER TYPE:	☒ ELECTRICAL	☐ PROTOCOL	☐ PHYSICAL
VERIFICATION TECHNIQUE:	☒ TEST	☒ ANALYSIS	☐ INSPECTION

VERIFICATION CRITERIA: The aircraft is considered to have passed if all HB verification methods are passed after all RNASP inputs and outputs have been exercised with their required signal sets without input or output terminations.

APPARATUS: N/A

VERIFICATION METHOD:

To verify by analysis:

Analyze the RNASP TDP for the system to verify that no terminations are required to prevent damage to the input or output.

To verify by test:

Apply the appropriate logic to activate the HB path under test and remove the input and output terminations for the required RNASP path. If this is a bi-directional signal path, switch the direction and repeat the test. Repeat for all required RNASP paths.

Apply the appropriate signal to each required input to the RNASP, apply the appropriate logic to activate the HB path under test and then disconnect the output load from the path being tested. If this is a bi-directional signal path, switch the direction and repeat the test. Repeat for all required RNASP paths.

Apply the appropriate signal to each required input to the RNASP, apply the appropriate logic to activate the HB path under test and then disconnect the input termination from the path being tested. If this is a bi-directional path, switch the direction and repeat the test. Repeat for all required RNASP paths.

Verify the correct operation of each signal path after the completion of the test methods above.

NOTES: N/A

METHOD: HBW103

PARAMETER: Type A Signal Requirements

MIL-STD-1760E PARAGRAPH: 4.3.1.1a

PURPOSE: This method verifies the routing network meets the steady state and transient signal condition requirements.

PARAMETER TYPE: ☒ ELECTRICAL ☐ PROTOCOL ☐ PHYSICAL
VERIFICATION TECHNIQUE: ☒ TEST ☐ ANALYSIS ☐ INSPECTION

VERIFICATION CRITERIA: The aircraft is considered to have passed if the routing network can support:

- a. A 1.3 V P-P signal within a ± 1.55 VDC steady state component.
- b. The 1.3 V P-P signal returns to within 5% of its steady state limit in less than 250 ms following a transient change and stays within the range of ± 2.0 V.

APPARATUS:

- a. Function generator capable of producing a 1.3 V P-P, 20 Hz to 20 MHz sine wave and capable of supplying a DC offset of ± 900 mV.
- b. Oscilloscope
- c. Adapters cables (50 and 75 Ω) for connecting the test equipment to the ASI.
- d. 50 and 75 Ω BNC 'T' with 50 and 75 Ω loads

VERIFICATION METHOD:

- a. Input a sine wave in the frequency range of 20 Hz to 20 MHz, 1.3 V P-P within ± 1.55 V into the signal path input and verify on the oscilloscope, the signal integrity.
- b. Input a sine wave in the frequency range of 20 Hz to 20 MHz, 1.3 V P-P within ± 1.55 V and record the P-P output. Input a DC offset of +900 mV then change the offset to -900 mV, verify the output remains within ± 2.0 V and verify the output recovers to within 5% of the signals steady state P-P limit in less than 250 ms following the transient change of the DC offset component.
- c. Repeat test in b change the DC offset from -900 to +900 mV.

NOTES:

1. If multiple paths through the aircraft routing network are possible, then each path shall be validated.
2. HB1 is a 50 Ω signal path.
3. HB3 is a 75 Ω signal path.
4. All signal paths must be terminated with their correct characteristic impedance.

METHOD: HBW104

PARAMETER: Type A Signal Requirements

MIL-STD-1760E PARAGRAPH: 4.3.1.1b

PURPOSE: This method verifies the routing network meets the power spectral component requirement between 20 and 200 MHz of 14 dB/octave.

PARAMETER TYPE: ☒ ELECTRICAL ☐ PROTOCOL ☐ PHYSICAL
VERIFICATION TECHNIQUE: ☒ TEST ☐ ANALYSIS ☐ INSPECTION

VERIFICATION CRITERIA: The aircraft is considered to have passed if the output of any signal path is within the power spectral component limit line of 14 dB/octave between 20 to 200 MHz.

APPARATUS:

- a. Spectrum Analyzer
- b. Signal Generator (20 MHz at 1.33 V P-P)
- c. Adapters cables (50 and 75 Ω) for connecting the test equipment to the ASI.

VERIFICATION METHOD:

Connect the signal generator (20 MHz at 1.33 V P-P) to the ASI input connector and the input of the spectrum analyzer to the ASI output. Verify the power spectral component measurement at 20 MHz and then scan the spectrum analyzer to 200 MHz. Verify that between 20 and 200 MHz the power spectral component does not exceed 14 dB/octave.

NOTES:

1. If multiple paths through the aircraft routing network are possible, then each path shall be validated.
2. HB1 is a 50 Ω signal path.
3. HB3 is a 75 Ω signal path.
4. All signal paths must be terminated with their correct characteristic impedance.

METHOD: HBW105

PARAMETER: Type A Signal Requirements

MIL-STD-1760E PARAGRAPH: 4.3.1.1c

PURPOSE: This method verifies the routing network meets the slew rate requirements.

PARAMETER TYPE: ☒ ELECTRICAL ☐ PROTOCOL ☐ PHYSICAL
VERIFICATION TECHNIQUE: ☒ TEST ☐ ANALYSIS ☐ INSPECTION

VERIFICATION CRITERIA: The aircraft is considered to have passed if the routing network can support a minimum slew rate or 65 V/microsecond.

EQUIPMENT:

- a. Function generator capable of producing a 2 V P-P, 10 MHz square wave
- b. Oscilloscope
- c. Adapters cables (50 and 75 Ω) for connecting the test equipment to the ASI
- d. 50 and 75 Ω BNC 'T' with 50 and 75 Ω loads

VERIFICATION METHOD:

- a. Adjust the function generator output for a 10 MHz, 2 V P-P square wave.
- b. View the square wave on the oscilloscope and insure the rise time of the leading or trailing edge is 65 V/microsecond or greater.
- c. Apply the square wave into the signal path input.
- d. Connect the oscilloscope to the signal path output.
- e. Measure the voltage change versus time of the leading or trailing edge of the output square wave.
- f. Calculate the voltage change (slew rate) per microsecond to see if it meets the passing requirement of being equal to or greater than the minimum requirement of 65 V/microsecond.

NOTES:

- 1. If multiple paths through the aircraft routing network are possible, then each path shall be validated.
- 2. HB1 is a 50 Ω signal path.
- 3. HB3 is a 75 Ω signal path.
- 4. All signal paths must be terminated with their correct characteristic impedance.

METHOD: HBW106

PARAMETER: Signal Requirements

MIL-STD-1760E PARAGRAPH: 4.3.1.3, 4.3.1.3a, 4.3.1.3b, 4.3.1.3c

PURPOSE: This method verifies that the RNASP assigns the allowed signals to the proper HB signal paths.

PARAMETER TYPE: ☒ ELECTRICAL ☐ PROTOCOL ☐ PHYSICAL
VERIFICATION TECHNIQUE: ☐ TEST ☒ ANALYSIS ☐ INSPECTION

VERIFICATION CRITERIA: The aircraft is considered to have passed if the:

- a. RNASP only transfers signals which comply with type B signal characteristics on the HB1 interface.
- b. RNASP only transfers time correlation (synchronization, clocking and blanking) signals which comply with type A signal characteristics on HB1.
- c. RNASP only transfers monochrome raster composite video that complies with STANAG 3350 on HB3.

APPARATUS: N/A

VERIFICATION METHOD: Evaluate the aircraft's TDP to determine if the aircraft HB distribution network only transfers the allowed Type A and B signals on the specified HB interface.

- a. Signals which comply with type B signal characteristics shall only be transferred on HB1.
- b. Time correlation (synchronization, clocking, and blanking) signals which comply with type A signal characteristics shall only be transferred on HB1.
- c. Monochrome raster composite video shall only be transferred on HB3. Raster composite video shall comply with STANAG 3350.

NOTES: N/A

METHOD: HBW107

PARAMETER: Aircraft HB Interface

MIL-STD-1760E PARAGRAPH: 5.1.1

PURPOSE: This method verifies that the aircraft provides the HB signal routing network necessary to support bi-directional signal transfer at each ASI for transfer of both type A and type B signals.

PARAMETER TYPE: ☐ ELECTRICAL ☐ PROTOCOL ☒ PHYSICAL
VERIFICATION TECHNIQUE: ☐ TEST ☒ ANALYSIS ☐ INSPECTION

VERIFICATION CRITERIA: The aircraft is considered to have passed if the HB distribution network provides the necessary paths to support the transfer of a simplex HB signal between the RNASP and any ASI or between ASIs as applicable. The aircraft shall be capable of assigning, controlling, and routing/re-routing HB signals to their proper destinations.

APPARATUS: N/A

VERIFICATION METHOD: Evaluate the aircraft's TDP to determine if the aircraft HB distribution network provides the necessary paths to support bi-directional signal transfer from RNASP to any ASI and between ASIs where applicable.

NOTES: N/A

METHOD: HBW108

PARAMETER: Minimum Transfer Capacity

MIL-STD-1760E PARAGRAPH: 5.1.1.1

PURPOSE: This method verifies that the aircraft provides the minimum simultaneous transfer of HB signals through an ASI.

PARAMETER TYPE: ☐ ELECTRICAL ☐ PROTOCOL ☒ PHYSICAL
VERIFICATION TECHNIQUE: ☐ TEST ☒ ANALYSIS ☐ INSPECTION

VERIFICATION CRITERIA: The aircraft is considered to have passed if the HB distribution network provides the necessary capacity to support the transfer of a one type A signal or one type B signal on HB1, simultaneously with the transfer of a type A signal on HB3 through an ASI.

APPARATUS: N/A

VERIFICATION METHOD: Evaluate the aircraft's TDP to determine if the aircraft HB distribution network provides the necessary capacity to support the simultaneous signal transfer of one type A signal or one type B signal on HB1 with the transfer of a type A signal on HB3 through an ASI.

NOTES: N/A

METHOD: HBW109

PARAMETER: Type A Return Loss

MIL-STD-1760E PARAGRAPH: 4.3.1, 5.1.1.2.1

PURPOSE: This method verifies that all aircraft type A ASI transfer paths meet the return loss requirements.

PARAMETER TYPE: ☒ ELECTRICAL ☐ PROTOCOL ☐ PHYSICAL
VERIFICATION TECHNIQUE: ☒ TEST ☐ ANALYSIS ☐ INSPECTION

VERIFICATION CRITERIA: The aircraft is considered to have passed if the input and output Return Loss measured is not less than 20 dB from 20 Hz to 20 MHz when properly terminated.

APPARATUS:

- a. Network Analyzer (20 Hz to 20 MHz) capable of 50 and 75 Ω measurements
- b. Adapters cables (50 and 75 Ω) for connecting the test equipment to the ASI
- c. Calibration standards (50 and 75 Ω) including impedance matching attenuator

VERIFICATION METHOD:

The input and output return loss of HB1 and HB3 shall be measured from 20 Hz to 20 MHz.

NOTES:

1. The network analyzer uses type N or SMA connectors that will not mate with the size 12 coaxial contacts used by the MIL-STD-1760 ASI. Therefore, an adapter cable will be required to connect the network analyzer cable to the size 12 coaxial contacts. The calibration standards will connect directly to the network analyzer. The adapter cable will not be included in the network analyzer calibration. However, the adapter cable should be normalized with the network analyzer after the analyzer has been calibrated.
2. The open end of the signal path must be terminated with the characteristic impedance during the return loss measurement. HB1 must be terminated with 50 Ω and HB3 must be terminated with 75 Ω .
3. The test set up is shown in Figure A1.
4. If multiple paths through the aircraft routing network are possible, then each path shall be validated.

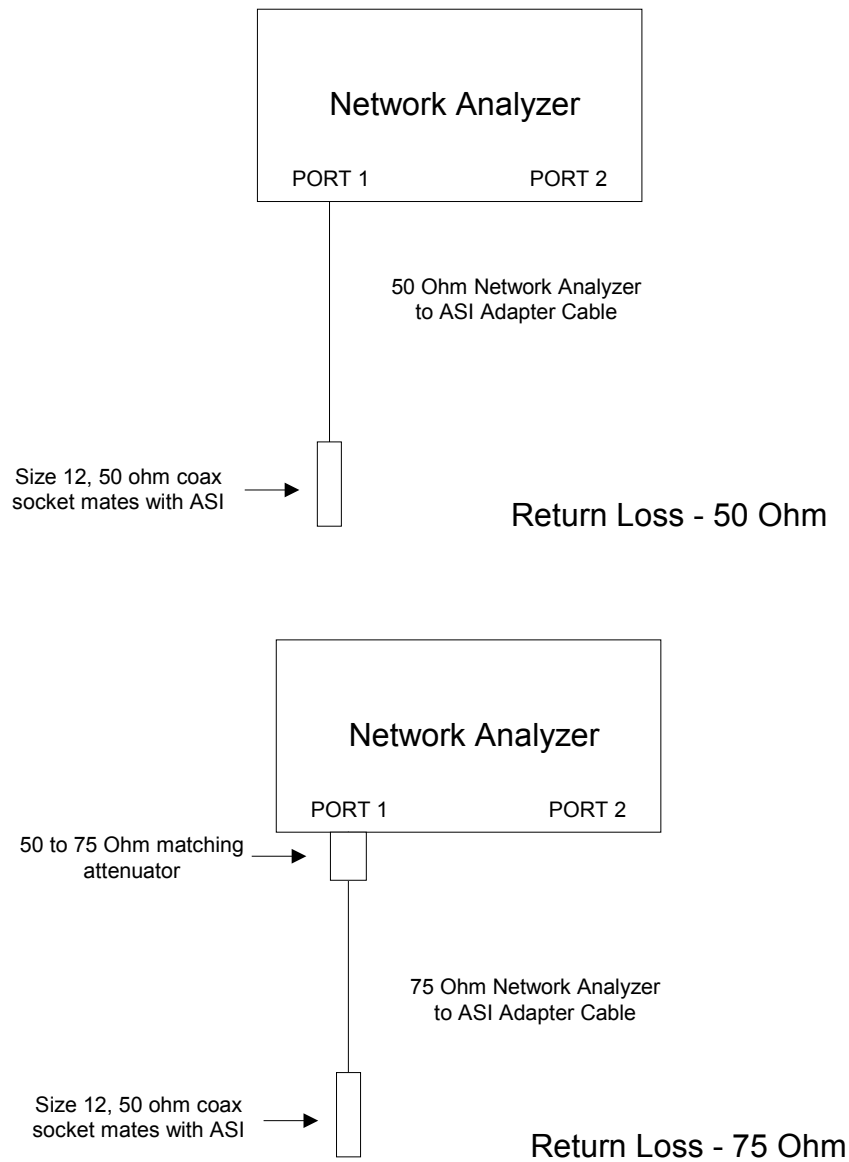


Figure A1 - HBW109

METHOD: HBW110

PARAMETER: Type A Transient Response

MIL-STD-1760E PARAGRAPH: 5.1.1.2.2, Figure 5b, Figure 6b

PURPOSE: This method verifies that all aircraft type A ASI transfer paths meet the transient response requirements.

PARAMETER TYPE: ☒ ELECTRICAL ☐ PROTOCOL ☐ PHYSICAL
VERIFICATION TECHNIQUE: ☒ TEST ☐ ANALYSIS ☐ INSPECTION

VERIFICATION CRITERIA: The aircraft is considered to have passed when the transfer path output signal falls within the allowed response envelope described by Figures 5b (Allowed response envelope cosine-squared T), 6b (Allowed response envelope for cosine-squared 2T) and 8b (Allowed response envelope for 2T bar) of MIL-STD-1760. Each figure contains several pass/fail verification test criteria.

APPARATUS:

- a. Arbitrary Waveform Generator
- b. Oscilloscope capable of displaying 50 ns rise time pulse
- c. Adapters cables (50 and 75 Ω) for connecting the test equipment to the ASI
- d. 50 and 75 Ω BNC 'T' with 50 and 75 Ω loads
- e. Impedance matching attenuator

VERIFICATION METHOD:

Connect the output of the waveform generator to the input of the ASI port to be measured. Connect the oscilloscope to the output of the ASI port to be measured. Compare the oscilloscope's output waveform, described in the Verification Criteria, to the input response envelope described in MIL-STD-1760 Figure 5a (Cosine-squared T), 6a (Cosine-squared 2T) and 8a (2T Bar).

NOTES:

- 1. The test set up is shown in Figure A2.
- 2. If multiple paths through the aircraft routing network are possible, then each path shall be validated.
- 3. HB1 is a 50 Ω signal path.
- 4. HB3 is a 75 Ω signal path.
- 5. All signal paths must be terminated with their correct characteristic impedance.

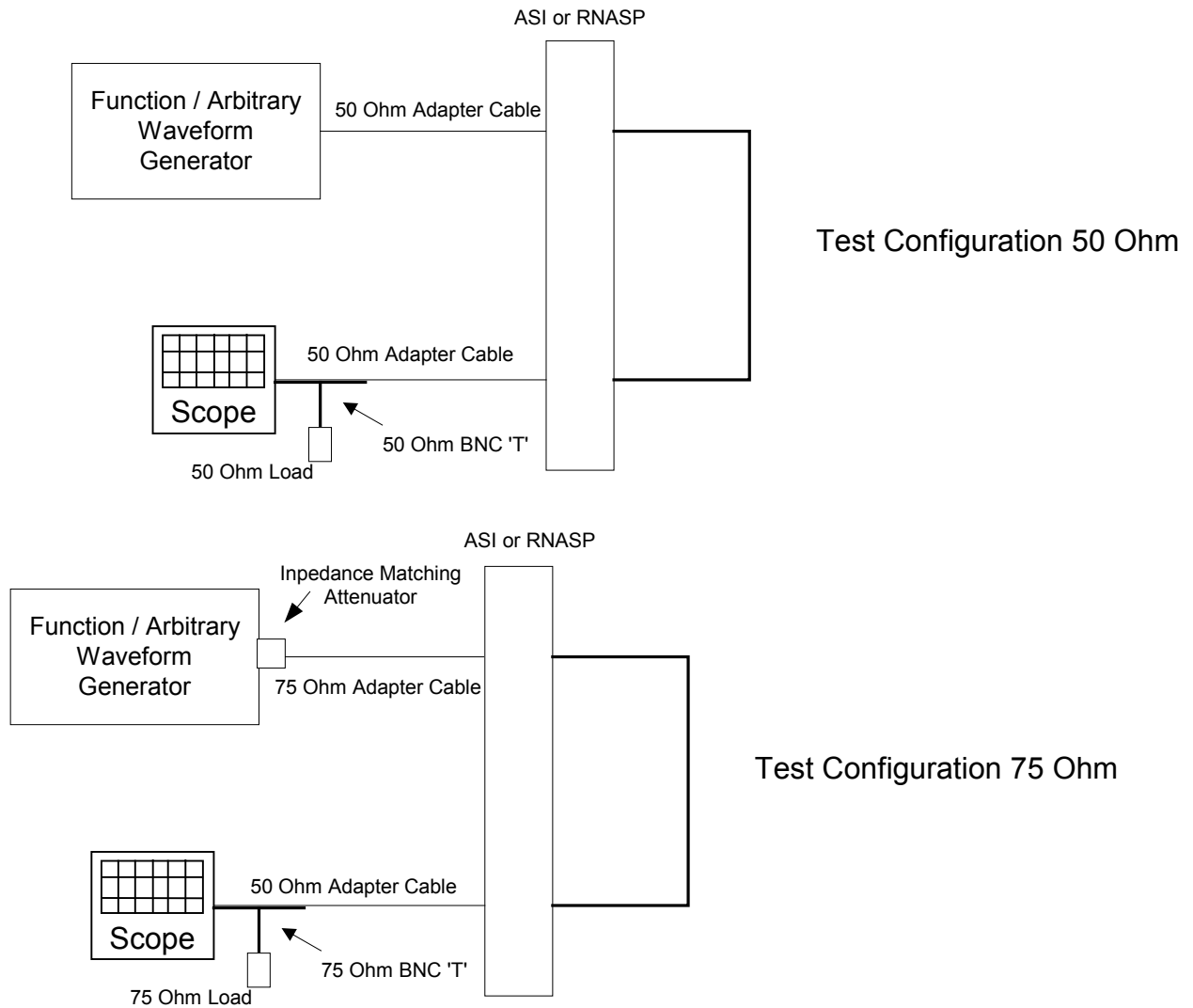


Figure A2 - HBW110

METHOD: HBW111

PARAMETER: Insertion Gain

MIL-STD-1760E PARAGRAPH: 5.1.1.2.3

PURPOSE: This method verifies that all aircraft type A ASI transfer paths meet the insertion gain requirements.

PARAMETER TYPE:	☒ ELECTRICAL	☐ PROTOCOL	☐ PHYSICAL
VERIFICATION TECHNIQUE:	☒ TEST	☐ ANALYSIS	☐ INSPECTION

VERIFICATION CRITERIA: The aircraft is considered to have passed if the signal insertion gain between the input and output is not more than 0.5 dB and not less than -4.0 dB.

APPARATUS:

- a. Arbitrary Waveform Generator
- b. Oscilloscope capable of displaying 50 ns rise time pulse
- c. Adapters cables (50 and 75 Ω) for connecting the test equipment to the ASI
- d. 50 and 75 Ω BNC 'T' with 50 and 75 Ω loads
- e. Impedance matching attenuator

VERIFICATION METHOD:

Configure the waveform generator to produce waveform described by MIL-STD-1760 Figure 8a (2T Bar). Connect the output of the waveform generator to the input ASI port to be tested. Connect the oscilloscope to the output ASI port to be measured. Calculate the insertion gain from the output waveform displayed on the oscilloscope using the following formula: Insertion gain = $20 \log (V_{1.3}/V)$ where V and $V_{1.3}$ are defined in Figures 8a (2T Bar) and 8b (Allowed response for 2T Bar) respectively.

NOTES:

1. The test set up is shown in Figure A2.
2. If multiple paths through the aircraft routing network are possible, then each path shall be validated.
3. HB1 is a 50 Ω signal path.
4. HB3 is a 75 Ω signal path.
5. All signal paths must be terminated with their correct characteristic impedance.

METHOD: HBW112

PARAMETER: Representative Pulse Delay

MIL-STD-1760E PARAGRAPH: 5.1.1.2.4

PURPOSE: This method verifies that all aircraft type A ASI transfer paths meet the representative pulse delay requirements.

PARAMETER TYPE: ☒ ELECTRICAL ☐ PROTOCOL ☐ PHYSICAL
VERIFICATION TECHNIQUE: ☒ TEST ☒ ANALYSIS ☐ INSPECTION

VERIFICATION CRITERIA: The aircraft is considered to have passed if the pulse delay of any signal path does not exceed 2.0 microseconds and does not vary by more than ± 35 ns from its nominal value. The nominal value of the signal path representative pulse delay for the current routing path configuration shall be retained and made available for computing signal latency. The pulse delay is measured at the V/2 rising edge.

APPARATUS:

- a. Arbitrary Waveform Generator
- b. Oscilloscope capable of displaying 50 ns rise time pulse
- c. Adapters cables (50 and 75 Ω) for connecting the test equipment to the ASI
- d. 50 and 75 Ω BNC 'T' with 50 and 75 Ω loads
- e. Impedance matching attenuator

VERIFICATION METHOD:

Configure the waveform generator to produce waveform described by MIL-STD-1760 Figure 8a (2T Bar). Connect the output of the waveform generator to the input ASI port to be tested. Connect the oscilloscope to the output ASI port to be measured. Measure the pulse delay displayed on the oscilloscope. The representative pulse delay is the time difference between the voltage V/2 being measured on the input signal rising edge and the voltage $V_{1.3}/2$ measured on the output signal rising edge. V1.3 is defined in Figure 8b (Allowed response envelope for 2T Bar) of MIL-STD-1760. Evaluate the aircraft's TDP to determine if the aircraft HB distribution network retains the Representative Pulse Delay and makes it available for computing signal latency.

NOTES:

- 1. The test set up is shown in Figure A3.
- 2. If multiple paths through the aircraft routing network are possible, then each path shall be validated.
- 3. HB1 is a 50 Ω signal path.
- 4. HB3 is a 75 Ω signal path.
- 5. All signal paths must be terminated with their correct characteristic impedance.

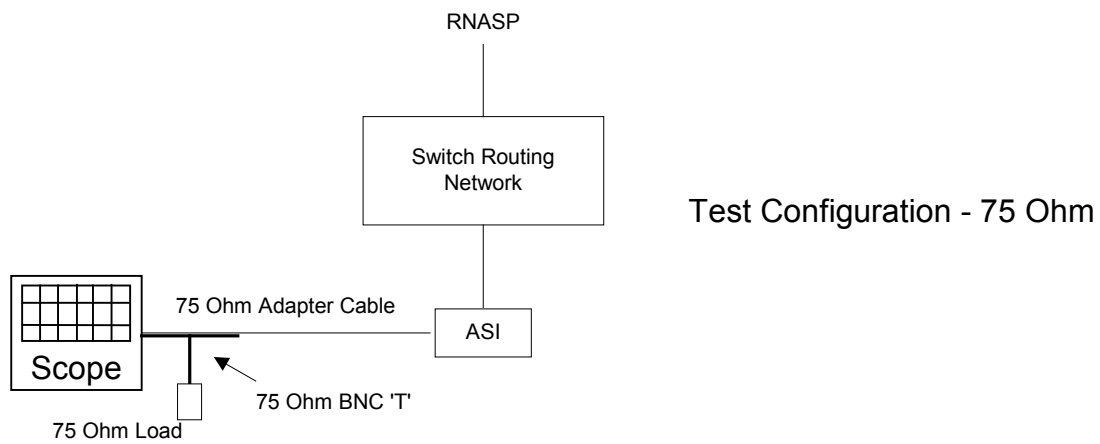
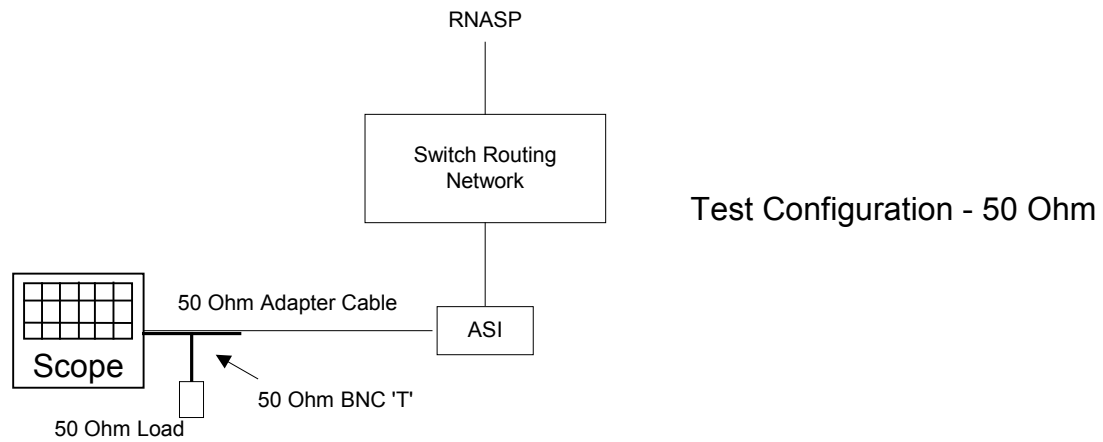


Figure A3 - HBW112

METHOD: HBW113

PARAMETER: Equalization

MIL-STD-1760E PARAGRAPH: 5.1.1.2.5

PURPOSE: This method verifies that all aircraft type A ASI transfer paths meet the gain equalization loss requirements.

PARAMETER TYPE: ☒ ELECTRICAL ☐ PROTOCOL ☐ PHYSICAL
VERIFICATION TECHNIQUE: ☒ TEST ☐ ANALYSIS ☐ INSPECTION

VERIFICATION CRITERIA: The aircraft is considered to have passed if the gain of any signal path is within the limits shown in Figure 9 (Gain misequalization envelope) of MIL-STD-1760. The zero dB reference gain shall be the gain at 20 KHz. The maximum gain between 20 and 200 MHz shall not exceed the envelope limits of 1760 Figure 9 (Gain misequalization envelope).

APPARATUS:

- a. Network Analyzer (20 Hz to 200 MHz) capable of 50 and 75 Ω measurements
- b. Adapters cables (50 and 75 Ω) for connecting the test equipment to the ASI

VERIFICATION METHOD:

Calibrate the network analyzer for insertion "loss/gain measurements" measurement. Connect the output of the network analyzer to the ASI input connector and the input of the network analyzer to the ASI output. Verify the gain is within the limits of MIL-STD-1760 Figure 9 (gain misequalization envelope) and the gain between 20 and 200 MHz is less than +3 dB with respect to the zero 0 dB gain reference.

NOTES:

- 1. The adapter cables that connect the network analyzer to the ASI must be included in the calibration procedure so that they are not part of the measurement.
- 2. The through calibration cable, used to calibrate the network analyzer for 0 dB attenuation, should be as short as possible to minimize the error introduced in the calibration.
- 3. The test set up is shown in Figure A4.
- 4. If multiple paths through the aircraft routing network are possible, then each path shall be validated.
- 5. HB1 is a 50 Ω signal path.
- 6. HB3 is a 75 Ω signal path.
- 7. All signal paths must be terminated with their correct characteristic impedance.

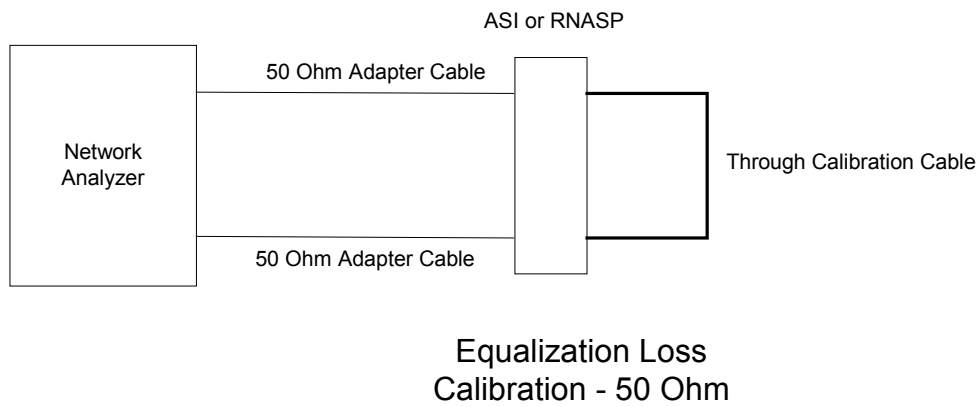
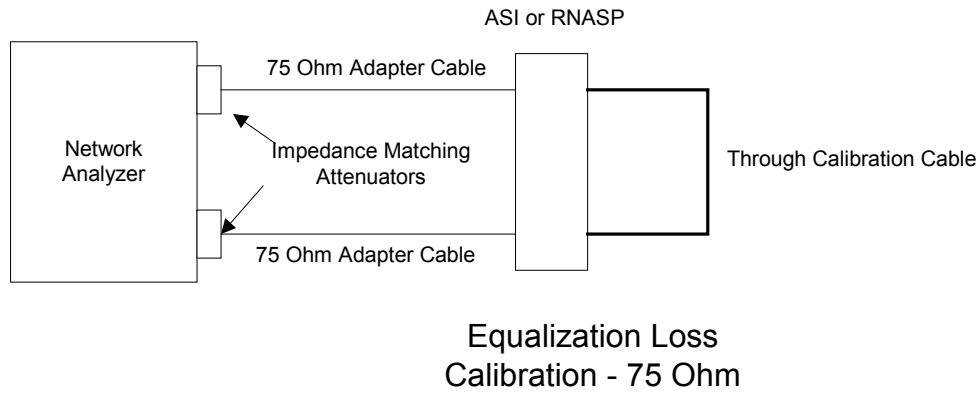


Figure A4 - HBW113

METHOD: HBW114

PARAMETER: Dynamic Range

MIL-STD-1760E PARAGRAPH: 5.1.1.2.6

PURPOSE: This method verifies that all aircraft type A ASI transfer paths meet the dynamic range requirements.

PARAMETER TYPE: ☒ ELECTRICAL ☐ PROTOCOL ☐ PHYSICAL
VERIFICATION TECHNIQUE: ☒ TEST ☐ ANALYSIS ☐ INSPECTION

VERIFICATION CRITERIA: The aircraft is considered to have passed if the dynamic range of any signal path is not compressed or clipped by more than 6%.

APPARATUS:

- a. Function generator capable of producing a 3.5 V P-P, 1 kHz sine wave and capable of supplying a DC offset.
- b. Oscilloscope
- c. Adapters cables (50 and 75 Ω) for connecting the test equipment to the ASI.
- d. 50 and 75 Ω BNC 'T' with 50 and 75 Ω loads

VERIFICATION METHOD:

Input a 1 kHz sine wave, 3.5 V P-P with a ± 0.5 VDC component into the signal path input. Verify on the oscilloscope, the signal at the output is not compressed or clipped by more than 6%.

NOTES:

1. The test set up is shown in Figure A2.
2. If multiple paths through the aircraft routing network are possible, then each path shall be validated.
3. HB1 is a 50 Ω signal path.
4. HB3 is a 75 Ω signal path.
5. All signal paths must be terminated with their correct characteristic impedance.
6. The ± 0.5 VDC component is an offset measured from 0 VDC to the mean of the sine wave.

METHOD: HBW115

PARAMETER: Signal Path DC Offset

MIL-STD-1760E PARAGRAPH: 5.1.1.2.7

PURPOSE: This method verifies that all aircraft type A ASI transfer paths meet the DC offset requirements.

PARAMETER TYPE:	☒ ELECTRICAL	☐ PROTOCOL	☐ PHYSICAL
VERIFICATION TECHNIQUE:	☒ TEST	☐ ANALYSIS	☐ INSPECTION

VERIFICATION CRITERIA: The aircraft is considered to have passed if the maximum dc voltage at each output of each signal path does not exceed ± 250 mV with the input terminated in its characteristic impedance.

APPARATUS:

- a. Oscilloscope
- b. Adapters cables (50 and 75 Ω) for connecting the test equipment to the ASI
- c. 50 and 75 Ω BNC 'T' with 50 and 75 Ω loads

VERIFICATION METHOD:

Connect the oscilloscope to the signal path output with proper impedance matching. Apply power to all aircraft systems that connect to the RNASP. With the input properly terminated, verify the signal at the output does not exceed ± 250 mV.

NOTES:

- 1. The test set up is shown in Figure A3.
- 2. If multiple paths through the aircraft routing network are possible, then each path shall be validated.
- 3. HB1 is a 50 Ω signal path.
- 4. HB3 is a 75 Ω signal path.
- 5. All signal paths must be terminated with their correct characteristic impedance.

METHOD: HBW116

PARAMETER: Random Noise

MIL-STD-1760E PARAGRAPH: 5.1.1.2.8, 5.1.1.2.8.1

PURPOSE: This method verifies that all aircraft type A transfer paths meet the random noise requirements.

PARAMETER TYPE:	☒ ELECTRICAL	☐ PROTOCOL	☐ PHYSICAL
VERIFICATION TECHNIQUE:	☒ TEST	☐ ANALYSIS	☐ INSPECTION

VERIFICATION CRITERIA: The aircraft is considered to have passed if the random noise power at each signal path output, with the input terminated, does not exceed -45 dBm RMS after the weighting function of MIL-STD-1760 Figure 10 (Random noise weighting function) has been applied.

APPARATUS:

- a. Power Meter capable of measuring down to at least -55 dBm RMS. Frequency response tailored to take account of the weighting function
- b. Adapters cables (50 and 75 Ω) for connecting the test equipment to the signal path input and output
- c. 50 and 75 Ω loads

VERIFICATION METHOD:

Connect the power meter to the output of the signal path with the proper impedance matching components. Replace the signal aircraft source feeding the signal path under test with a load of the proper impedance. Apply power to all aircraft systems that are necessary to support delivery of a weapon. Measure the random noise on the power meter.

NOTES:

1. The test set up is shown in Figure A5.
2. If multiple paths through the aircraft routing network are possible, then each path shall be validated.
3. HB1 is a 50 Ω signal path.
4. HB3 is a 75 Ω signal path.
5. All signal paths must be terminated with their correct characteristic impedance.
6. Random noise is defined as randomly occurring noise, which is distributed over a large bandwidth. Random noise, which is keyed on and off from time to time, is included.
7. The spectral components of random noise are random in phase. Therefore, doubling the measurement bandwidth doubles the measured power. For this reason, random noise is usually specified as some noise power per unit bandwidth (dB/Hz). The random noise pass criteria specified by MIL-STD-1760 specified a noise power (-45 dB m RMS) without a measurement bandwidth. Therefore, a power meter was selected for this test, which measures noise power independent of bandwidth. Some power meters do not allow the frequency response table to be edited. This approach using a power meter is simple providing the weighting function can be implemented.

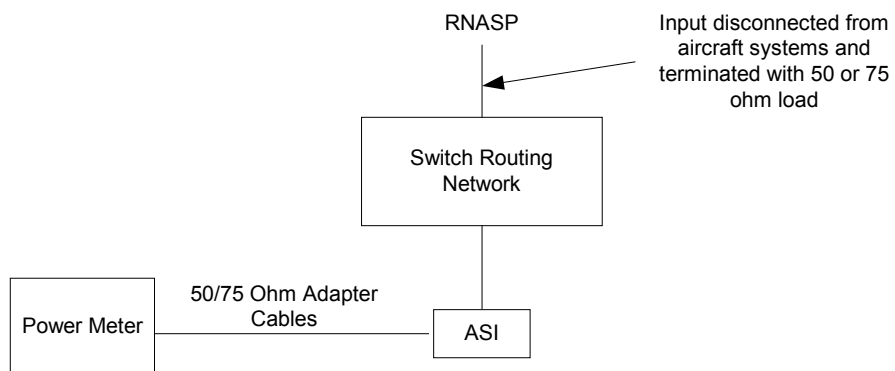


Figure A5 - HBW116